SIA Comments
On the
Octamethylcyclotetra-siloxane (D4); Manufacturer Request for Risk Evaluation Under the Toxic Substances Control Act (TSCA); Notice of Availability and Request for Comments

EPA–HQ–OPPT–2018–0443

CASRN 556–67–2

Submitted July 31, 2020

The Semiconductor Industry Association (SIA) submits these comments to the U.S. Environmental Protection Agency (EPA) on the Octamethylcyclotetra-siloxane (D4); Manufacturer Request for Risk Evaluation Under the Toxic Substances Control Act (TSCA); Notice of Availability and Request for Comments (CASRN 556–67–2).

SIA is the trade association representing leading U.S. companies engaged in the design and manufacture of semiconductors. Semiconductors are the fundamental enabling technology of modern electronics that has transformed virtually all aspects of our economy, ranging from information technology, telecommunications, health care, transportation, energy, and national defense. The U.S. is the global leader in the semiconductor industry, and continued U.S. leadership in semiconductor technology is essential to America's continued global economic leadership. More information about SIA and the semiconductor industry is available at www.semiconductors.org.

The semiconductor industry uses D4 in totally enclosed radio frequency (RF) plasma enhanced chemical vapor deposition (PECVD) processes to deposit a very thin dielectric layer (measured in nm) on the wafer surface (an article). This specific CVD process is a radio frequency plasma-enhanced CVD (RF PECVD) process, that results in a high level of material conversion and rearrangement of OMCTS into a very thin layer of a distinctly different material than OMCTS, called SiCOH. The term "SiCOH" describes the elements present in the thin dielectric layer (it does not represent the stoichiometry). The SiCOH film structures (composed of Si, C, O and H atoms) are extensively cross-linked with little relation to the molecular composition of the D4 precursor. It can best be described as an inorganic porous glass like structure, it also may be characterized as an organosilicate glass. To be clear: the resulting SiCOH dielectric layer does not include any D4 impurities (also please note that the resulting transistors in the semiconductor chip would not be functional with D4 impurities included).

The D4 that is fed into the PECVD tool is destroyed within the tool plasma, and any potential remaining D4 in the process exhaust is believed to be destroyed via point of use abatement at the process tool. There are no known emissions of D4 to the environment. D4 is not present in the wafer or in subsequent process steps; thus, the industry is not a processor of D4 and D4 itself is not incorporated in semiconductor devices. The 2019 total annual D4 usage by SIA members was less than 8,500 kg.

This document provides a summary of our industry's manufacturing process and the conditions of use of D4 in semiconductor manufacturing. As described in this document, the industry's use of D4 is unique and should not be bundled with other, dissimilar uses of this chemical. As EPA considers whether to undertake a risk evaluation of D4, these comments seek to inform EPA of the conditions of use in the semiconductor industry. Based on the information included here,

and if EPA were to proceed with a risk evaluation of D4, we recommend EPA conclude the semiconductor industry's use of D4 does not pose a risk to human health or the environment.

I. Background on Semiconductor Manufacturing

A. Overview of the Semiconductor Manufacturing Process

Semiconductor device fabrication is the process used to create integrated circuits that are present in electrical and electronic devices. An overview of semiconductor manufacturing process can be found in OECD emissions scenario documents.[1] The fabrication process (see Figure 1) begins with a wafer of semiconductor material varying in size from 150-300mm in diameter and includes a sequence of photographic and chemical processing steps during which electronic circuits are gradually created on the wafer substrate. These electrical circuits are made one layer at a time by the combination of depositing a layer on the surface of the wafer and using a patterning process to then remove designated parts of the layer to leave behind a specific shape. Advanced semiconductors may contain billions of transistors on a layer of silicon the size of a square centimeter, so manufacturing must be rigorously controlled and conducted with great precision to achieve features at the nanoscale. The basic steps of semiconductor manufacturing include:

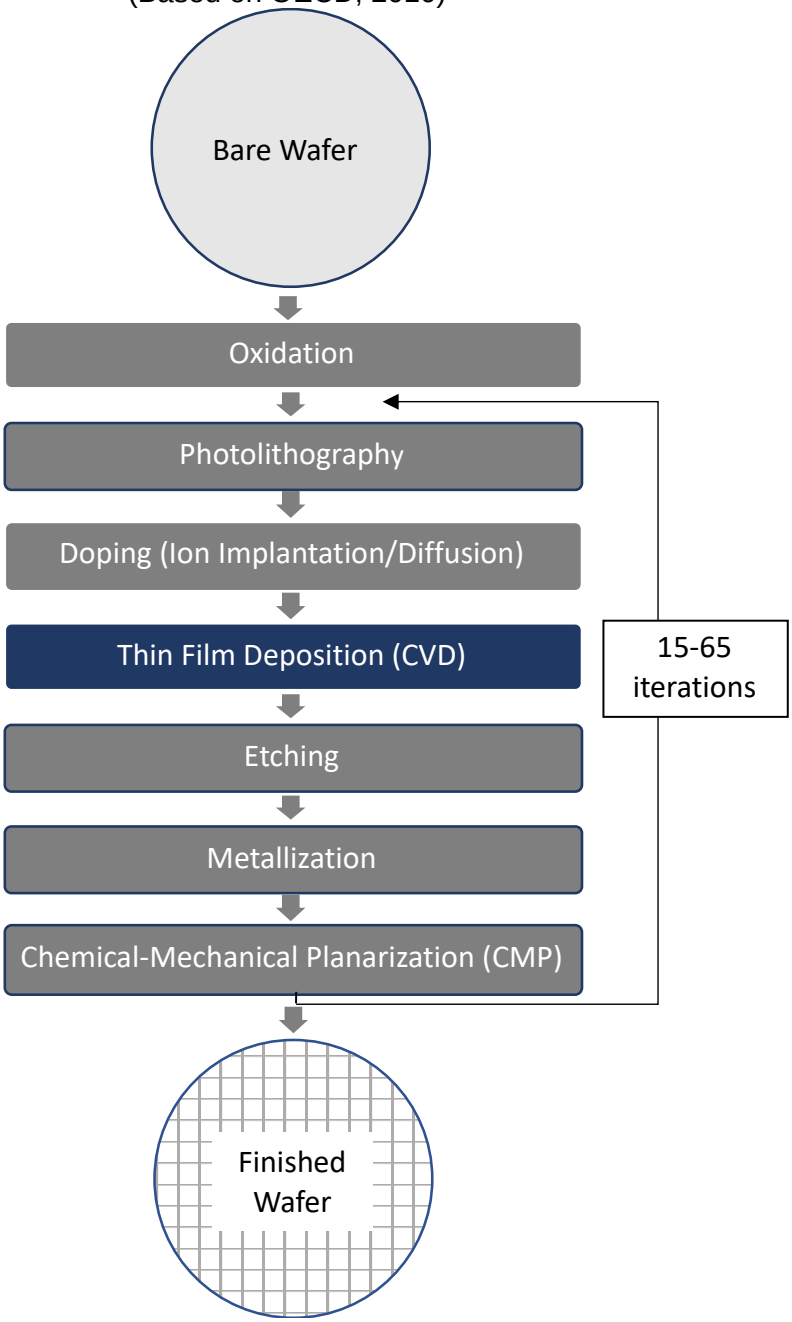
- Oxidation, a process usually performed at 800-1200 degrees C in a tube furnace, is a batch process that diffuses oxygen (O_2) or water (H_2O) vapor into the silicon wafer to form a silicon dioxide (SiO_2) layer that protects the wafer surface during subsequent steps.
- During the photolithography step, the wafer is coated with a layer of photoresist and subsequently covered with a mask that defines the specific patterns to be retained or removed in subsequent processes. In a typical processing scheme, the photoresist polymer formulation is applied to a spinning wafer, and then subjected to a pre-exposure bake to drive off a proportion of the solvent to impart dimensional stability to the film.
- The coated wafer substrate is then exposed thru a patterned photomask, with actinic radiation from a light source of specified wavelength. Reflectivity of the semiconductor material during light exposure can be problematic. To absorb light and reduce reflections during the exposure, a layer of anti-reflective coating is typically utilized. An anti-reflective coating applied after the photoresist is referred to as a top antireflective coating (TARC) agent and an anti-reflective coating applied before the photoresist is referred to as a bottom anti-reflective coating (BARC) layer.
- After exposure, the coated wafer substrate undergoes a development process whereby the previously exposed regions are selectively dissolved and removed from the photoresist film. This leaves the wafer surface with a patterned coating of photoresist, where in selected regions the resist material is completely removed, and where in the remaining areas the photoresist forms a protective coating. The open areas of the substrate may then be subjected to additive processes like physical vapor deposition, chemical vapor deposition, diffusion, ion implant or plating; or subtractive process like a plasma etch.

[1] ENV/JM/MONO(2015)5; ENV/JM/MONO(2004)14/REV1.

- In thin film deposition, a type of which is known as chemical vapor deposition (CVD),[2] thin layers or films are added to the wafer surface to change its electrical properties or to serve as masks. **Octamethylcyclotetra-siloxane** is used as a precursor in an enclosed RF PECVD process chamber to form a Si-C-O-H film on the wafer. D4 is not present in the wafer film; it is fully reacted in the process and subsequent point of use abatement and is not emitted to the environment.
- In etching, specific areas of a deposited film are chemically removed so that an underlying material is exposed or another material may be deposited. Etching may be performed in a wet process using solutions of acids, bases or oxidizers, or in a dry process using various gases in a plasma.
- In Doping/Diffusion, atoms with one less electron than silicon (such as boron) or one more electron than silicon (such as phosphorus) are introduced into the area exposed by the etch process, to alter the electrical character (conductivity) of the silicon. Diffusion is a high temperature batch process in which wafers are loaded into a quartz tube where impurities are added to change the conductivity of the surface layer.
- Subsequent to the etch or deposition process, the residual photoresist and anti-reflective coating must be removed from the wafer surface. This final step, known as the photoresist strip step, must be accomplished in a manner that completely and uniformly removes the residual photoresist, without adversely impacting the surfaces of the materials comprising the underlying wafer substrate (Dean et al, 1992; Lee et al, 1994).
- Cleaning occurs in various parts of the process flow and is also an important part of the wafer fabrication process as semiconductor devices are highly susceptible to various kinds of contamination such as particles, metal ions, chemicals, bacteria, and airborne molecular contaminants.
- Dielectric Deposition and Metallization - Following completion of the "front end," the individual devices are interconnected using a series of alternating metal depositions and dielectric films, with their respective patterning.
- Passivation- After the last metal is patterned, a final insulating layer (passivation) is deposited to protect the circuit from damage and contamination. Openings are etched in this film to allow access to the top metal later by electrical probes and subsequent wire bonds.
- Assembly and Packaging - A diamond saw slices the wafer into single chips. Sizes can vary from 1 x 1 mm to 76 x 56mm. Each chip is then assembled into an appropriate package that provides the contact leads for the chip. In one type of interconnect a wire bonding machine attaches wires, a fraction of the width of a human hair, to the leads of the package.

[2] A more complete description of the CVD process and potential release pathways for chemicals used as CVD precursors can be found in OECD No. 35: *Emission Scenario Document on Chemical Vapour Deposition In The Semiconductor Industry*, ENV/JM/MONO(2015)5.

Figure 1: Overall Process Flow Diagram – Semiconductor Manufacturing[3]
(Blue box signifies steps where Octamethylcyclotetra-siloxane may be)
(Based on OECD, 2010)



[3] Wafers undergo multiple iterations of the steps from photolithography to CMP, as indicated by the return arrow.

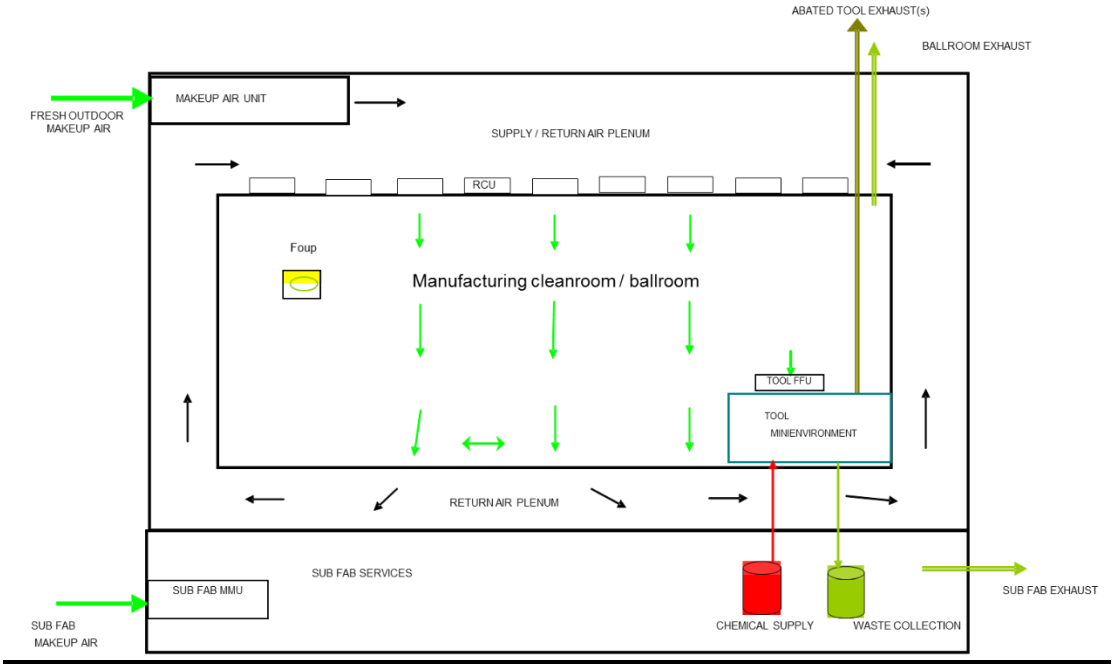
B. Semiconductor Manufacturing – Fab Cleanrooms and Equipment

The fabrication of semiconductors is conducted in specialized buildings known as “fabs” that involve the use of cleanrooms, and a hierarchy of design features that isolate workers and wafers from chemicals. The fab cleanroom design approach protects manufacturing personnel and is also critical to semiconductor wafer product quality. Figure 2 illustrates schematically the design of a typical 300mm fab. The fab consists of a cleanroom where the manufacturing operations are conducted, and an isolated ancillary space which contains chemical and air handling equipment, emission controls, and other infrastructure, and which is often located in an area within the building known as a “sub-fab”.

The fabrication of an integrated circuit on a silicon wafer involves a sequence of hundreds of additive, subtractive, photolithography, and cleaning steps that is accomplished by shuttling wafers between specialized manufacturing “tools” within which the individual unit operations are conducted on the wafer. The manufacturing tools, engineers and operators are located within the cleanroom, but the tools are supplied with chemicals, power, and other utility services from the subfab or other ancillary space.

As also indicated on Figure 2, fresh air is brought into the fab through an air conditioning unit that controls the fab air temperature and humidity and is recirculated through ultra-low particulate air (ULPA) filters before being exhausted to the building exterior. In a typical 300mm wafer manufacturing fab built in 2000, the entire volume of air in the fab cleanroom is replaced every 7 minutes, and the entire volume of air in the cleanroom is recirculated through the ULPA filters at a rate of once every 0.64 minute. This extensive level of air circulation and replacement provides an exceptional level of fab air cleanliness.

Figure 2. Schematic of airflow in a typical Fab.



In all semiconductor manufacturing, regardless of the level of sophistication of the factory, equipment systems operate with intrinsic controls that minimize or eliminate chemical liquid or vapor exposure potential during normal equipment operations. The equipment must be maintained frequently, which requires the operating parts of the equipment to be placed in stand-by (non-operating mode) and the opening of protective enclosures. During these maintenance activities, workers utilize protective equipment to reduce the potential for employee exposure. Older manufacturing equipment (150mm and older) is generally less sophisticated with varying degrees of protective equipment controls. In those cases, more PPE is used to protect the employee during operations. Even in these cases a high degree of engineering controls are used to ensure employee exposure is minimized including exhaust, interlocks, and monitoring. In all cases where engineering controls are not available, administrative controls are used to minimize the potential for exposure.

During fabrication, the wafers are highly susceptible to even minute amounts of contamination, and so the wafers are moved in and out of tools by robotics, placed robotically into enclosed boxes, known as front opening unified pods (FOUPs), and shuttled between tools via a computer controlled, automated transport system. Figure 3 shows manufacturing tools aligned along one of many corridors within a typical 300mm fab, and Figure 4 an automated transport system that shuttles FOUPs between tools.

Figure 3. Photo of typical 300mm wafer manufacturing cleanroom.

Figure 4. Robotic system moves wafers inside enclosed containers (FOUPs).

II. Use of D4 in the Semiconductor Industry

A. Overview of Semiconductor Uses of D4

Within that overall process flow, D4 is used as a technology critical precursor in a specific chemical vapor deposition (CVD) process of a specific dielectric layer that is a critical building block in transistors in advanced semiconductor technologies. This specific CVD process is an RF PECVD process, that uses D4 as a precursor chemical, and by the action of the plasma and co-reactants, converts it to a distinctly different material than D4, called SiCOH,[4] that is deposited in a very thin layer (measured in nm) on the silicon wafer. This resulting dielectric layer does not include any D4 impurities (in fact, the resulting transistors in the chip would not be functional if residual D4 impurities were present).

Docket document EPA-HQ-OPPT-2018-0443-0003.pdf, "Possible Conditions of Use (COU) Table for Octamethylcyclotetra- siloxane" describes a lifecycle stage of "Processing, Incorporation into formulation, mixture, or reaction product, Computer and electronic product manufacturing" and "Electrical equipment, appliance, and component manufacturing." These descriptions are not accurate for the use in semiconductor manufacturing, in which D4 reacts

[4] The term "SiCOH" describes the elements present in the thin dielectric layer (it does not represent the stoichiometry). The SiCOH film structures (composed of Si, C, O and H atoms) are extensively cross-linked. It can best be described as an inorganic porous glasslike material with a molecular structure, that has been reported to be similar to SiO2, but which also contains C and H atoms. It also may be characterized as an organosilicate glass.

and is not present in the finished wafer. The semiconductor industry are users, not processors, of D4 as that term is interpreted under TSCA.

B. Semiconductor Use is Essential

D4 use as a precursor for a specific dielectric layer deposition (thickness measured in nanometers) in advanced semiconductor technology manufacturing is essential and indispensable. This layer deposition step is part of the multiple step semiconductor manufacturing process flow.

The specific dielectric layer deposited from D4 as precursor is indispensable as it offers a unique combination of (thermos-)mechanical and dielectric properties that allows the transistors (up to several billion per individual chip) to function. The basic functionality requires the use of D4.

III. Controls in Semiconductor Manufacturing

A. Controls Employed with D4 Result in No Emission to the Environment

D4 use in the semiconductor industry is subject to significant levels of control. Manufacturing tools are equipped with exhaust interlocks to prevent an exposure during processing, a once-through closed path system, and pre-open purge and cleaning procedures.

D4 at 99.9% purity is provided to the fab in reusable, high integrity stainless steel containers. Container volumes range from 5 gallons to 200L. Upon receipt, the container is brought to a chemical delivery cabinet which has an automated sequence for connection and disconnection that avoids exposure of the operator to any liquid or vapor. While the container is physically connected and disconnected, the automated sequence manages purging of valves and lines using vacuum and high purity gas to clear lines before disconnecting. The cabinet is also exhausted to a scrubber and has liquid and vapor leak detection in the event of an accidental leak. Interlocks stop flow if a leak is detected. Once a container is connected, liquid is flowed through a sealed system to a vaporizer. Once in vapor form, the chemical is dispensed within a sealed process chamber to form a layer on a wafer.

After a defined number of SiCOH deposition steps in a RF PECVD tool, the RF PECVD tool process chambers that have been covered with SiCOH during the deposition step, are cleaned in a plasma cleaning process to remove all residues from the chamber.

In the process, the SiCOH material is deposited not just on the wafer but on the interior walls of the process chamber. Any unconverted D4 and vapor byproducts from the deposition and chamber clean processes are exhausted through an exhaust line to a point of use thermal abatement device which per standard practice operates at high temperature sufficient to achieve a very high destruction removal efficiency for D4 that is understood to be greater than 99 percent, reducing it to basic components such as SiO_2, CO_2 and water. The exhaust gas from the point-of-use abatement is typically routed to an acid exhaust system where a subsequent wet scrubbing process of the exhaust takes place. The resulting acid scrubber wastewater is typically routed to the site's industrial wastewater treatment plant.

RF PECVD tools do not have direct aqueous emissions. Also, under regular production conditions no waste is generated in the described RF PECVD process and empty D4 precursor

containers are returned to the supplier for reprocessing and refilling. Any liquid chemical remaining in the returnable container is recovered and re-purified.

In conclusion, in normal semiconductor manufacturing use, D4 is indicated to be fully transformed in the process and post-process abatement with no environmental release.

B. No Worker Exposure to D4 in Semiconductor Manufacturing

Semiconductor manufacturing takes place in a strictly controlled and safe production environment (the cleanroom). All manufacturing processes are performed in dedicated and enclosed process equipment, in this case in a RF PECVD tool. Generally, the presence of uncontrolled particles, as well as impurities in the form of chemical vapors and gases in the cleanroom constitutes an unacceptable risk from a production quality viewpoint and, therefore, are rigorously controlled.

There is also no worker exposure in the following steps that occur in addition to the actual CVD deposition step:

- D4 containers as supplied by the supplier are connected to the chemical delivery system as delivered - no filling or mixing or similar steps take place. The delivery of the D4 from the subfab delivery system to the RF PECVD process chamber is through a Helium purged line. D4 is heated and vaporized to the gas phase and Helium is used as a carrier gas. The gas box is equipped with leak detection. D4 container changeouts do not require any emptying or filling or cleaning of the D4 containers, or any tool opening, or tool shut down.
- Maintenance of RF PECVD tool chambers is only done after completion of the automated plasma cleaning step of the closed RF PECVD tool chamber that removes all residues from the chamber and purging of the tool chamber and exhaust lines. No chemical residues are expected to be present.
- Also, we would like to note that no in-process sampling is performed.

Semiconductor fabs employ extensive and redundant controls to minimize the exposure of workers to chemicals of concern. The typical risk management measures and safety practices deployed at fabs to prevent D4 releases and worker exposure include the following:

- Fabs employ professional industrial hygienists that evaluate and control potential workplace exposures.
- Extensive engineering controls to prevent employee exposure.
- Extensive training in hazard communication, safe handling of chemicals, and proper use of personal protective equipment.
- Chemical storage, dispense and handling:
    - Segregated Storage per local codes
    - Automatic, ventilated, and fully enclosed supply and discharge systems
    - Personal protective equipment (PPE) worn during container change out (chemical resistant gown, chemical protective gloves, safety glasses/goggles, and face shield)
    - General ventilation and local exhaust ventilation
- Routine semiconductor manufacturing operations:
    - Process tools are located in the clean room where a stringent clean regime is maintained as a requirement for production which also ensures no chemical releases
    - Closed systems

  - Continuous local exhaust ventilation under alarm
  - Automated chemical delivery (no chemical pouring)
- Invasive maintenance
  - Tool purged prior to invasive maintenance
  - Maintenance occurs at room temperature under local exhaust ventilation
  - Wearing of proper PPE as required.

D4 is used under highly controlled conditions and there is no expectation of worker exposure.

IV. Conclusion

The semiconductor industry is a user, not processor, of D4 because as described above D4 is completely reacted and does not remain present in any finished article which is distributed in commerce. The semiconductor industry uses D4 in totally enclosed RF PECVD processes to deposit a dielectric layer on the wafer surface (an article), a use that is unique and should not be clustered with other uses that are dissimilar. The D4 is transformed in the deposition process and any residual D4 in the tool exhaust is destroyed in the subsequent abatement device. The industry does not process D4 and D4 itself is not present in semiconductor devices.

As EPA considers whether to undertake a risk evaluation of D4, these comments seek to inform EPA of the conditions of use in the semiconductor industry, a use that is unique and should not grouped with other industrial uses. Based on the information included here, and if EPA were to proceed with a risk evaluation of D4, we recommend that EPA conclude that the semiconductor industry's use of D4 does not pose a risk to human health or the environment. As EPA continues its work on the scoping of D4 and the future risk evaluation, we look forward to working closely with EPA to properly characterize the uses and potential risks in the semiconductor industry.