

## Questions and Answers from SIA/SRC Webinar on the Decadal Plan for Semiconductors

<https://www.semiconductors.org/events/webinardecadal-plan-for-semiconductorssetting-the-2030-goals/>

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### 1. Will the slides be available for download?

Yes, they are available now at the SIA webinar event page -

<https://www.semiconductors.org/events/webinardecadal-plan-for-semiconductorssetting-the-2030-goals/>

### 2. What's difference between SIA and SRC? Are they competing organizations?

- SIA and SRC are separate, partner organizations with a successful track record of driving innovation in the US and across the globe.
- SIA seeks to strengthen U.S. leadership in semiconductor manufacturing, design, and research by working with Congress, the Administration, and key industry stakeholders to encourage policies and regulations that fuel innovation, propel business, and drive international competition. SIA advocates and organizes industry action on:
  - Defining strategies to promote and maintain world leadership in technology
  - Advocating for public policies that provide a fair field for competition
  - Promoting fair and open trade
  - Tracking and distributing statistical information of market trends
- From the SRC website on mission and vision (<https://www.src.org/about/mission/>), SRC establishes and operates programs that drive and meet industry's future technology needs and creates a pipeline of relevantly educated talent. SRC addresses its mission by creating the following outputs:
  - Research
  - Talent
  - Creation of and access to intellectual property
  - Global, integrated university capabilities
  - Networking opportunities for members

### 3. Does SRC have newsletter we can sign up to get latest info if not affiliated with any member company?

SRC has a monthly newsletter that can be subscribed to by emailing [newsletter@src.org](mailto:newsletter@src.org).

You can also learn more at our website, [www.src.org](http://www.src.org) and follow SRC on Linked In,

<https://www.linkedin.com/company/semiconductor-research-corporation/>.

### 4. I would like more details about the Decadal Plan for Semiconductors?

The detailed report is forthcoming – ideally by the end of 2020.

**5. Is there linkage with this effort to the SIA's semiconductor technology roadmap or other roadmaps?**

The SIA discontinued its participation in the ITRS after the 2013 edition. The ITRS was primarily aimed at constructing a detailed roadmap for the continuation of feature scaling for a rolling 15-years. The purpose of the ITRS roadmap was to identify the evolution of CMOS technology node target parameters (note: with the ITRS was no longer being updated, the CMOS technology node naming has now lost its comparative importance).

In contrast, the Decadal Plan is aimed at identification of the "seismic" shifts (the goals) which need to be addressed by research over the next decade in order to continue progress in information technology. The Decadal plan calls for the invention of revolutionary materials and devices for energy efficient circuits, algorithms and architecture technologies. A path/roadmap to do this cannot yet be identified. A strategy on where to focus the main research investments is needed to identify the leading options to explore. This will involve fundamental applied science investments for materials, devices and circuits coordinated with the algorithm, and architecture research.

**6. SRC/SIA have been well known for the forward looking work for the industry and the world, resulting in famous semiconductor technology roadmap, for example. The current decadal plan seems to be fittingly more complex and holistic. Will there be a more detailed roadmap in the future?**

The Decadal Plan is aimed at identification of the "seismic" shifts (the goals) which need to be addressed by research over the next decade in order to continue progress in information technology. A path/roadmap to do this cannot be identified yet. The document identifies the what, not the how. Having said that, a strategy on where to focus the main research investments is needed to identify the leading options to explore. There are indeed plans to develop further documents detailing specific needs. We'd like to see that develop into a roadmap.

**7. In the ITRS there was a cross trust activity that included a discussion on risk related to materials and manufacturing that could be limited or impacted by regulatory or other issues related to the environment and/or employee/community human health. While those may not be currently addressed in the decadal plan, were any provisions made to include those in future revisions? When might that be feasible to include and how would an effort to address that best be formed and who would that group work with to facilitate the addition?**

The ITRS was a detailed roadmap and the work here is a bit higher level. As this research explores new materials for new devices and structure, manufacturability and safety will need to be considered. There will be opportunities to include these considerations (including costs) once the technical or performance value of the new materials/devices is demonstrated. This can also be addressed in specific project formulations.

The purpose of the Decadal Plan is to identify the principal challenges – “seismic shifts”- requiring research that would enable continued progress in information technology. Some of the research addressing these needs may indeed involve new materials. Of course, at some point in the down-selection toward practical application of such solutions it would be necessary to verify ESH, and such further research would be encouraged. Of course, in most cases, the scope would drive toward ESH-expert researchers. At a high level, the "seismic shifts" are challenges of such magnitude that we should pursue a broad search for new concepts. Currently, the industry is working with congress and federal agencies to arrange for public-private funding of research areas of mutual interest. We are not yet at the point of organizing into specific groups for each of the individual areas.

- 8. Two questions: (1) As you are thinking about the fifth seismic shift to new computing paradigms to overcome the energy restrictions, what timeframe realistically are we talking about? Isn't it more likely to be in a period post 2030? (2) Would the seismic shift in Analog translate into higher importance or value claim to the analog semiconductor suppliers?**

(1) New computing architectures and "paradigms" will be transitional through the next decade with some applied earlier and others may be beyond 2030. Areas such as neural morphic processing can be implemented in accelerators shorter term while whole scale computation architectures will come later. Some additional near-term capabilities will arise from the co-design of new forms of hardware accelerators (possibly with reconfigurability), that are integrated into heterogeneous SoC processors CIM, smart NIC, or IoT sensors. These accelerators are application/algorithm driven and intended to provide energy-efficient performance over general purpose CPU and GPUs. Longer term, post 2030, it is possible that heterogeneous computing can extend to integrate quantum computing "accelerators."

(2) Analog semiconductors are foundational to many of the seismic shifts including sensing, communications, computing and storage. They will continue to be and analog technology will increase in value as new capabilities such as smart sensing and THz technologies be more widely applied. While the plan has articulated 5 shifts, there is a high level of interdependence: all semiconductor areas will continue to rise (and need to) and analog semiconductors with them and may increase but certainly will not decrease in importance or value.

- 9. There are a lot of logos of larger industry incumbents that have been shown in these slides. But do smaller players and startups have a role to play here too? How do they fit into the industry - SRC - academia model that has been framed here? Does any of the proposed**

**funding help fund disruptive startups that are working on R&D for in-memory compute, analog ML, new devices, etc.?**

The Decadal Plan for Semiconductors is designed to identify problems and opportunities for all members of the research community to innovate upon and solve. This includes academic, government, and industrial stakeholders from companies of all shapes and sizes. It is a call for an increased federal commitment to semiconductor investments to drive future ICT breakthroughs.

While startups are a vital part of that equation, SRC's members provide SRC with funds that are then, in turn, used to drive competitively selected university research. As start-ups are often looking to receive funds rather than provide SRC (and universities) with funding, those two forces are often at odds with each other. This is where an existing start-up is better served by DARPA, NSF, or other SBIR operations. SRC does encourage the creation of new start-ups out of its university research catalog and will be looking to do more of that in the years ahead.

**10. What is the impact on neuromorphic chips going forward and what are the challenges?**

Please see the answer to question #11, below.

**11. There are five separate groups, IDMs, and government labs funding the neuromorphic chip development area. Has this work moved into a competitive stage versus the pre-competitive stage, where companies work together?**

Special purpose neural accelerator integrated circuits which efficiently train and execute neural networks have become a topic of broad-ranging research and development. Work in this area ranges from near term development of neural chips relying on production CMOS which execute run well-developed algorithms, all the way to exploratory research. Greatly expanded basic research is needed which explores new materials, devices, architectures, and algorithms that will maximize energy efficiency, performance, scalability, and functionality in new neural chips. The Decadal Plan will focus on this pre-competitive, long horizon research which has the potential for major advancements. Our research programs will be closely coordinated with the currently funded US Government programs and initiatives on neural accelerator technology.

**12. The emphasis in Goal #1 for sorting meaning from raw data is intriguing. The human brain has decent systems for categorizing data from one-time-useful up to better-store-this-a-long-time by either assigning a high value on first reception by recognizing context, or promoting items upon multiple receptions. It would be interesting to understand trends in the grand goal to assist in such categorizing.**

This is an good and interesting question. The "Grand Goal #1" of 100,000:1 reduction of data is to address the challenges of moving, storing and computing in as local as possible to take action

- or as a local level of information hierarchy. As highlighted in the webinar, human senses such as vision and hearing reduce the broad spectrum of nature to key components for further processing. Also, there is a "learning" function of what is important to "retain" or not as well as what may need to be communicated to a higher level - even to the cloud for global analytics. Humans do this initially on preservation or pain avoidance - get burned once and likely to remember how not to get burned again.

The notion of "digitizing the sensor" and passing data to a central location for processing runs into limits around communication bandwidth, latency, storage, and processing. As "big data" grows exponentially bigger, this "data deluge" becomes a problem behind several of the seismic shifts. This calls for re-examination of how we move from SIGNAL to DATA to INFORMATION to INSIGHT to DECISION to ACTION. Biological systems (including human cognition) offer some interesting inspiration for different possibilities.

Communication networks are built incrementally and naturally evolve with applications needs. Understanding of major seismic shifts in compute and storage requirements and research in semiconductor technologies & standards like 5G & 6G will help overcome the impact of seismic shift by smoothening the transition phases.

**13. We need more information on the comparison of various devices based on Fe devices, Spin devices, TFETs and phase change devices in comparison to CMOS. Which is considered to have more impact in the future?**

A] We need more information on comparison of various devices based on Fe devices, Spin devices, TFETs and phase change devices in comparison to CMOS. Answer: Some suggested papers on benchmarking exploratory devices compared to CMOS:

- D. E. Nikonov and I. A. Young, "Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits," in IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 1, pp. 3-11, Dec. 2015, doi: 10.1109/JXCDC.2015.2418033.
- C. Pan and A. Naeemi, "An Expanded Benchmarking of Beyond-CMOS Devices Based on Boolean and Neuromorphic Representative Circuits," in IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 3, pp. 101-110, Dec. 2017, doi: 10.1109/JXCDC.2018.2793536.

B] Which is considered to have more impact in future? Answer: Solutions with platform potential, i.e. excelling over CMOS on all key metrics, will have most impact; those options along with other alternatives are still subject of active research.

**14. Regarding compute/energy efficiency: (1) What role do memristor-based processors play? and (2) What role do non-Si based semi play (GaN, SiC)?**

(1) Memristor-based (or cross-point analog processing) will have value for neural net type processing where parallel multiply and sum is useful. The additional value of memristor is potential for learning and storing parameters. Not as a general purpose processor.

(2) Wide-bandgap and similar technologies clearly have a role in power conversion and distribution for compute solutions. Distribution of power at higher voltages reduces distribution loss but requires higher voltage devices at higher frequencies to facilitated down conversion to chip level voltage but at high currents. Size becomes increasingly important as this power conversion is need at a "card" level in a server for example. The small size also exacerbates the efficiency challenge since smaller areas(volumes) cannot dissipate as much heat. Wide-bandgap and Ultra-wide-band-gap technologies can address these challenges and applications.

**15. The speakers talked about needing 'radically new memory and storage solutions'. Speaking as someone working a novel memory technology (universal memory), I have found that the semiconductor industry is generally very conservative. To what extent do you recognize that, and what can be done about it?**

The main factors contributing to the "conservative" behavior of the industry stems from 2 main factors: (1) the research and development expense involved in bringing radically new memory and storage technologies to market; (2) extant systems are already designed to work around the deficiencies of the current technologies and while radically new technologies may be technically better, in practice they are often only actually better when coupled with significant changes to the systems or applications running on them.

Additionally, novel memory technologies that may be viewed as "universal memory," may look reasonably good on paper for single or few devices, like for instance many ReRAM (incl CBRAM), and even PCRAM cells. However, when one looks at the device statistics (esp. Roff & endurance), the device to device variability (due to the stochasticity in atomic motion) precludes very large array implementations. This variability generally gets exaggerated with device scaling (volume shrink). New sorts of methodologies for computation that are error tolerant can possibly harness systems with stochasticity, but they are likely going to be limited to some niche set of problems, and thus difficult for large semiconductor companies to make profitable-- memory and logic companies make need chips that sell in the billions. Beyond reliability and scalability, device properties like Ion/Off ratio, switching voltage, and switching current density must be amenable to large scale device integration. Other times, the technology necessary to make devices work in VLSI is just too difficult (i.e. costly) like some technology that has been proposed requiring very high quality single crystal materials to be integrated with Si, or the thermal budgets for such integration are not feasible.

For a novel "universal memory" to be competitive, it must fill a lot of buckets. So, what from the outside may look to be conservatism, is often largely practicality when viewed from the eye of industry.

**16. Do you think Compute-In-Memory (CIM) will happen?**

Computing systems are rapidly changing from general purpose compute platforms to more heterogeneous compute platforms heavily using domain specific accelerators like GPUs, TPUs, Smart NICs and FPGAs. Data-centric computing where memories perform low ops/byte operations in the memory itself can be viewed as just another kind of domain specific accelerator. The main hurdle to data-centric computing is the associated programming model. This parallels the challenges that the other domain specific accelerators faced and addressed with CUDA, TensorFlow, and other domain specific languages.

**17. Software is always the tail that wags the dog. Is the intent to migrate existing software to the new architectures, or is it that new applications will be developed to use the heterogeneous environment?**

For High Performance Computing (HPC), the intent is to leverage existing software (modeling & simulation applications, algorithms & solver libraries, open source system software stack) where feasible. There is an expectation that these future "Converged Application" workloads/workflows will integrate HPC Modeling & Simulation applications with a wide portfolio of Data Science methods including: AI/ML, Uncertainty Quantification (UQ), Graphs, Streaming Analytics, etc. Many of these application software capabilities are existing, but new compilers and runtime system software will need to be "co-designed" to map these converged applications to the advanced heterogeneous computer architectures. Of course, the availability of new heterogeneous computing capabilities will likely motivate the development of new types of applications and algorithms that were not feasible/realistic with previous computing capabilities.

**18. If research is changing, should educational practices change to support this?**

Both the "challenges" and "promising technologies" call for a depth of technical expertise across a variety of fields, from materials to algorithms. The other theme that is recurring through the Decadal plan is a call for "holistic" and "system" approaches: more than ever before, research will need to work across domain boundaries to create the necessary breakthroughs. This calls for multi-disciplined individuals and the ability to work effectively in teams.

**19. What do countries in SE Asia especially Malaysia need to focus on (educating) the next 10 years to stay relevant.**

Comments on education in general – Graduate schools will still need to train scientists and engineers in their areas of technical specialization. But once this foundation is established, graduate students need to be exposed to multi-disciplinary collaborations. This is the foundation for co-design that will be needed to address the energy efficient computing challenges and other seismic shifts described in the Decadal Plan. This is not just hardware

architects collaborating with software developers. It extends to domain experts understanding enough of the capabilities of ICT to communicate what tradeoffs and priorities meet their needs. Specialists also need exposure and education with generalists. This is a role for SRC, Industry, and National Labs.

**20. How do you persuade younger people to consider hardware as well as software?**

See answer to question #21 - part 2.

**21. (1) How to overcome the seismic shifts that you identified here? (2) There will be a STEM talent crunch for sure, because there are distractions from other interesting undertakings in other fields such as med-tech, smart mobility, ...etc., and not to mention China, who is doling out high salaries to lure experienced talents away. How can these obstacles be overcome?**

(1) The Decadal Plan was created to address the "What" and the "How" that could be met by research with increased funding. The final report highlights many promising directions but not the solution. Much as John F. Kennedy said in 1962 that the US was going to put a man on the moon (what) by the end of the decade (when) and return him safely to earth (measure of success), the Decadal Plan for Semiconductors has similarly outlined what, when, and the measure of success by identifying seismic shifts that must be addressed and setting metrics for that success. As dimensional scaling that has driven Moore's Law of economics has continued to slow, the collective industry, academia and government ecosystem has yet to identify a silver bullet. Of course, there are some promising paths to explore more deeply and some of those are outlined in the final report that will be published later this month. But, as with Kennedy's speech it is not the intent of the committee to prescribe how to meet the goals but rather identify the gaps, opportunities, and impact of achieving them.

(2)

To maintain global semiconductor industry leadership and ensure America wins the worldwide race to develop and implement the technologies of the future, the U.S. needs a highly skilled workforce. Leadership in semiconductor research, design, and manufacturing requires access to the best and brightest scientists and engineers from around the world, as well as skilled technicians and other occupations requiring STEM proficiency. In the global race for talent, the U.S. educational system is failing to produce a sufficient number of American workers and students with the necessary STEM expertise to meet the needs of the semiconductor industry and other technology fields.

The STEM challenge and filling the pipeline for future engineers was clearly highlighted by all panelists. Other fields are and will leverage and become dependent on semiconductors more so in the future. The areas of med-tech and smart mobility, among others, are included in the applications which will further leverage semiconductor technology - even more than they already are. What is critical, is exposing students early on the system view and all the technologies which enable the solution so they can appreciate the hardware, software, and associated physics to build interest. Salary competition is always an issue but may be augmented by other benefits which can be provided. Many startups have low salaries but high



incentive to succeed via equity, as an example. Perhaps a useful why to think about these "other interesting undertakings," is that these applications provide the co-design Challenge Problems that will drive innovation in ICT technologies. They help define requirements, and the boundaries for the design trade-space. History has shown that part of drawing talent into a field involves articulating the challenges and opportunities in a way that can "capture the imagination!" The Decadal Plan and these discussions is a step in that direction.

**22. What new technologies pose the greatest risk to the semiconductor industry and what is the industry doing to combat or adapt to those risks?**

The greatest risk for the semiconductor industry is not investing in semiconductor research discussed in the webinar. The consequences for the future will be far reaching. Thus, this webinar serves as a first call-to-action to support a path forward to continue to enjoy the benefits in all aspects of lives that Moore's Law has provided. New technologies will, of course, complement existing semiconductor technologies. In fact, the semiconductor industry today invests in several new technologies, for example quantum computing, semiconductor synthetic biology, among others as complementary technologies. For example, quantum techniques in computing, sensing, and communications could be seen as "disrupting" the semiconductor industry, but semiconductor advances are actually critical enabling technologies for the emerging quantum machines.

**23. What technology is the greatest risk to the semiconductor industry and what is the industry doing to combat/evolve to face this risk?**

The greatest risk is not investing in semiconductor research for the future. New technologies will complement existing semiconductor technologies and, in fact, may provide new opportunities for the semiconductor industry to leverage the massive installed and developing manufacturing capability.

**24. I think we all agree on the issues. My question is do we have enough funding in this program - especially compared to other countries - to avoid instrumentalization of the research?**

The Decadal Plan focus is to identify and demonstrate the key challenges with objective intent to infuse significant increase in semiconductor research funding by governmental agencies. Objective is fund larger "moon shot" programs to provide leadership in technology. Victor's slide indicated 3x increase of federal investments in semiconductors and explicitly \$3.4B annually across the 5 seismic shifts. Is it enough?

**25. What new application spaces do you see enabled by these shifts? For example, what new business models might help to justify the investments in system-level security overhead across the ecosystem (design cost, integration/validation cost, lifecycle, etc.)?**

A few application areas were mentioned but medical diagnostics/monitoring, industrial automation/monitoring/action, AI for various autonomous elements (robotics, UAV, automobiles), manufacturing optimization etc.

**Thank you for your participation and interest.**

**-SRC and SIA**

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**NOTE: The following questions were considered out of scope:**

- How will the distribution of semiconductor manufacturing sites, foundries & OSATs, geographically play out? Will there be new & more semiconductor manufacturing sites in the United States? Would this mean less for the other regions? And in particular, less for which regions and countries?
- What actions are US companies taking to reduce their supply chain dependence on Greater China?
- What will the direction be under Biden for the semiconductor industry vs. under Trump? Will there be any significant changes in the next term?