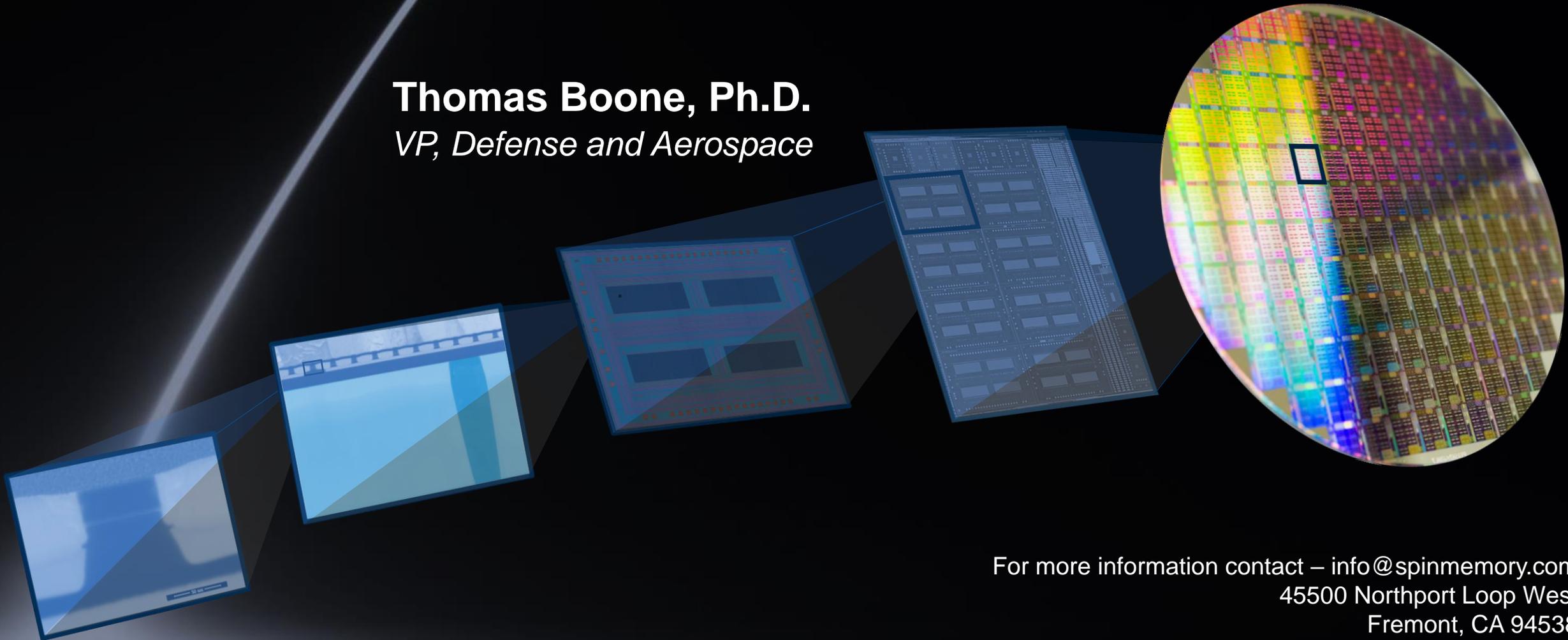


Accelerating MRAM for Strategic Applications

Thomas Boone, Ph.D.
VP, Defense and Aerospace

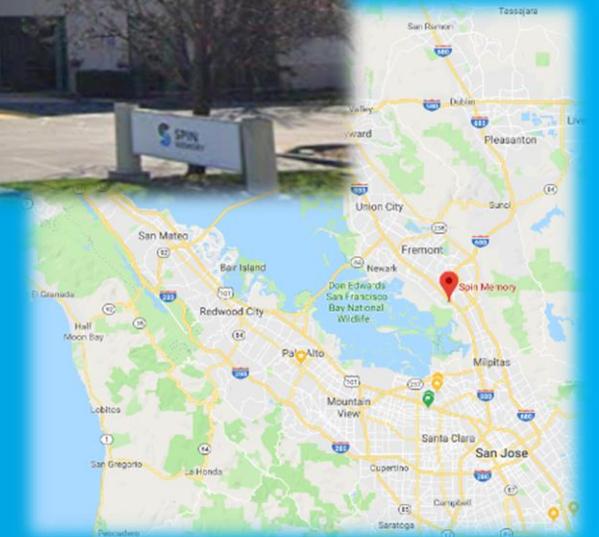
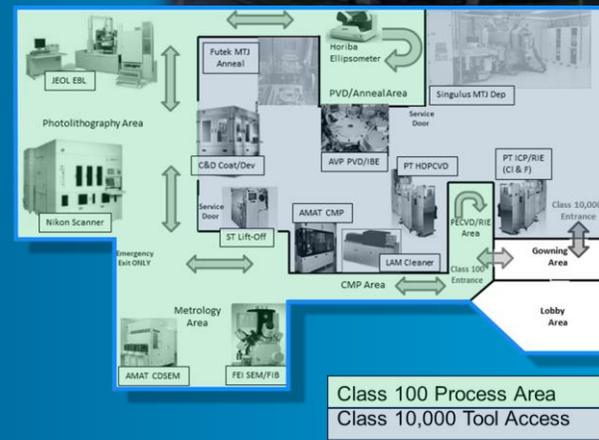


For more information contact – info@spinmemory.com
4550 Northport Loop West
Fremont, CA 94538
(510) 933-8200

Spin Memory Corporate Overview

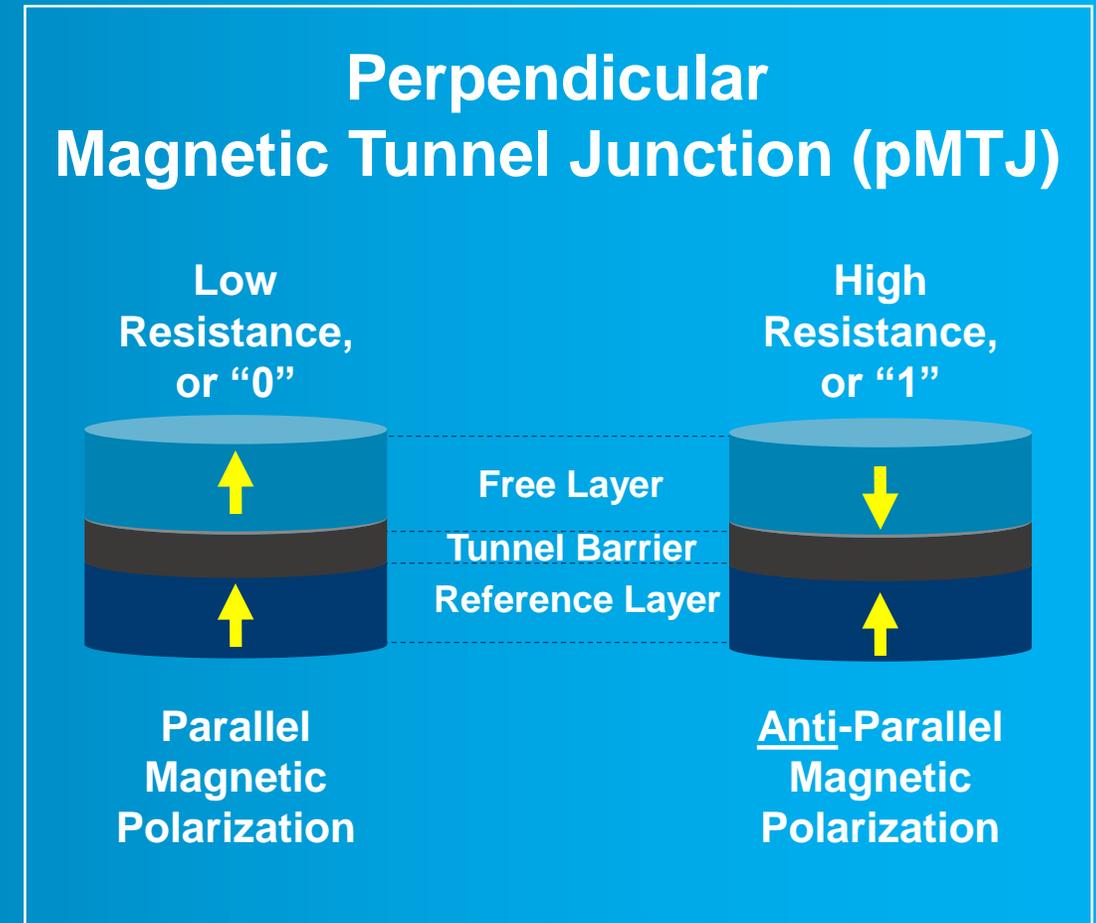
- US company located in Fremont, CA developing perpendicular spin transfer torque magnetic random access memory (pSTT-MRAM).
- Developing technology to provide embedded NVM, SRAM and ultimately DRAM
- Company owns a class 100 cleanroom “back-end” manufacturing facility
- World Class Team of US Citizen and US Persons including 10 PhD’s
- Currently developing radiation hardened memory solutions to support U.S. Military and Space applications
STT-MRAM is inherently rad-hard!

Spin Memory- Fremont, CA



What is STT-MRAM? A Class of Computer Memory.

- MRAM is Magneto-resistive RAM
 - Magnetic polarization sets '1', '0'
- STT is Spin Transfer Torque
 - Electron spin sets Free Layer polarization
 - ST-MRAM using pMTJ is latest MRAM generation
- Bitcell uses 1 transistor + 1 MTJ
 - Very dense configuration
- Attributes:
 - Non-volatile
 - High-speed read and write
 - High endurance
 - Easy integration in BEOL – no impact on FEOL



Spin Memory's Defense and Aerospace Value Proposition

NEED: US Government and DoD requires advanced Rad-Hard microelectronics memory for strategic and space applications.

APPROACH: STT-MRAM is intrinsically Radiation immune. Space Probe and Satellite applications. Targeting Trusted and Assured Foundries.

BENEFITS: Spin Memory's enabling STT-MRAM IP and resources including CONUS 200 mm Factory in Fremont, CA - 100% US Persons.

COMPETITION: Legacy Toggle MRAM, RRAM, FRAM, CRAM. Less upfront cost, but lack in performance of perpendicular STT-MRAM

Space-Based Systems Need a New Memory

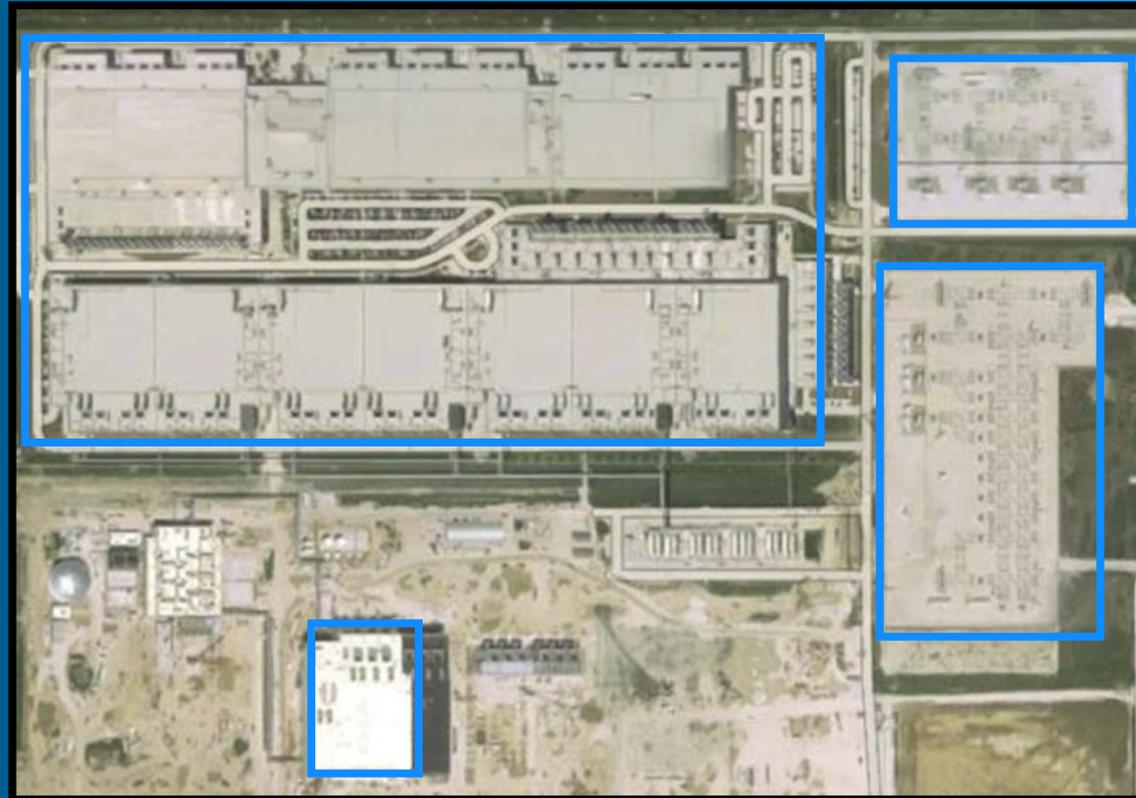
| | SRAM | DRAM | NOR | NAND | ReRAM | MRAM |
|---------------------------|-----------|-----------|-----------|-----------|------------|------------|
| Non-Volatile | No | No | Yes | Yes | Yes | Yes |
| Read/Write Speed | High | High | Slow | Slow | Slow | High |
| Read/Write Power | Low | Low | High | Low | Low | Low |
| Stand-by Power | High | High | Low | Low | Low | Low |
| Cost (Cell Size) | High | Low | Low | Low | Low | Low |
| Endurance | High | High | Low | Low | Low | High |
| Retention | No | No | High | High | High | High |
| Scalable < 16nm | No | No | No | No | Yes | Yes |
| Non-Charge Based | No | No | No | No | Yes | Yes |
| Radiation Tolerant | No | No | No | No | Yes | Yes |

Enormity of Modern Data Centers

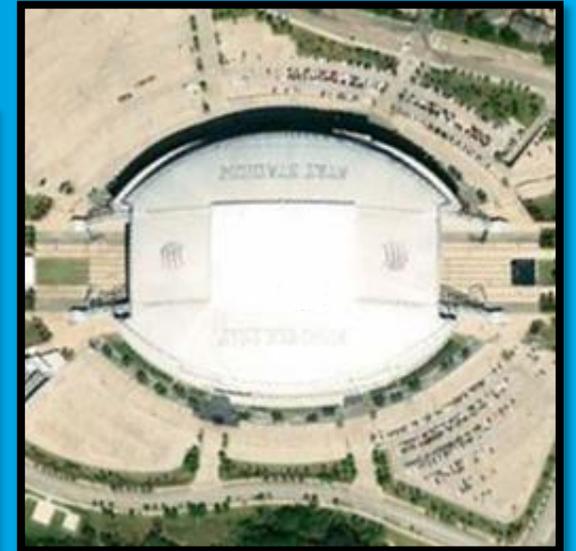
Modern data centers are increasingly becoming the world's largest facilities.
(aerial photos on same approximate scale)



Pentagon – Washington DC



Google Data Center – Council Bluffs, IA



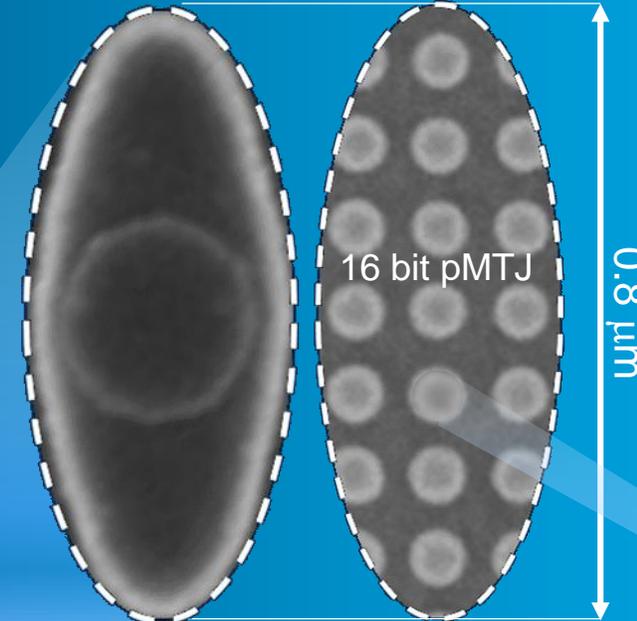
AT&T Stadium – Arlington, TX

Legacy RH Toggle MRAM vs. advanced STT-MRAM

Toggle MRAM

- Toggle is 16-20x larger than pMTJ
- Toggle-MRAM uses simple etch process
- Limited to 130nm+ CMOS Nodes
- Reticle Limited to 16Mb

Top Down View



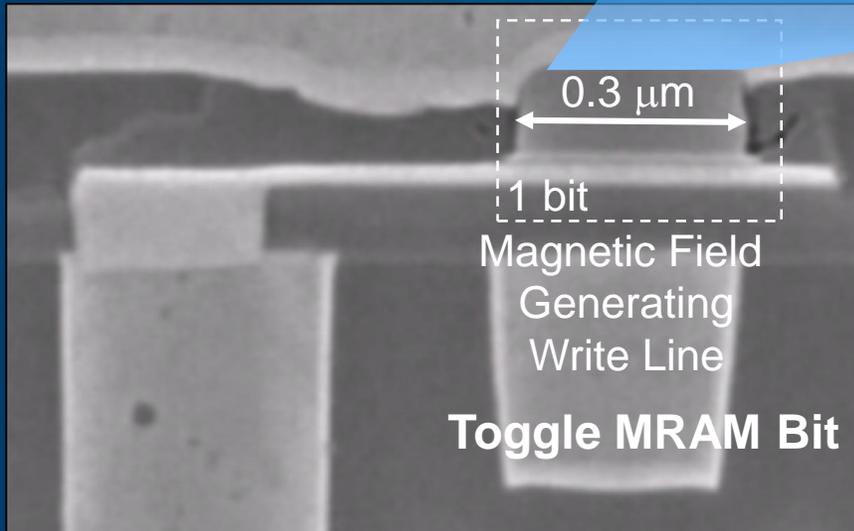
1 Toggle Bit 2 Bytes STT

This side-by-side comparison illustrates that nearly 2 Bytes of STT-MRAM data fits in the same area as 1 bit of Toggle-MRAM

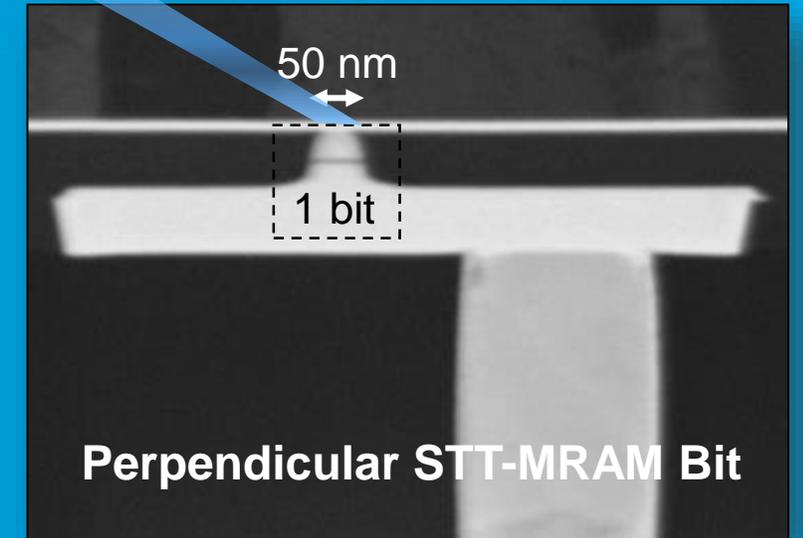
Perpendicular STT-MRAM

- 20x Density of Toggle
- Ion Mill Etch to preserve MgO
- Scales to 3nm CMOS
- Path to 8Gb w/ 1xnm CMOS

Cross-sectional View

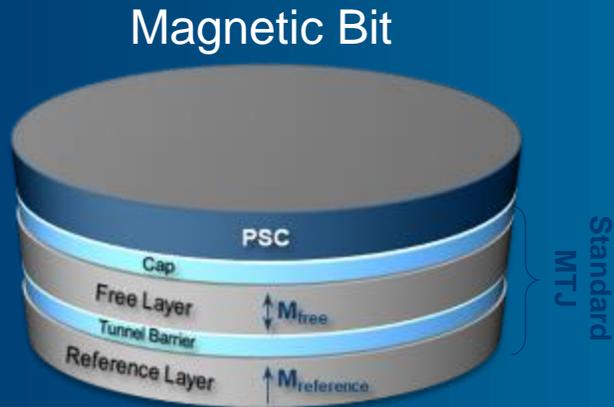


Cross-sectional View



Spin's Patented IP Engineers MRAM to Challenge DRAM/SRAM

Enhanced Retention Time

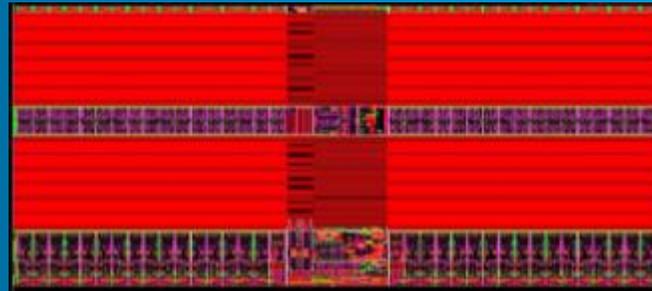


PSC Structure

- Demonstrated increase MRAM Memory retention by 1,000 times
- Enables high-density memory designs
- Technology remains intrinsically rad-hard

Endurance Boost

Engine/Design

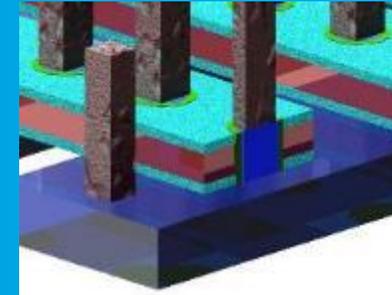


Endurance Engine:

- Demonstrated increases endurance of MRAM 100,000 times.
- Enables 10ns access times
- Corrects hard/soft errors from radiation
- Built-in health monitoring

Density Increase

CMOS Selector Technology



Selector:

- Enables MRAM to compete in cost with DRAM by increasing density.
- Can be used for all emerging memories: FeRAM, ReRAM, etc.
- Eliminates "RowHammer"