Strengthening the Global Semiconductor Supply Chain in an Uncertain Era

Slides for webinar

APRIL 6, 2021
The semiconductor industry ranks high simultaneously in both R&D and capital intensity.

### R&D as % of Revenues, 2019

- Design: 12%
- Manufacturing: 6%
- Rest of value chain: 4%

### Capital Expenditure as % of Revenues, 2019

- Rest of value chain: 2%
  - Design: 3%
  - Manufacturin**: 20%
- Semiconductors: 26%
- Utilities: 25%
- Power generation: 21%
- Broadcasting & Info. Services: 19%
- Trucking: 17%

1. Includes EDA and Core IP, Equipment and Materials
2. Includes Wafer Fabrication and Assembly & Test

Sources: BCG analysis based on Capital IQ data.
The global semiconductor supply chain based on geographic specialization has delivered enormous value for the industry.

**Semiconductor Supply Chain**

- **Precompetitive research**
  - EDA
  - Core IP
- **Design**
  - Logic
  - DAO
  - Memory
- **Manufacturing**
  - Wafer fabrication
  - Assembly, packaging and testing

**Share by region** (\% of worldwide total, 2019)

<table>
<thead>
<tr>
<th>Region</th>
<th>US</th>
<th>China</th>
<th>East Asia</th>
<th>Europe</th>
<th>Other</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDA and core IP</td>
<td>74</td>
<td>3</td>
<td>20</td>
<td>4</td>
<td>34</td>
</tr>
<tr>
<td>Logic</td>
<td>67</td>
<td>8</td>
<td>4</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>DAO</td>
<td>37</td>
<td>4</td>
<td>5</td>
<td>3</td>
<td>19</td>
</tr>
<tr>
<td>Memory</td>
<td>29</td>
<td>6</td>
<td>3</td>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>Equipment</td>
<td>41</td>
<td>3</td>
<td>8</td>
<td>3</td>
<td>18</td>
</tr>
<tr>
<td>Materials</td>
<td>11</td>
<td>3</td>
<td>12</td>
<td>3</td>
<td>57</td>
</tr>
<tr>
<td>Wafer fabrication</td>
<td>12</td>
<td>4</td>
<td>9</td>
<td>6</td>
<td>56</td>
</tr>
<tr>
<td>OSAT</td>
<td>38</td>
<td>13</td>
<td>4</td>
<td>6</td>
<td>43</td>
</tr>
</tbody>
</table>

**Source:** BCG analysis

Note: DAO = discrete, analog, and other (including optoelectronics and sensors); EDA = electronic design automation; OSAT = outsourced assembly and test

1. For EDA and core IP, design, manufacturing equipment and raw materials the regional breakdown is based on company revenues and company headquarters location. For wafer fabrication and OSAT is based on installed capacity and geographic location of the facilities
2. Mainland China
3. East Asia includes South Korea, Japan, and Taiwan

**Costs savings vs. fully localized "self-sufficient" supply chains:**

- **$0.9-1.2T** avoided upfront investment
- **$45-125B** annual cost efficiencies
- **35-65%** enabled reduction in semiconductor prices
## Five key vulnerabilities identified in the semiconductor supply chain

<table>
<thead>
<tr>
<th>Risk factor</th>
<th>Description</th>
<th>Current examples</th>
<th>FOCUS</th>
<th>AREA IN REPORT</th>
</tr>
</thead>
<tbody>
<tr>
<td>High geographic concentration of some activities</td>
<td>Single points of failure which may be disrupted by natural disasters, infrastructure failures, cyberattacks or geopolitical frictions</td>
<td>• Wafer fabrication • Assembly, packaging &amp; testing • Some specialty materials</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Geopolitical frictions</td>
<td>Broad export controls over inputs or technologies with no viable alternative suppliers in other countries</td>
<td>• US-China frictions • Japan - S. Korea frictions</td>
<td></td>
<td></td>
</tr>
<tr>
<td>National self-sufficiency policies</td>
<td>National industrial policies that seek broad import substitution or broadly discriminate against foreign suppliers, leading to distortion in global competition and risk of overcapacity</td>
<td>• China policies in pursuit of “self sufficiency” across the semiconductor value chain</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Talent constraints</td>
<td>Current growth in talent pool of Science &amp; Engineering graduates is insufficient to meet the industry demand for technical talent</td>
<td>• All countries, but US in particular given leadership in R&amp;D intensive activities and reliance on attracting &amp; retaining global talent</td>
<td></td>
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</tr>
<tr>
<td>Stagnation in funding of basic research</td>
<td>Government programs and funding play a critical role in basic research, which is essential for the semiconductor industry</td>
<td>• US government-funded R&amp;D in semiconductors has stagnated and is below overall level across all sectors</td>
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</tbody>
</table>
50+ points of high geographical concentration across the supply chain (but not all with the same level of associated risk)

Value chain activities where one single region accounts for ~65% or more of global share

<table>
<thead>
<tr>
<th>Design</th>
<th>Front End</th>
<th>Manufacturing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced processors (CPU, GPU, FPGA), and DSP</td>
<td>Logic: leading nodes (&lt; 10nm)</td>
<td>Outsourced Assembly and Test (OSAT)</td>
</tr>
<tr>
<td>RFFE and cellular basebands</td>
<td>Logic: mature nodes (&gt;= 10nm)</td>
<td></td>
</tr>
<tr>
<td>Data converter, switches, multiplexers and other analog</td>
<td>Memory</td>
<td></td>
</tr>
</tbody>
</table>

EDA & Core IP

23 equipment types, i.e. doping, process control
12 equipment types, i.e. photomask processing
3 equipment types, i.e. EUV lithography

Equipment & Tools

Select examples (not exhaustive):
- Photore sist, photomask
- Silicon wafers
- Packaging substrates
- Specialty gases (in aggregate)

Materials

Select examples (not exhaustive):
- Photore sist, photomask
- Silicon wafers
- Packaging substrates
- Specialty gases (in aggregate)

Sources: BCG analysis with data from Gartner, SEMI, UBS; SPEEDA
East Asia + China concentrate ~75% of the wafer fabrication capacity; in particular, ~90% of advanced logic capacity <10 nm is located in Taiwan

### Breakdown of the Global Wafer Fabrication Capacity by Region, 2019 (%)

<table>
<thead>
<tr>
<th>Region</th>
<th>Logic</th>
<th>Memory</th>
<th>% of Global Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt; 10 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10-22 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>28-45 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>&gt; 45 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DAO¹</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Total</td>
<td></td>
<td></td>
</tr>
<tr>
<td>US</td>
<td>US</td>
<td>12%</td>
<td>33%</td>
</tr>
<tr>
<td>China</td>
<td>China</td>
<td>16%</td>
<td>2%</td>
</tr>
<tr>
<td>Taiwan</td>
<td>Taiwan</td>
<td>20%</td>
<td>8%</td>
</tr>
<tr>
<td>S. Korea</td>
<td>S. Korea</td>
<td>19%</td>
<td>9%</td>
</tr>
<tr>
<td>Japan</td>
<td>Japan</td>
<td>17%</td>
<td>22%</td>
</tr>
<tr>
<td>Europe Other²</td>
<td>Europe Other²</td>
<td>8%</td>
<td>7%</td>
</tr>
</tbody>
</table>

1. Discrete, analog and optoelectronics and sensors  2. Other includes Israel, Singapore and the rest of the world

Sources: BCG analysis with data from SEMI fab database
Enhancing the supply chain resilience through a focused approach: example of US minimum viable capacity for advanced logic (< 10nm)

**Breakdown of Total US Semiconductor Consumption, 2019**

- **Memory**: 28% (25% of global semiconductor sales $107B)
- **Advanced logic**: 34%
- **DAO**: 15%
- **Other logic**: 23%

$107B includes 25% of global semiconductor sales.

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- **Advanced logic**: 34%
- **Other logic**: 23%
- **DAO**: 15%

**1. Considering only leading node capacity (< 10nm)**

**2. Total Cost of Ownership** - includes capex and 10 years of opex, before government incentives.

**3. Includes both existing local/state incentives and potential new federal incentives**

Sources: BCG analysis

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**Total US Advanced Logic Consumption**: 34%

- **Other Infra**: 24%
- **Critical Infrastructure**: 9% (980 + 420)

- **Total US Consumption**: 10-year investment in new fabs for onshore coverage in 2030 ($B)
  - **Private sector + Government incentives**: 980 + 420
  - 60-65 new fabs
  - 6-7 new fabs

**45 + 18** includes 2-3 new fabs of 20-35 kwpm.

Includes:
- Defense & Aerospace
- Telecom networks
- Energy, security and medical equipment
- Data centers of Government and essential sectors (telecoms, energy & utilities, healthcare and financial services)

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1. Considering only leading node capacity (< 10nm)  
2. Total Cost of Ownership - includes capex and 10 years of opex, before government incentives  
3. Includes both existing local/state incentives and potential new federal incentives
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