



Semiconductor  
Research  
Corporation

# **Future Analog Electronics and Intelligent Sensing SIA Webinar**

## **SIA-SRC Decadal Plan for Semiconductors**



**Fundamental breakthroughs in analog hardware are required to generate smarter world-machine interfaces that can sense, perceive and reason.**



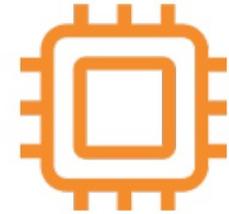
The growth of memory demands will outstrip global silicon supply presenting opportunities for **radically new memory and storage** solutions.



Always available communication requires new research directions that address the **imbalance of communication capacity vs. data generation rates.**



Breakthroughs in hardware research are needed to address **emerging security challenges** in highly interconnected systems and AI.

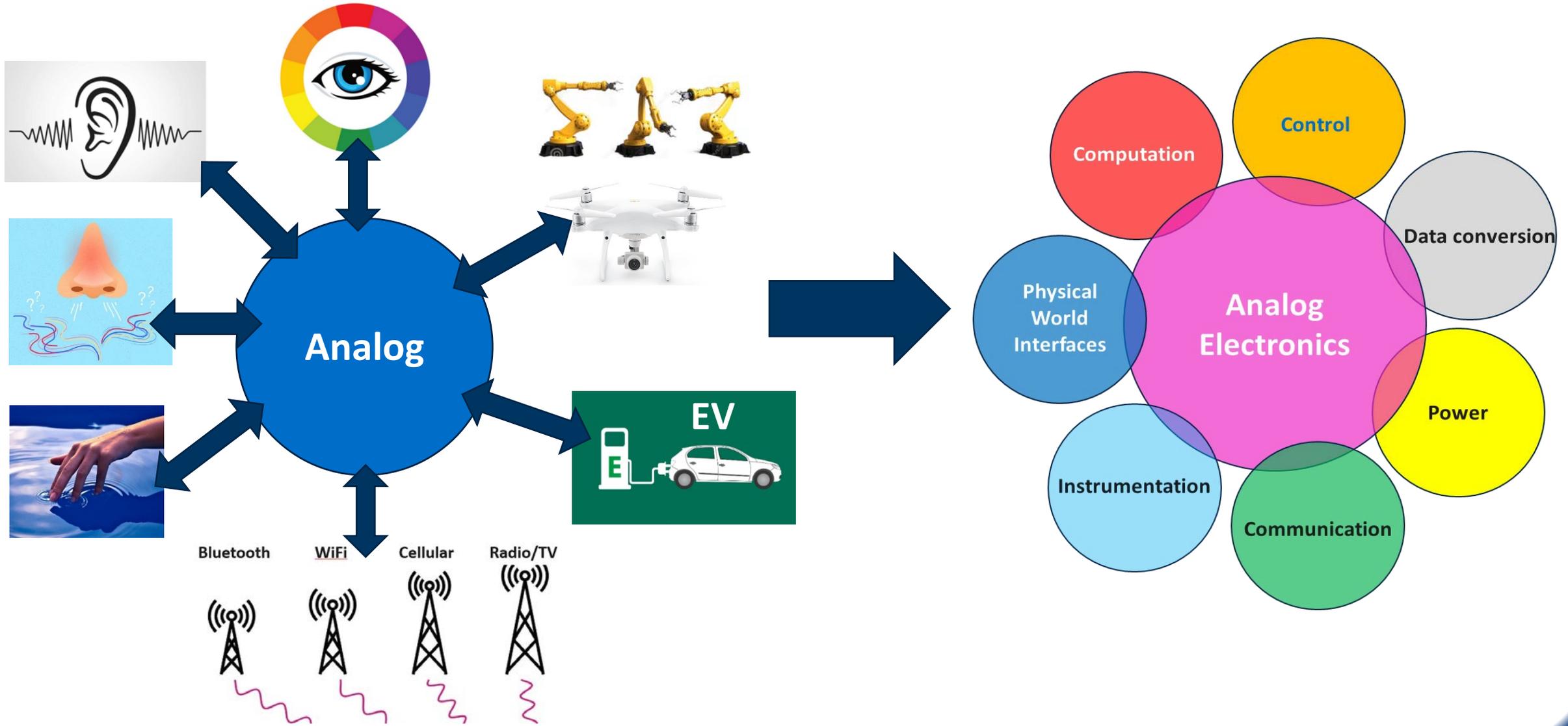


Ever rising energy demands for computing vs. global energy production is creating new risk, and new computing paradigms offer opportunities with **dramatically improved energy efficiency.**

**Full Report Serves As A Guide Towards 2030 and Beyond**



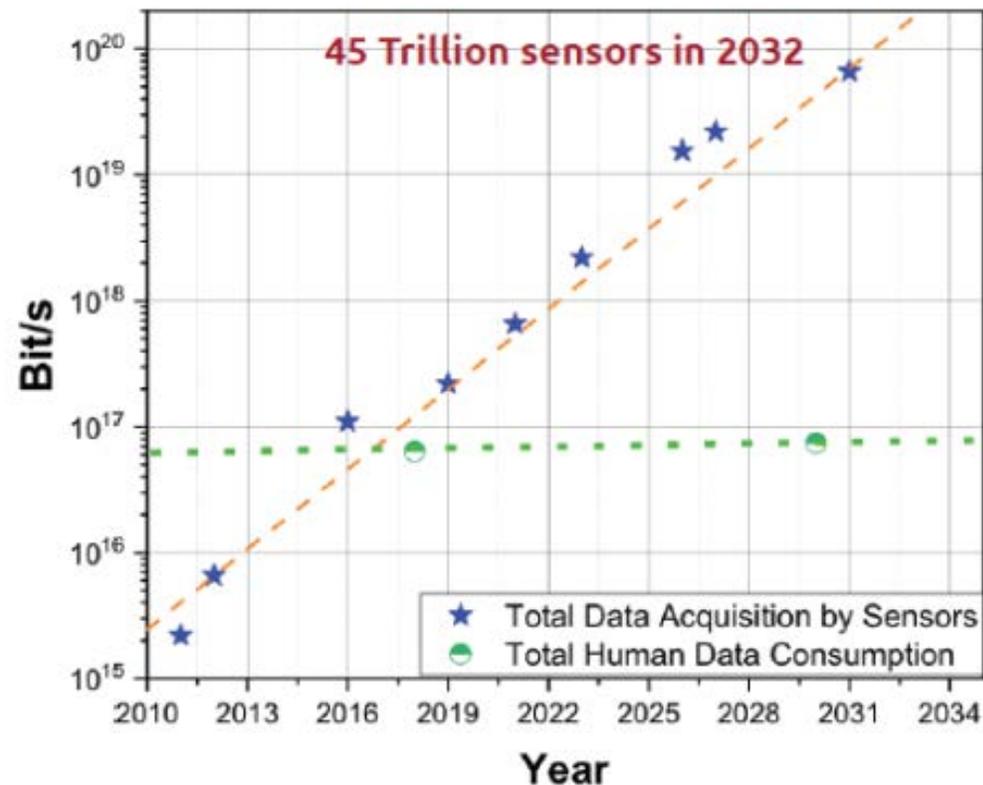
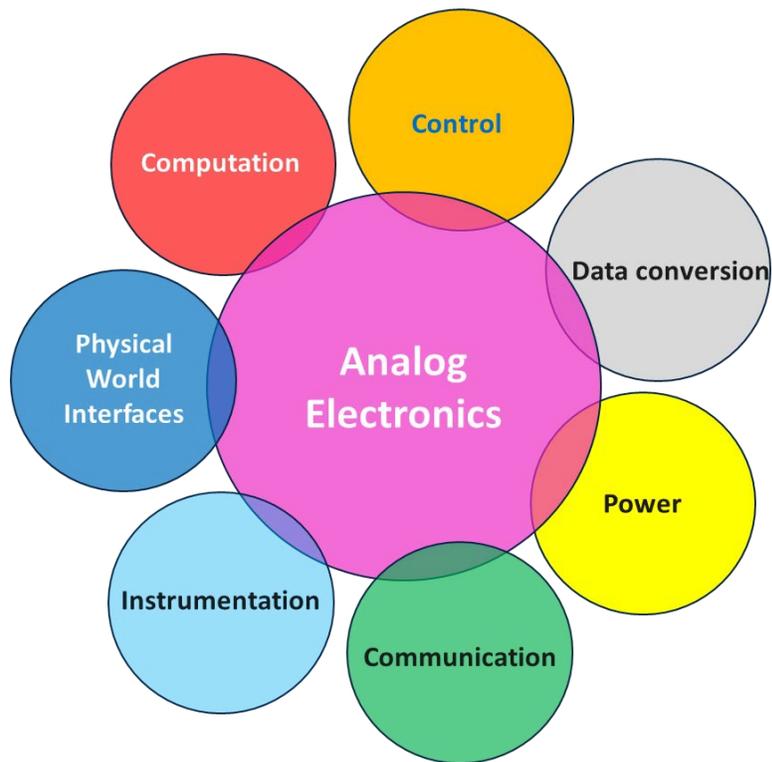
# Analog is the Interface to the Real World





# Analog and Data Deluge – Seismic Shift #1

*Effectively leveraging massive analog data*



**Analog Grand Goal** is for revolutionary technologies to increase actionable information with less energy, enabling efficient and timely (low latency) sensing-to-analog-to-information with a practical reduction ratio of **100,000:1**

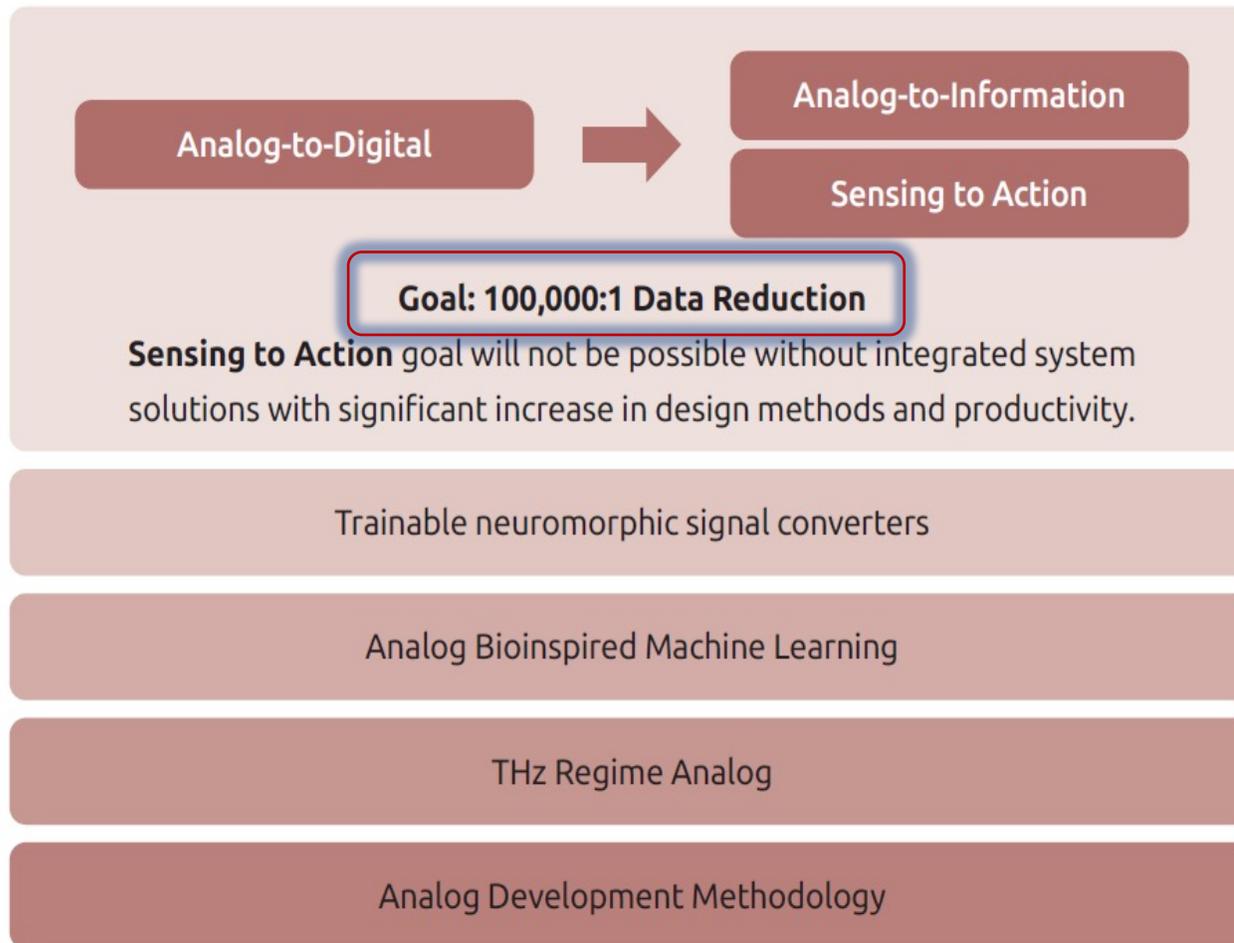


# New Trajectories for Analog Electronics

## *“Interface to the Real World”*

- **Sensing & Processing**
- **Energy Efficient Functions**
  - Communications
  - Computing/Processing
  - Power Conversion & Management
- **Bio-Inspired Model**
- **Holistic Co-Design**

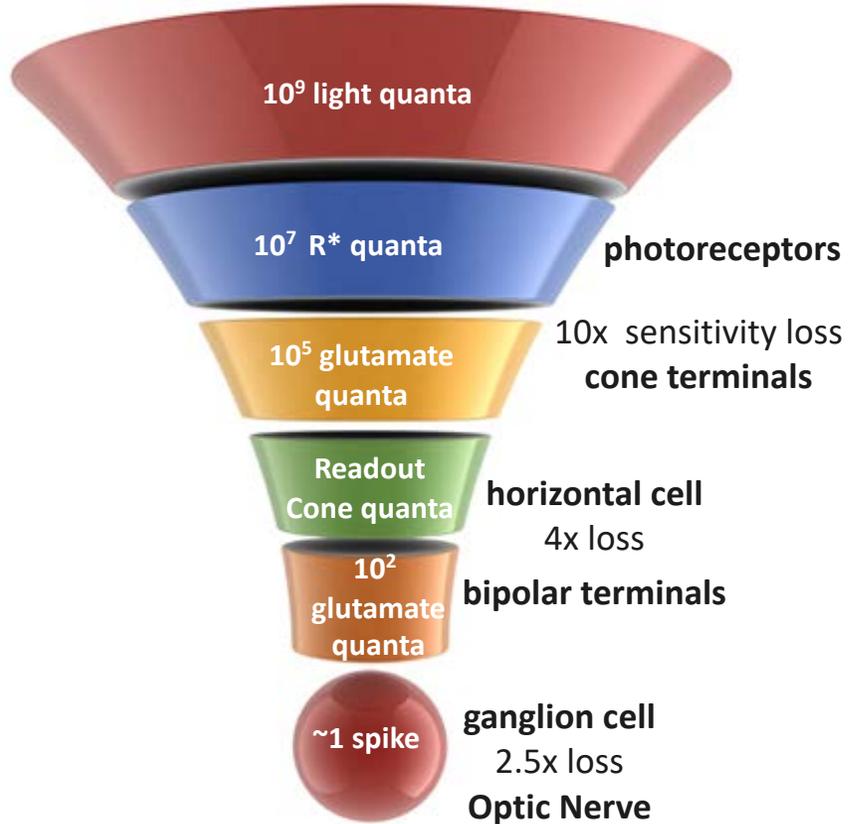
## Research Themes/Opportunities



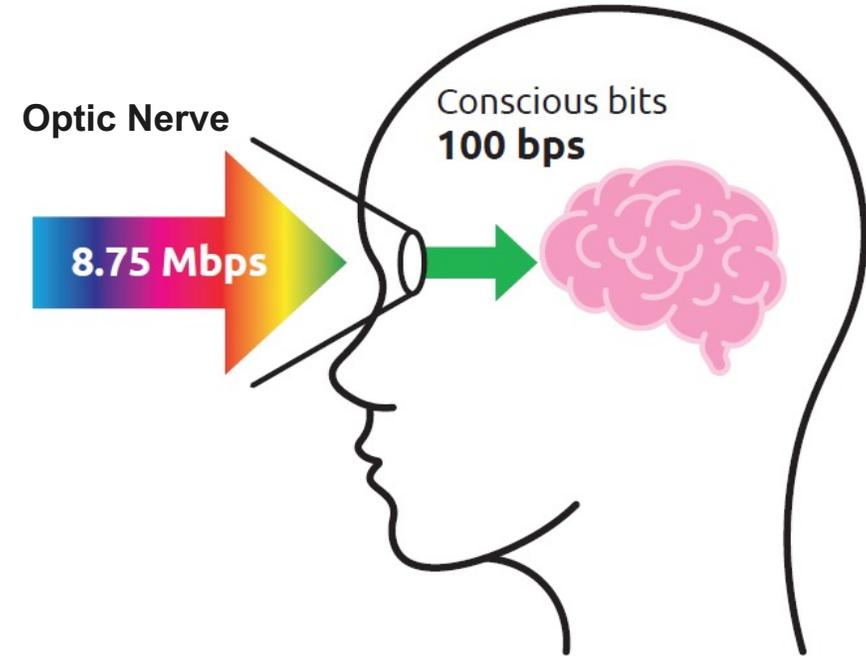
# Bio-Stimulus Domain Reduction

## *Holistic View and Inspiration*

### Eye/Retina Reduction "sensor"



### Processing Reduction



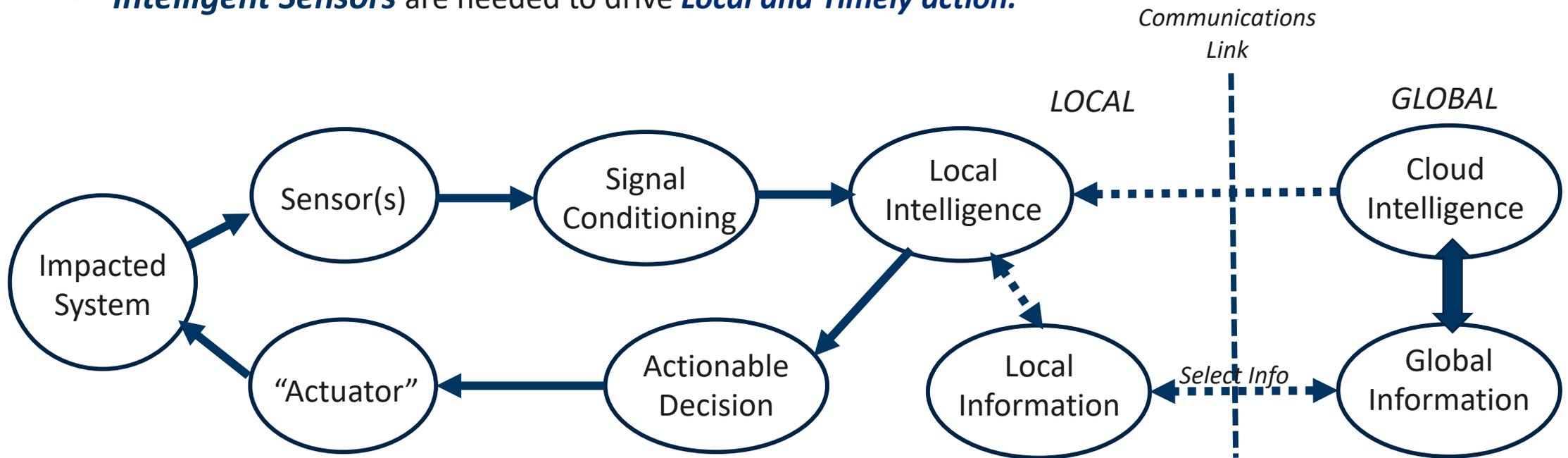
Sensory System	Bits per second	Processed by the brain (bits/s)
Eyes	10,000,000	40
Ears	100,000	5
Smell	100,000	1
Taste	1,000	1

Ref. "Principles of Neural Design"; Sterling and Laughlin

Figure A2: Human sensory system of data acquisition via sensors

# Sensing System Approach - hierarchical

- Trillions” of sensors generate redundant and unused “data.”
- Cloud is not the answer.
  - Communication is a bottleneck and requires significant energy
  - Power to process redundant data is not efficient
  - Latency is too long for local control and action
- **Intelligent Sensors** are needed to drive **Local and Timely action.**





# Required Research – *Largest Need and Impact*

- Study of holistic solutions - with key applications knowledge and focus on minimal processing to take action
  - Collaborative multi-expertise research projects demonstrator platform(s)
  - Effective and Efficient design methods
- Heterogeneous integration - to make best use of best technology in an energy, size, and cost efficient manner
  - CMOS platform integration – optimized technologies
  - Package platform integration – multi-technology/multi-die from DC to THz
- Optimum power management – control and conversion for efficient and fast energy response and management
- Leverage human systems - as a model for bioinspired, local “sensing to action” including efficient machine learning and inference at the edge
  - Analog-based ML architectures (compute in memory, synapse, etc.)
  - Architectures and algorithms that leverage analog approach and compensate or take advantage of analog non-idealities
- Flexible, scalable, secure **platform** and technology - including sensors, memory, and signal representation matched to domain



# Roundtable Discussion

**Moderator:** Dave Robertson

Senior Technology Director / Analog Devices



## Introduction:

- **Jim Wieser**

Director of University Research and Technology / Texas Instruments



## Roundtable:

- **Steven Spurgeon**

Staff Scientist, Energy and Environment Directorate / Pacific Northwest National Laboratory



- **Mark Rodwell**

Doluca Family Endowed Chair in Electrical & Computer Engineering / UC Santa Barbara



- **Kostas Doris**

Fellow / NXP Semiconductors  
Professor / TU of Eindhoven



- **Wai Lee**

Chief Technologist, Sensing Business / Texas Instruments



- **Boris Murmann**

Professor of Electrical Engineering / Stanford University



# SIA – SRC Roundtable New Trajectories for Analog Electronics

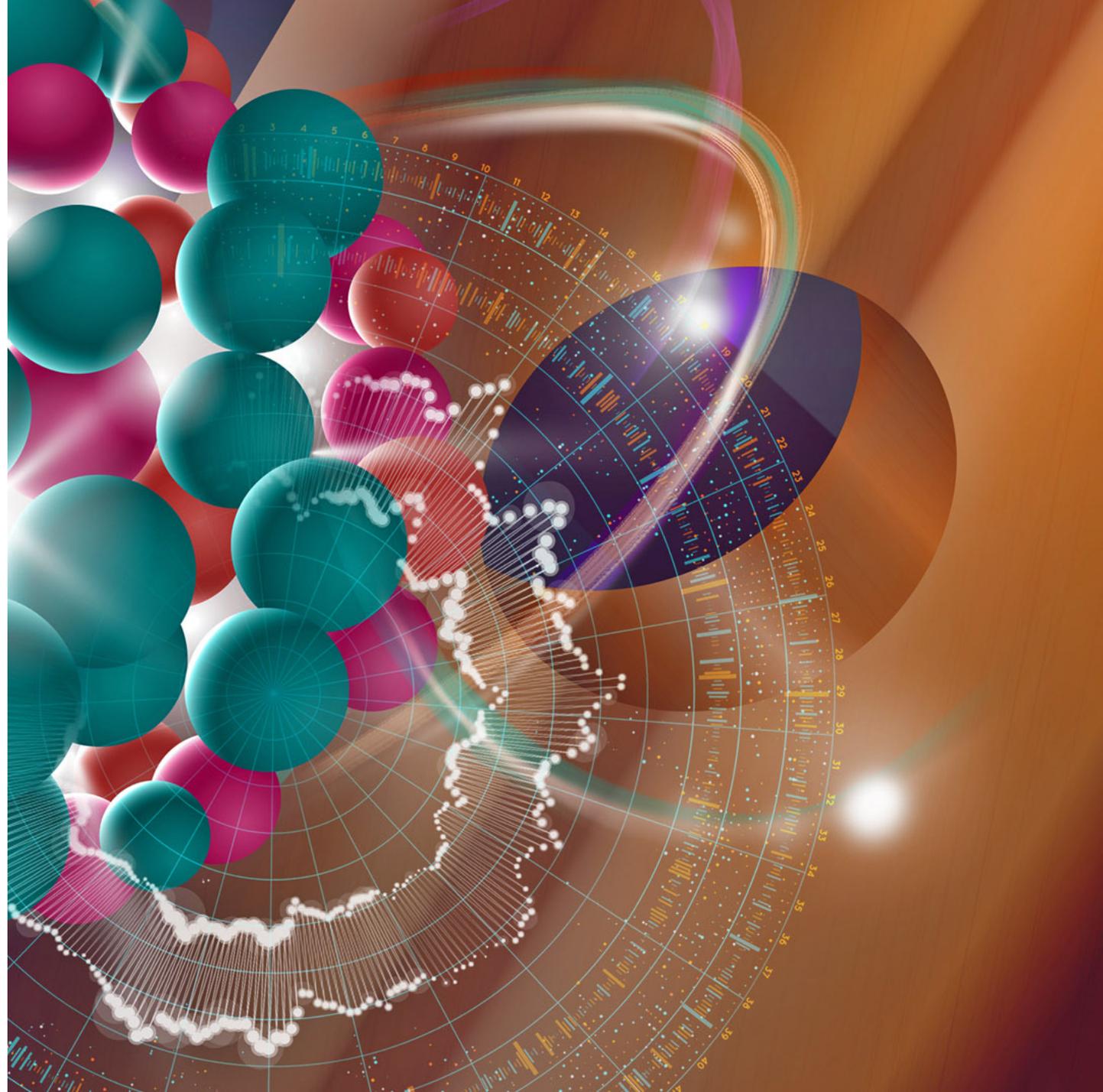
June 10, 2021

**Steven R. Spurgeon**

Energy and Environment Directorate  
Pacific Northwest National Laboratory



PNNL is operated by Battelle for the U.S. Department of Energy



# Advanced instrumentation is a catalyst for national scientific innovation and discovery.



**FY 2019  
27 user facilities**

**Multi-omics** (connected to Summit@OLCF, ALCF, NERSC, ESnet)

**Theory & Simulation** (connected to ESnet, HFIR)

**Climate Science** (connected to EMSL, ARM, JGI, SNS, SSRL)

**Neutron Scattering** (connected to SNS, SSRL)

**Light Sources** (connected to APS, LCLS, NSLS-II, SSRL)

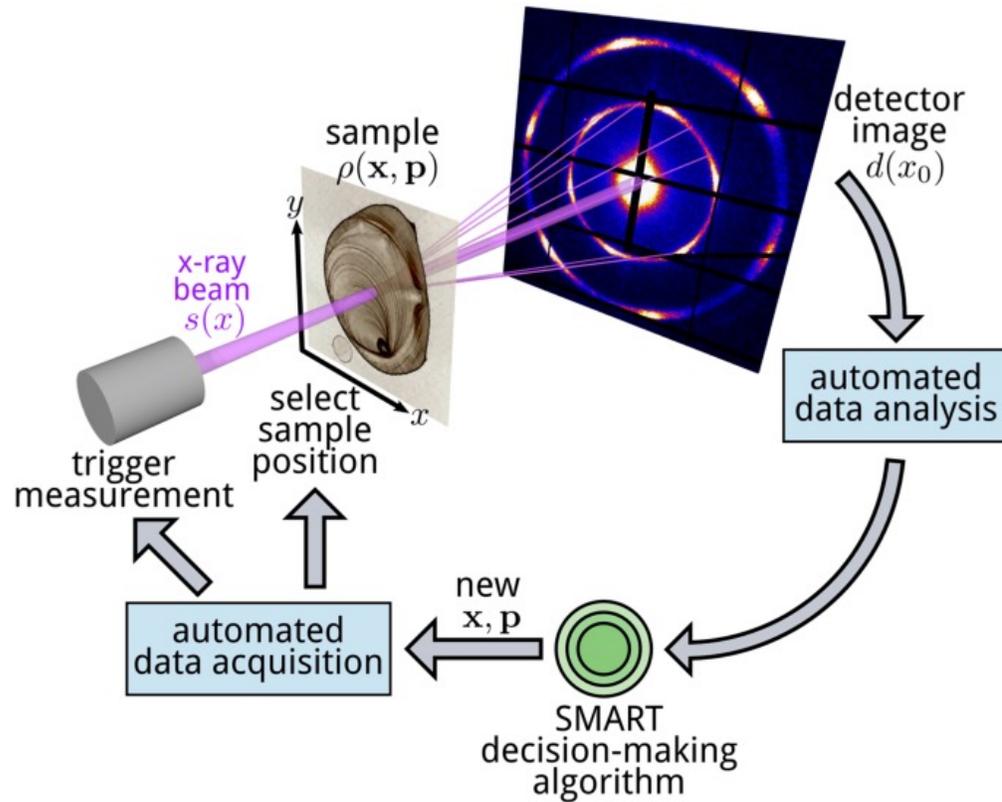
**Cosmology** (connected to RHIC)

**Electron Microscopy** (connected to FACET, ATF, Fermilab AC)

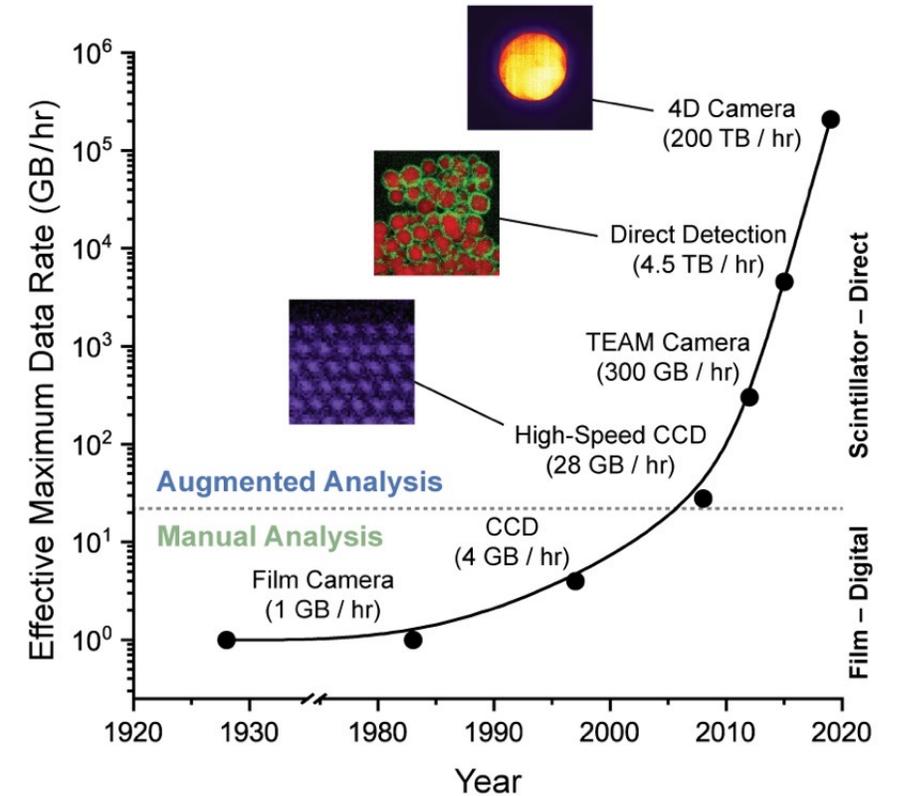
**DEPARTMENT OF ENERGY  
Office of Science**

# We must develop new ways to quickly interpret and act on high bandwidth, heterogeneous data.

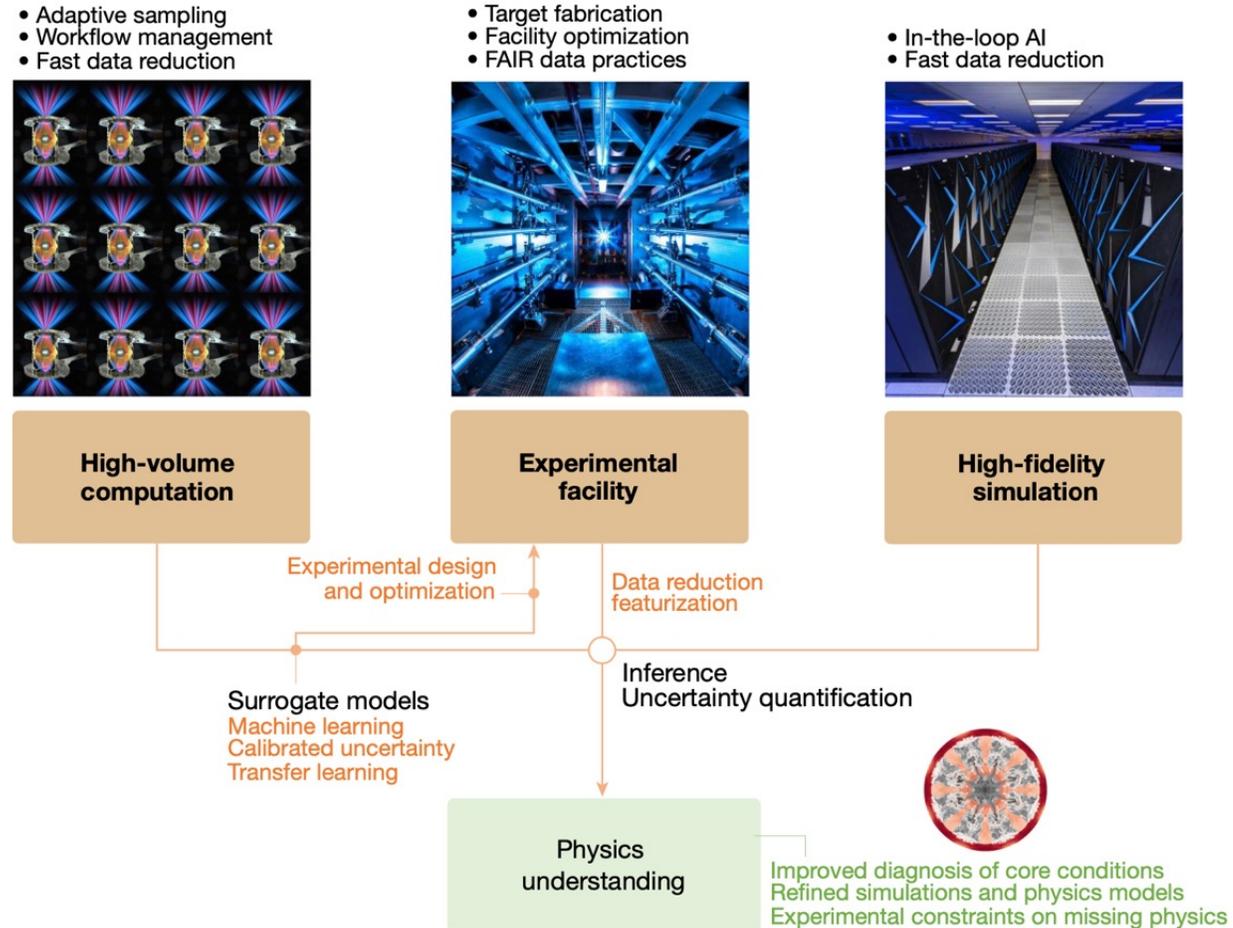
## X-ray Scattering



## Electron Microscopy

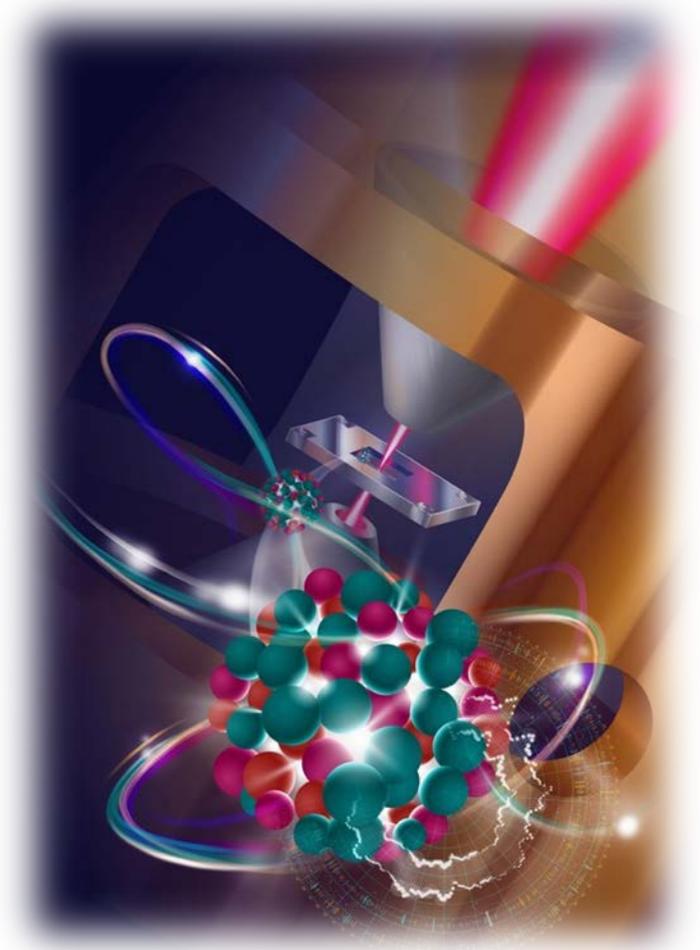


# Domain-grounded reduction and inference are needed to unlock the full potential of sensors.



## Challenges and opportunities

- How can embedded domain knowledge aid in the sensing-to-action workflow?
  - Physically meaningful reduction and inference
  - Expanding intelligence to all system components
- How do we effectively harness multi-modal analog data streams?
  - Efficiency gains from data fusion/redundancy
  - Identification of unique processing solutions
- What does codesign look like in specific analytic contexts?
  - Universal vs. domain-specific designs
  - Determination of bottlenecks in data flow and decision-making process



*SIA/SRC Webinar - Decadal Plan for Semiconductors: New Trajectories for Analog Electronics  
June 10, 2021*

# Transistors for Wireless

***Mark Rodwell***

***University of California, Santa Barbara***

***[rodwell@ece.ucsb.edu](mailto:rodwell@ece.ucsb.edu)***

# 5G/6G Wireless: Terabit Aggregate Capacities

Wireless networks: exploding demand.

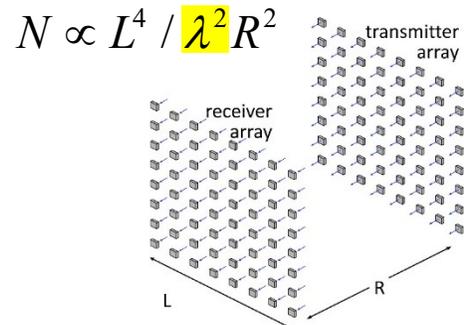
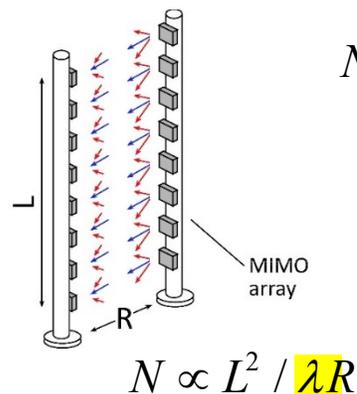
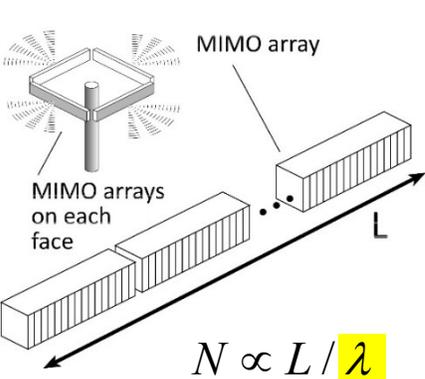
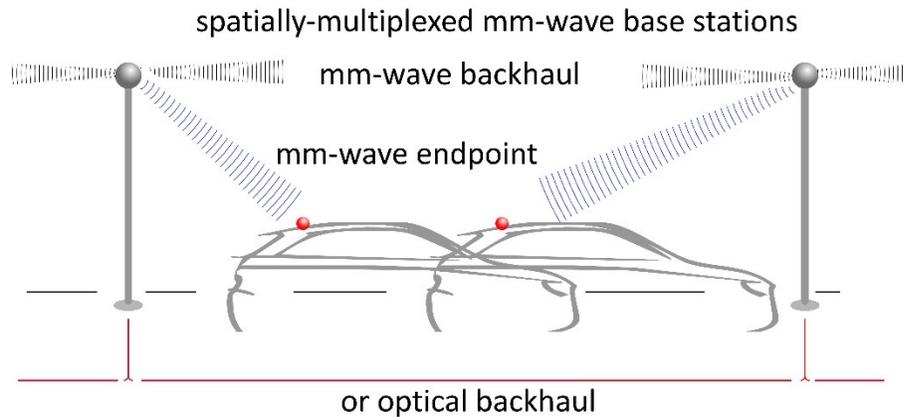
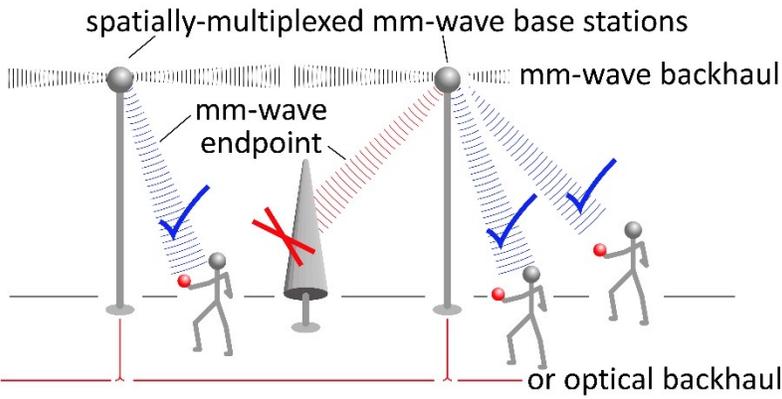
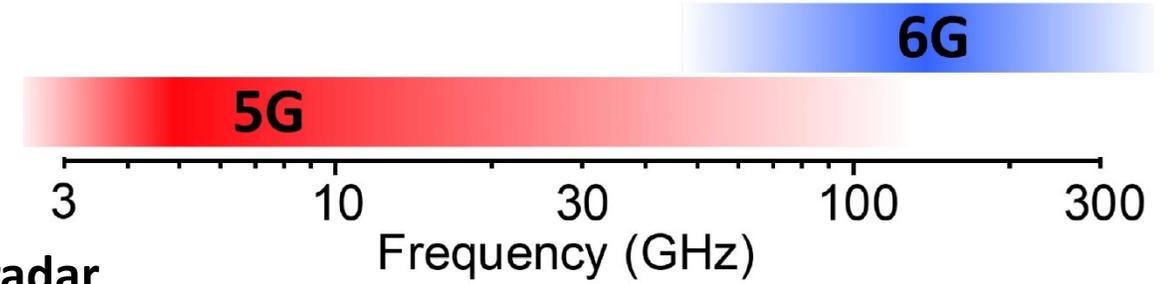
High frequencies → plentiful spectrum → high capacity

Short wavelengths → many beams → massive capacity

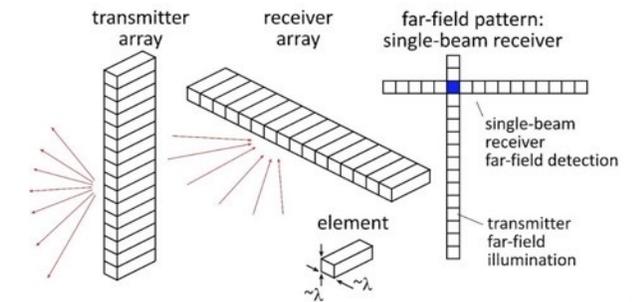
**30-300GHz** carriers, **massive** spatial multiplexing

→ **Terabit** hubs and backhaul links, **near-video-resolution** radar

**Plus: 5-meter Gigabit bluetooth** for many small gadgets.



$$\Delta\theta \propto \lambda / L$$



# CMOS alone won't do it

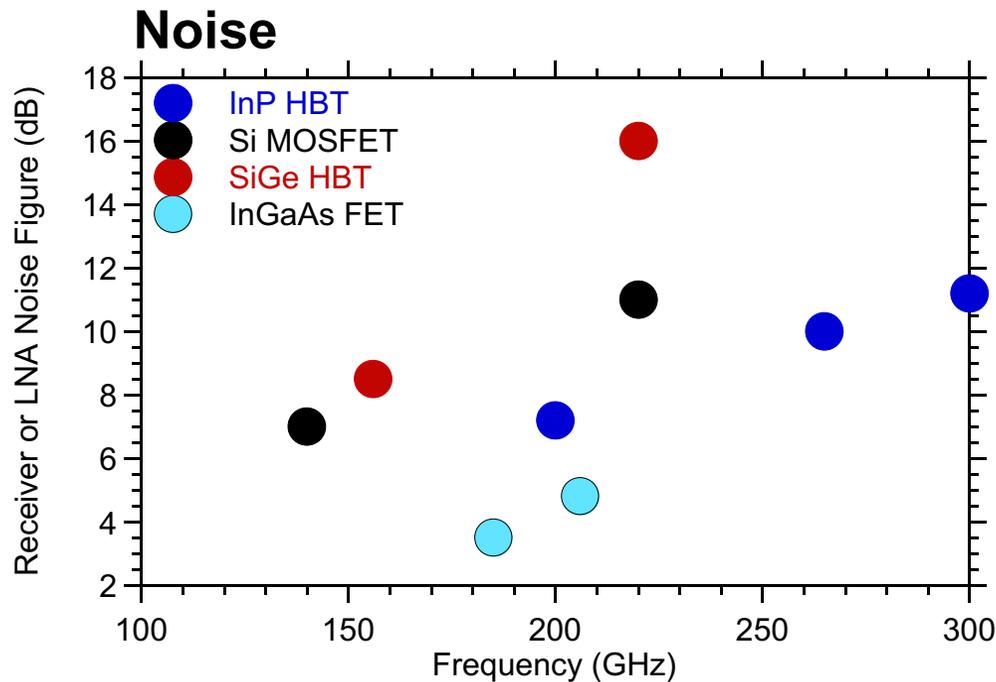
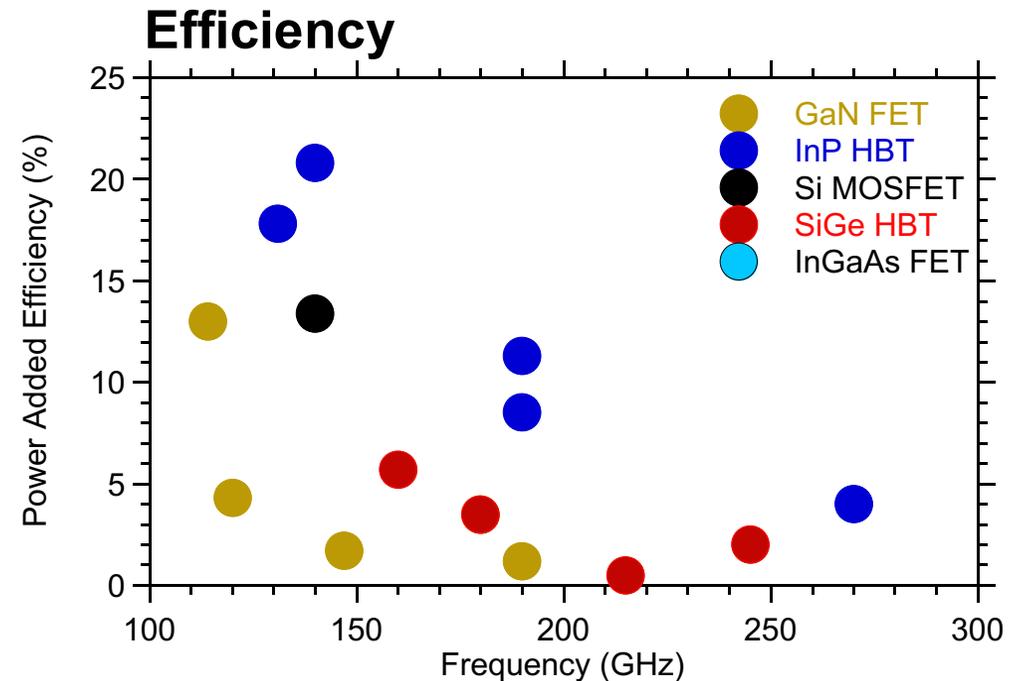
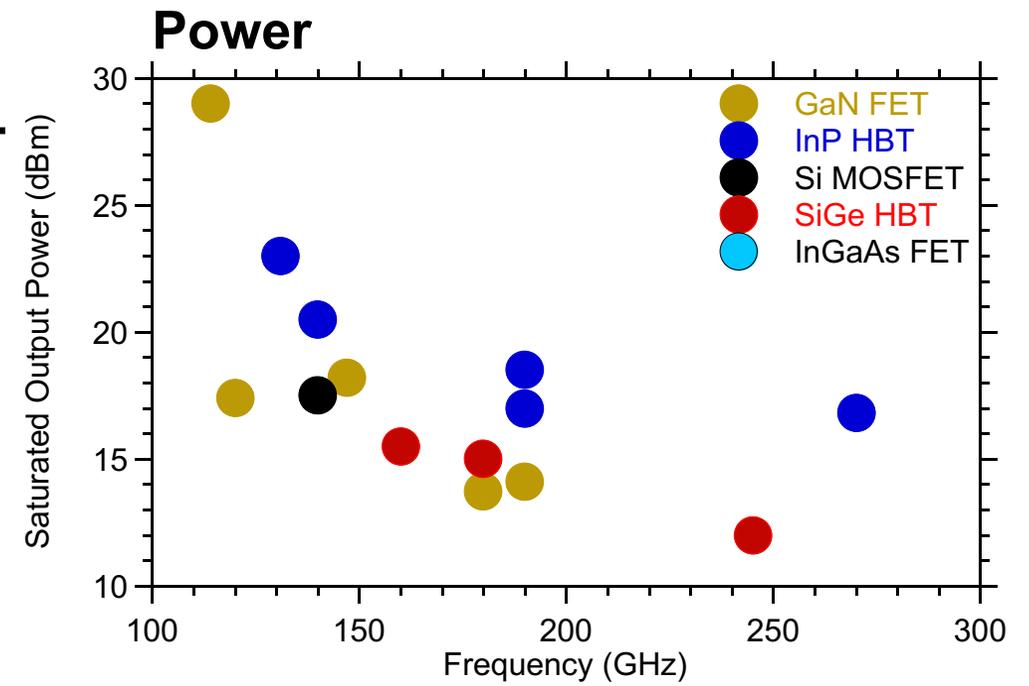
Wireless needs: low **noise**, high **power** & **efficiency**.

VLSI CMOS: compromised on all 3.

Dennard's scaling laws are broken.

CMOS: optimized for VLSI, not **wireless & analog**.

CMOS: needs help to cover moderate distances.



# What wireless needs

---

Need technology mix: CMOS + (InP, SiGe, GaN)

## Cheap but High Performance

Receiver noise: 3dB less noise saves 2:1 transmitter power.

Efficient transmitters : 30% is bare minimum

Powerful transmitters: (0.1W arrays, 1W single beam)

Not just better transistors: interconnects matter

Cost: What is cheap today? **What could be made cheap if we tried ?**

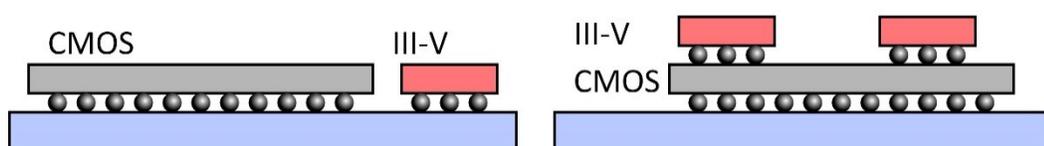
## Needed: **Application-specific wireless IC technologies**

high-volume, low-cost InP HBT, InP HEMT, near-THz SiGe,  
wireless-optimized CMOS (e.g. GF 45nm SOI, Intel 22FFL)

## Needed: **heterogeneous integration (very dense packaging)**

CMOS plus (SiGe, III-V **chipllets**).

integration density, heat, production III-V.



# HETEROGENEOUS AND CO- FUNCTIONAL INTEGRATION NEEDS, OPPORTUNITIES, CHALLENGES

SRC Analog Trajectories

Kostas Doris

JUNE 2021



SECURE CONNECTIONS  
FOR A SMARTER WORLD

EXTERNAL

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## PRELIMINARY NOTE

- Precision and reliable sensing needed in many emerging applications
  - Robotic/industrial, agriculture, drone, safety, medical, 6G Telecom
- This talk focusses on sensing for Automotive without loss of generality

### **A few messages to take away from this talk**

- 1. We need sensors that generate more information not more data. This means smaller wavelengths and more functionality in the sensor are needed.**
- 2. In-package integration is the new cauldron of integration like CMOS technology was in the past.**
- 3. Many heterogeneous technologies and functions must be conditioned optimally together to the perception function.**

# AUTONOMOUS DRIVING NEEDS MULTIPLE SENSOR MODALITIES

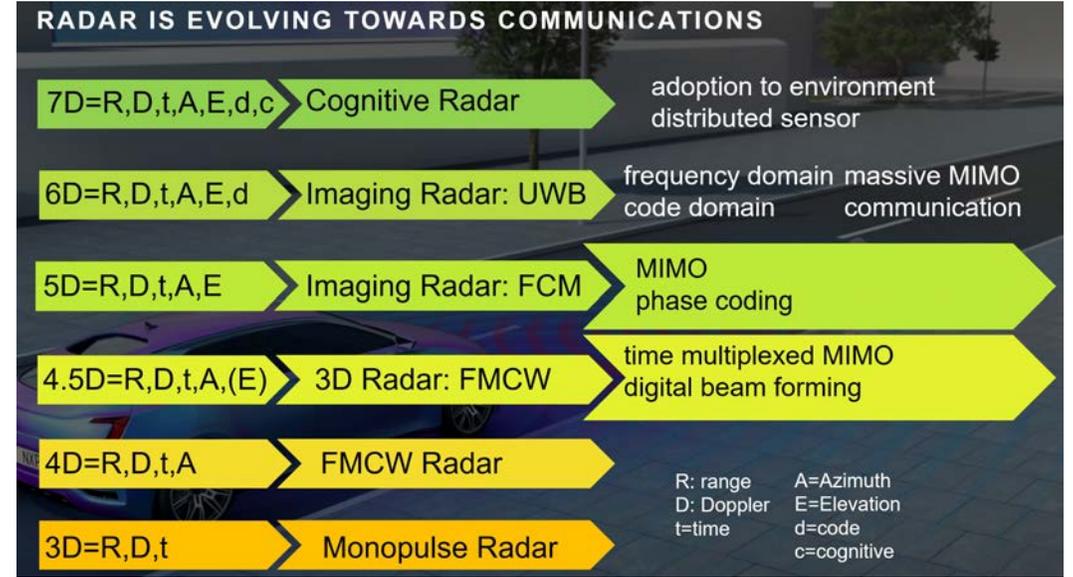
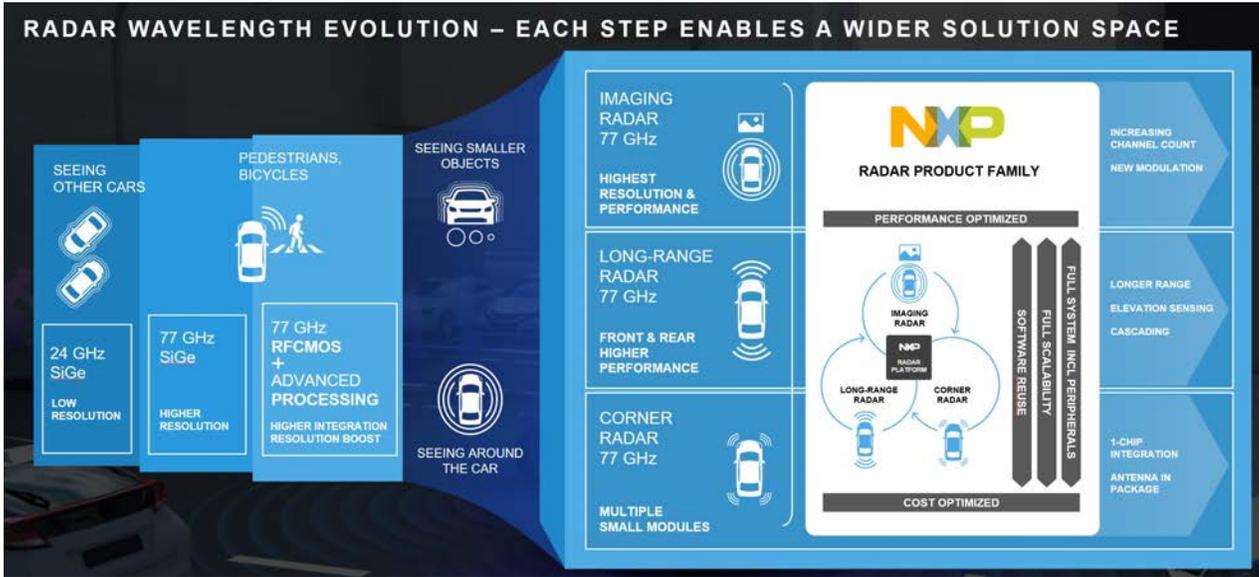
## TECHNOLOGY COMPLEMENTARITY AND REDUNDANCY IN PERCEPTION

	 Camera	 LIDAR	 Radar	 Fusion
Distance Ranging	<i>Indirect</i>	<i>Time of Flight</i>	<i>Time of Flight</i>	
Speed Measurement	<i>Indirect</i>	<i>Indirect</i>	<i>Direct Doppler</i>	
Angular Separation	<i>Megapixels</i>	<i>0.1° - 0.25°</i>	<i>1° - 3°</i>	
Colour Patterns	<i>Traffic Signs &amp; Lines</i>	<i>Intensity only</i>	<i>No</i>	
Adverse Weather/Light	<i>Very Limited</i>	<i>Limited</i>	<i>See through rain, fog, snow, night, sun</i>	
Output Data	<i>2D Image</i>	<i>3D Point Cloud</i>	<i>4D Target List</i>	<i>Complete 360° Perception</i>
Best For	<i>Recognition of Objects, Signs, Lanes</i>	<i>Freespace / Boundary Detection, Localization</i>	<i>All-weather distance &amp; speed measurement</i>	<i>Autonomous Driving L3+</i>

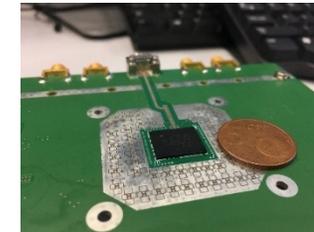
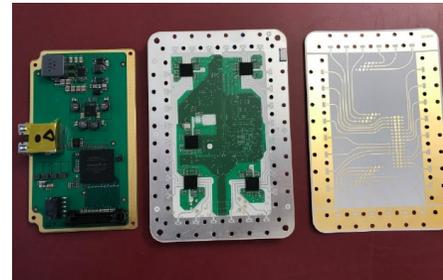
- No Sensor is perfect: the one sensor sees what the other does not see
- Functional Safety requires diversity in failure modes
- The path for affordable LIDAR keeps going on ...

**Is it that simple? Lidar, Radar, Camera?**

# ZOOM-IN AUTOMOTIVE RADAR EVOLUTION



## Enablers of 77GHz solution space expansion



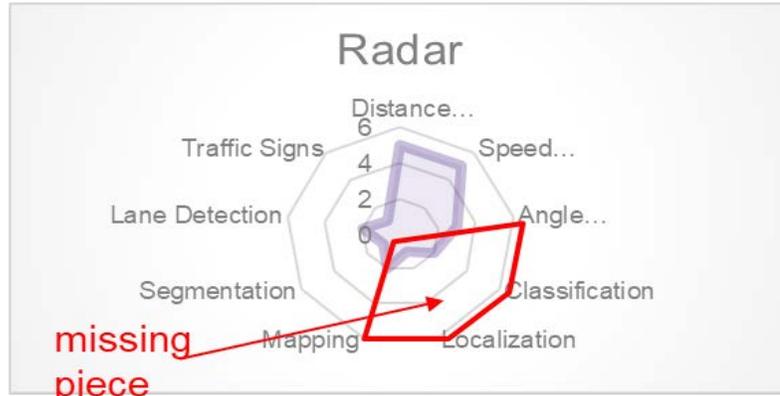
Mm-wave CMOS & ADC/CHIRP technology-front push  
One chip MIMO MMIC and Radar DSP size reduction  
Pathway to cascading/MIMO

3D WG/Antenna.

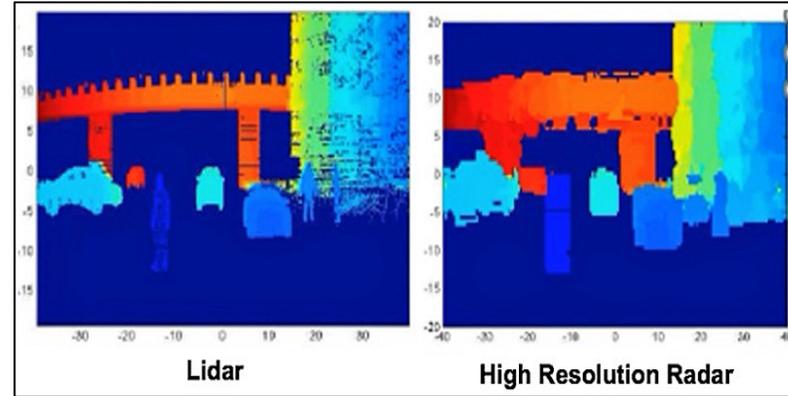
Mm-wave packaging  
/ Antenna-in-package  
Beginning of in-package integration

**Much more is needed!**

# RADAR / SENSING NEEDS AND 77GHZ BAND LIMITATIONS



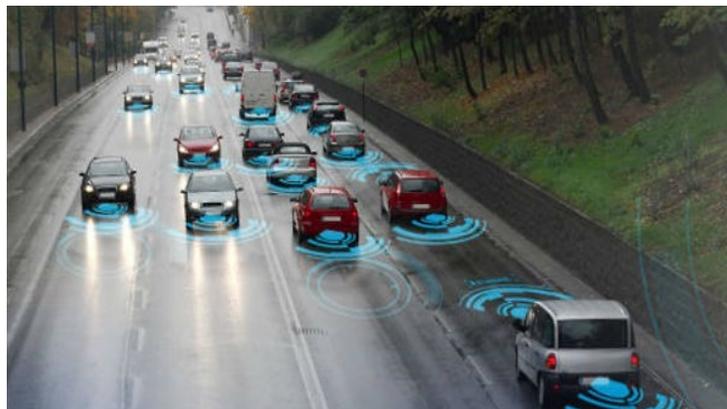
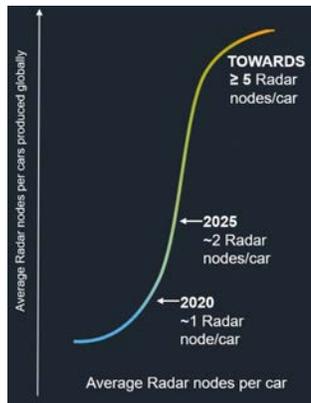
Mapping, localization, classification



"Lidar like" angular resolution, 360d view, Elevation



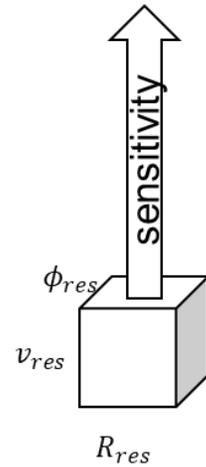
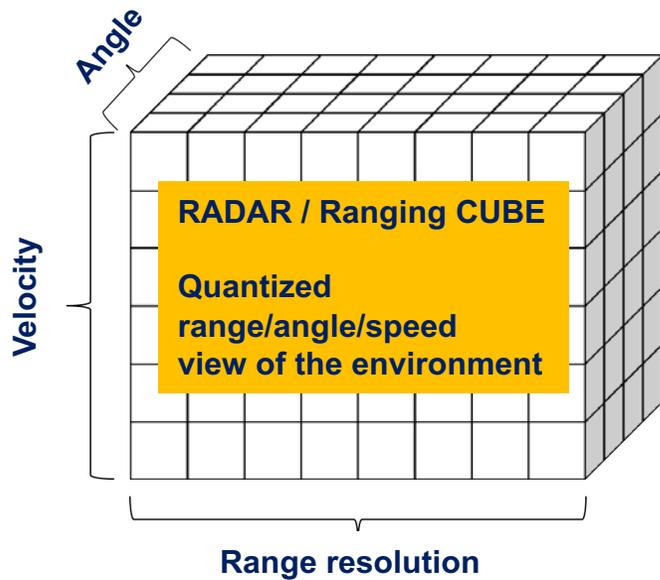
Size reduction



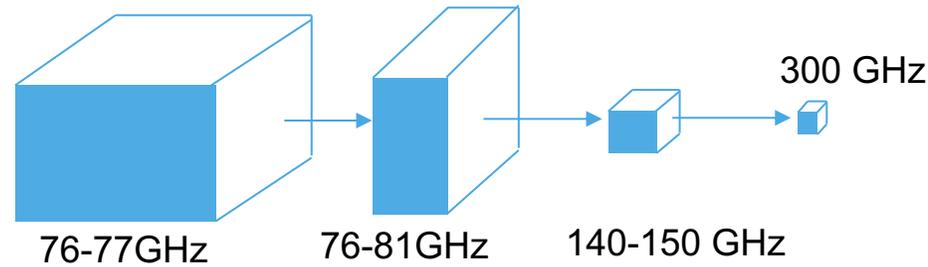
Interference management needed!  
Advanced waveforms in conflict with FMCW.

- Multiple limitations at 77GHz:**
- Fixed dimensions limits angular resolution
  - Bandwidth regulations and application defined (safety) radar cycle time limit range resolution
  - Resolution, Angle, speed tradeoffs
  - MIMO scalability / waveform orthogonality
  - MMIC power consumption

# IMPROVING RESOLUTION - OPPORTUNITIES AND CHALLENGES

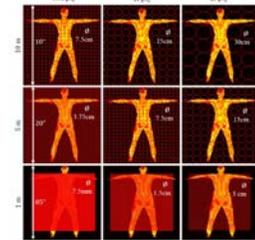


## Mm-wave Ranging evolution



## Mm-wave Imaging

10m passive imager view  
[S.v.Berkel, TU Delft]

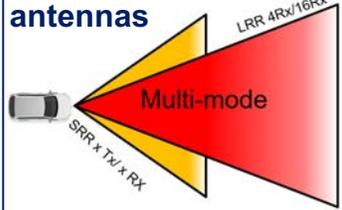


- Adoption of smaller wavelengths enables fundamental step in resolution and size reduction.
- More information classes become available!
- Finer sensor granularity possible: Ranging , Radar-Imaging, Camera, Light Ranging.

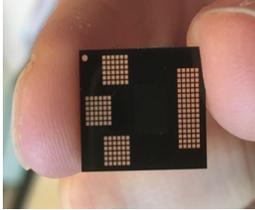
**Challenges ahead: Link budget, massive MIMO complexity, data rate explosion, no tech that does it all, power/heat management, manufacturing, reliability, cost...**

# HOW TO GET THERE – RESEARCH DIRECTIONS

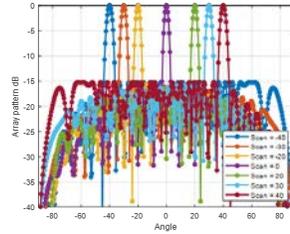
Electronic multi-mode antennas



Array-in-package



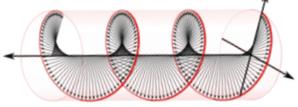
Sparse arrays



Conformal antennas



Polarimetry (feature extraction)

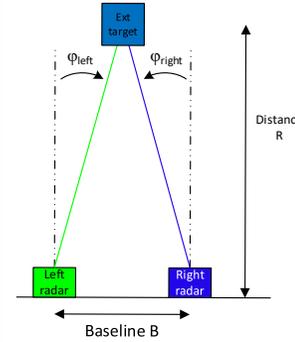


Mm-wave lenses  
Optical techniques



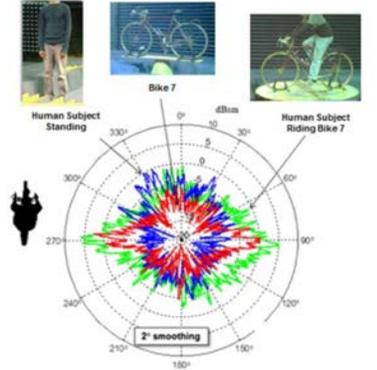
Massive MIMO  
Time, frequency, code

Distributed radar



Compressive Sensing

Explore channel behavior wavelenths



Radar image Processing with A.I.  
Enhanced classification

**multiple functions, in-package integration, multiple nodes  
advanced DSP: all conditioned together to the sensing function!**

Mm-wave signal generation  
RFCMOS? SiGe?  
Efficiency, reliability, Noise

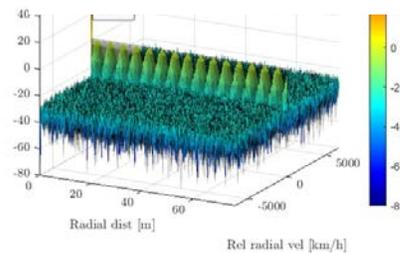
Arbitrary Waveform generators  
supporting radar signatures

Context/feature extraction in  
Analog to Digital

Synchronization in  
massive arrays



Full duplex / echo  
cancellation for MIMO



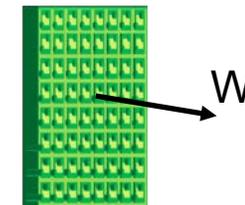
+ mm-Wave Tech Nodes,  
Grade1/150C

+ Antenna/Waveguide,  
Passives, Lenses

+ More radar DSP, more channels  
further CMOS scaling

Panel & System-in-Package/  
3D integration

- mechanical, tolerances,
- Heat management, mm-wave routing



System partitioning – electrification trends

# Intelligent Sensing and Sensor Fusion: Opportunities and Impacts

Wai Lee

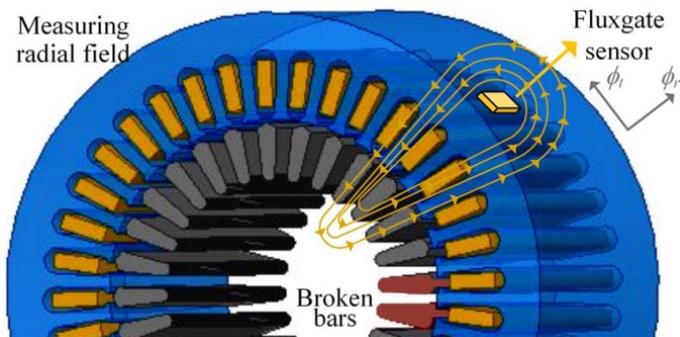
Chief Technologist, Sensing Products

Texas Instruments Inc.

June 10, 2021

# Multi-modal Sensing and Sensor Fusion

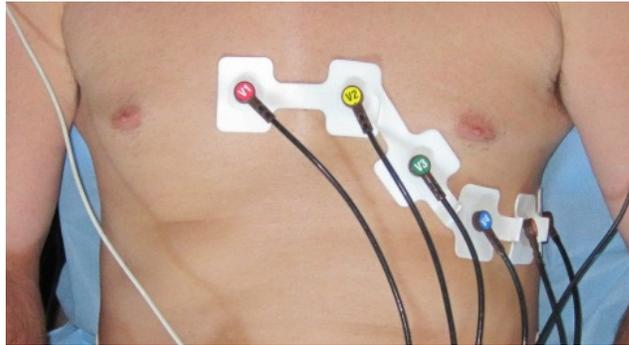
- Example: motor health monitoring
  - Multiple sensing modalities: Vibration, temperature, magnetic flux, and current
  - Yet to be accomplished:
    - Edge processing helps to minimize the energy used for data transmission to the cloud, allowing battery operated sensor nodes
    - Edge (local) sensor fusion to make timely decisions and interact with motor control
    - AI techniques to enable failure pattern recognition
    - Self monitoring sensors themselves for reliability
    - Security intelligence
- Innovation opportunities in next decade:
  - Sensor fusion at the edge
  - A2I, rather than A2D
  - Compressive sensing with multiple sensing modalities
  - Self health monitoring of sensors
  - Low complexity and energy efficient algorithms for pattern recognition and data security



Source: Prof. Akin, UTD, SRC Task 2810.016

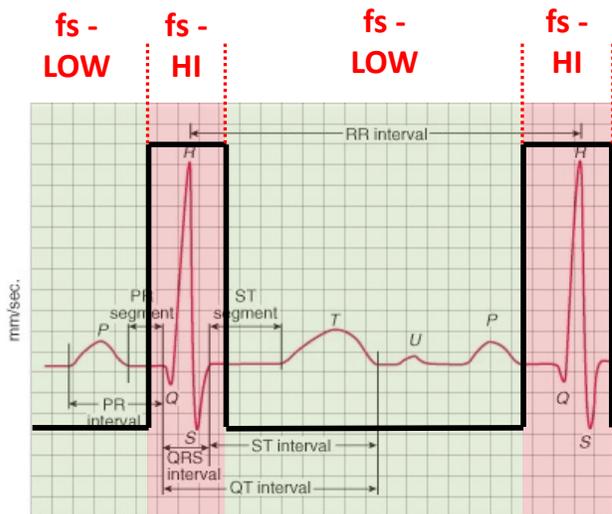
# Compressive Sensing and A2I

- Good progress in compressive sensing in past decade, demonstrating significant power savings in imaging, audio, and health applications



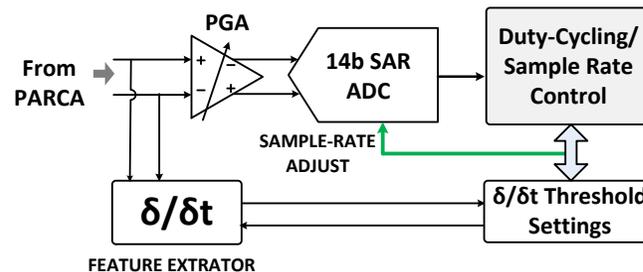
Wearable ECG  
~10x power reduction by adaptive sampling

- Innovation opportunities in next decade
  - Most compressive sensing techniques are application specific. How do we make them more general purpose by having more intelligence?
  - System level optimization to determine “I” for A2I
  - Flexibility vs optimization tradeoffs



mm/mV 1 square = 0.04 sec/0.1mV

**Low Importance** **High Importance**



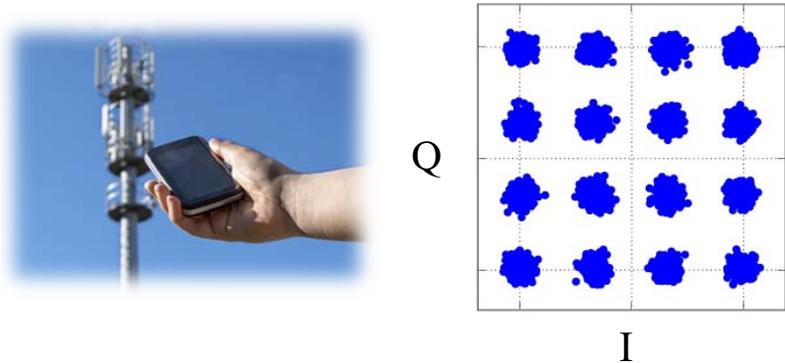
Source: Sharma, et al, IEDM 2016

# New Trajectories for Analog Electronics

Boris Murmann

June 10, 2021

# Communication



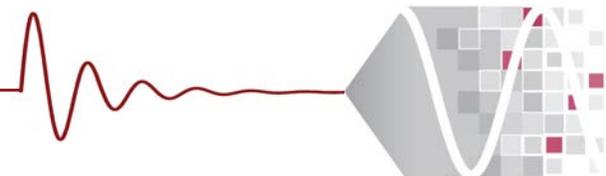
- Info bits per sample = large
- OK to digitize each sample

# Inference

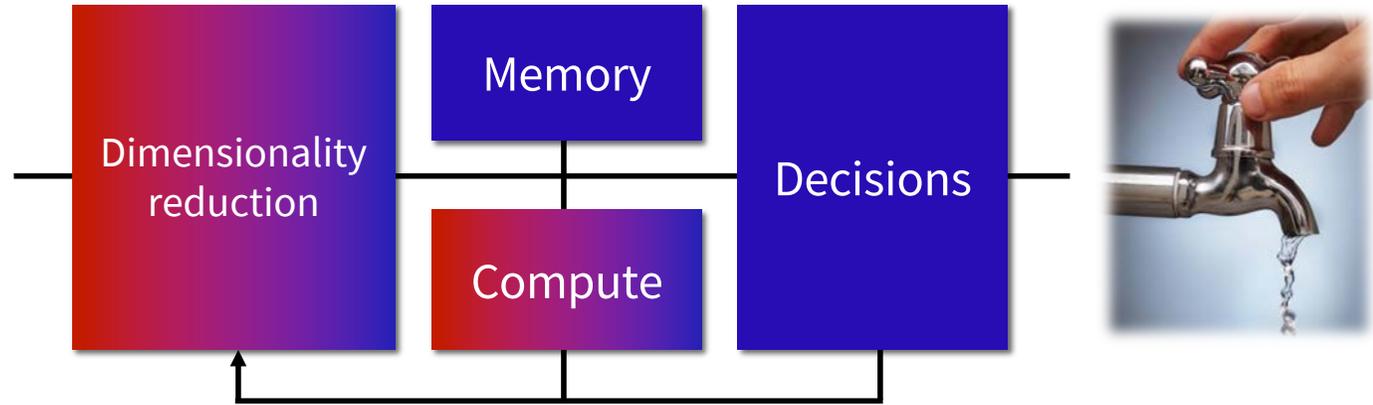


- Info bits per sample = very small
- Human speech: ~39 info bits/sec
- Full digitization: ~hundreds kbits/sec

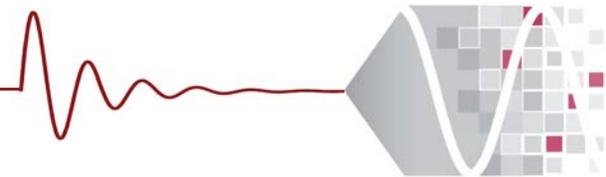
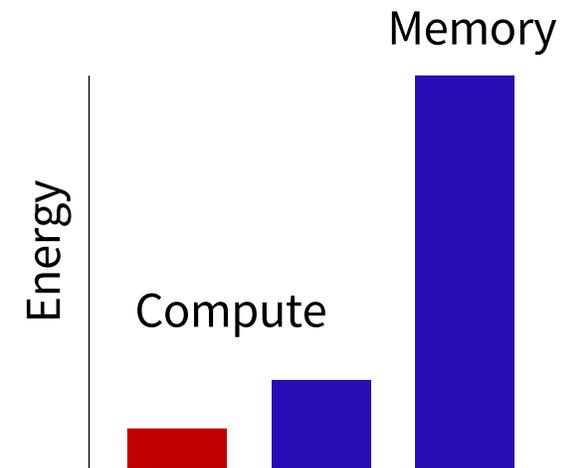
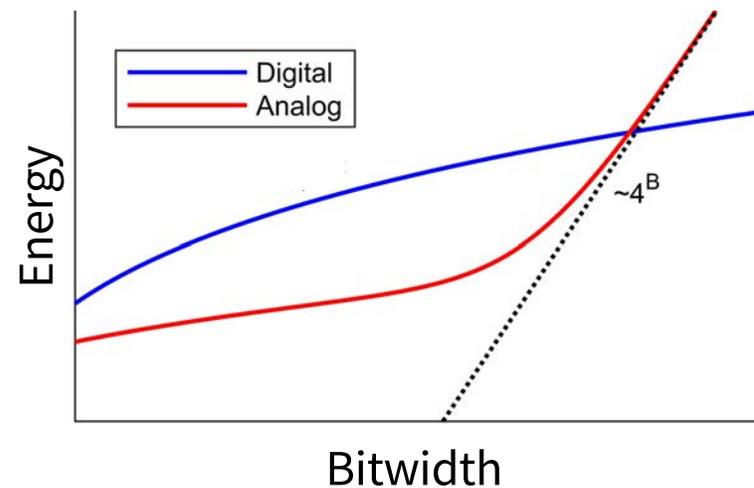
Hard to justify use of “same old” A/D interface for inference

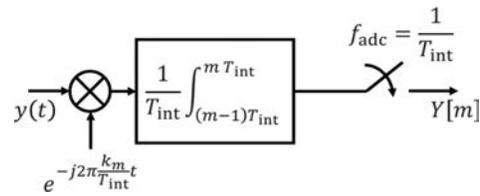


# Interfaces 2.0



- Domain-specific and “data driven” architecture design
- Minimize data conversions, data movement, memory access
- Combine strengths of analog & digital for low-energy processing





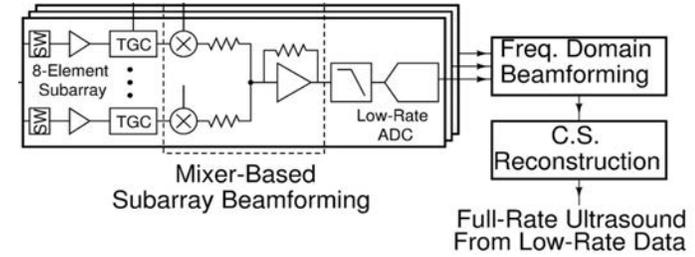
**30x**

**Predistorter spectrum sensing**  
Hammler, TCAS1 2019



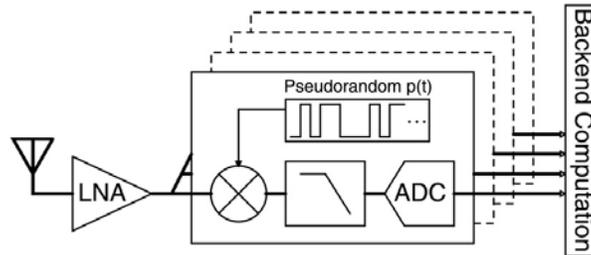
**25x**

**Log gradient imager**  
Young, JSSC 2019



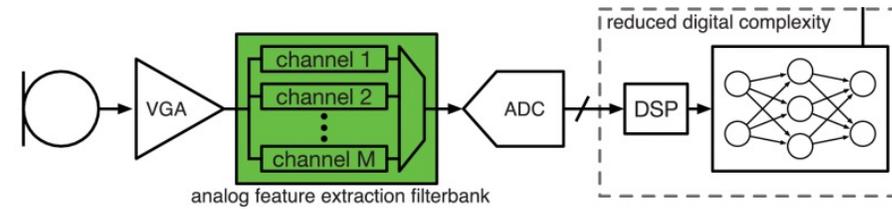
**43x**

**Sub-Nyquist ultrasound**  
Spaulding, IUS 2015



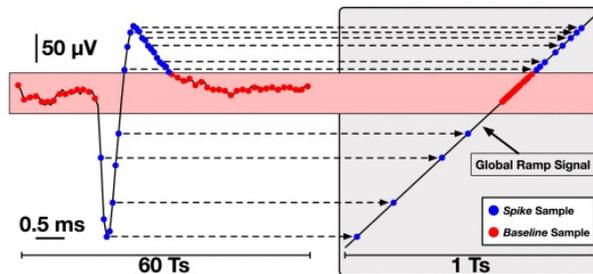
**RF spectrum sensing**  
Adams, JSSC 2017

**180x**



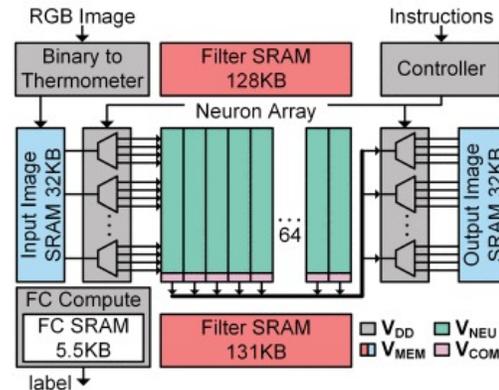
**1000x**

**Audio feature extraction**  
Villamizar, TCAS1 2021



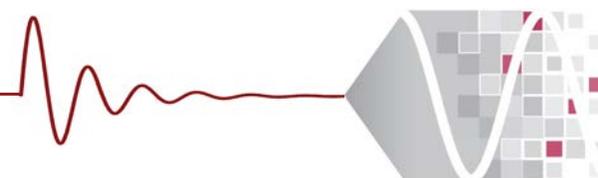
**40x**

**Compressive neural recording**  
Muratore, TBioCAS 2019



**Mixed-signal neural network**  
Bankman, JSSC 2019

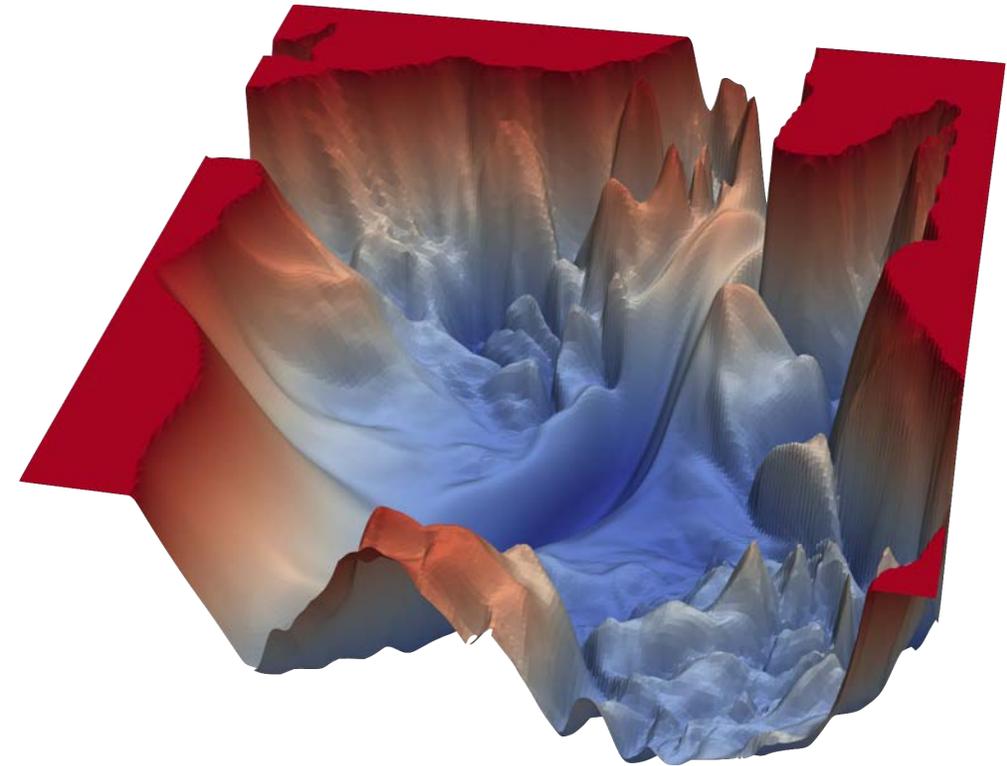
**772 1b-TOPS/W**



# Challenges and Research Needs

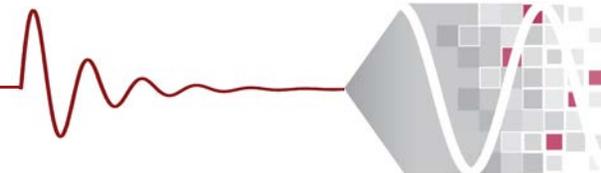
- How to generalize and amortize R&D effort across multiple applications?
- How to determine analog block requirements without running huge number of CPU cycles?
  - › Much easier for Interfaces 1.0
- How to link architecture search to relevant low-level circuit specs?
  - › Example of an insufficient proxy: Number of neural network model weights
- How to educate next generation IC designers to embrace higher levels of abstraction?

**The world is complex in high-dimensional space...**



**Loss landscape of a neural network**

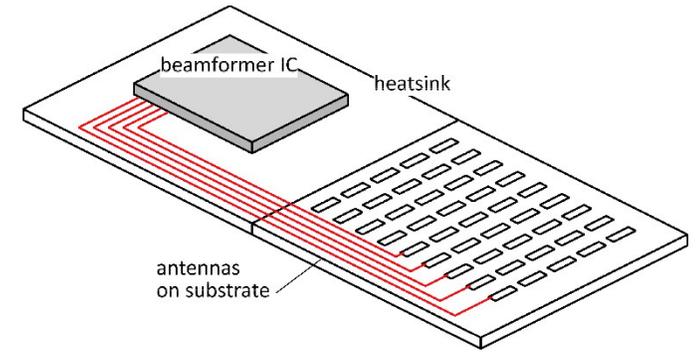
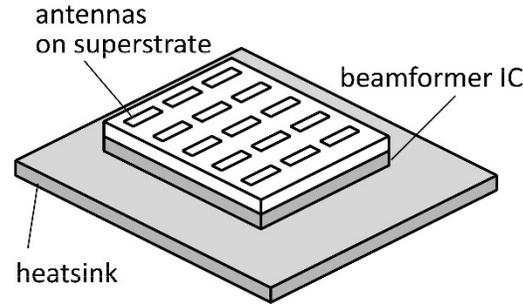
<https://www.cs.umd.edu/~tomg/projects/landscapes/>



# 2nd Discussion Phase

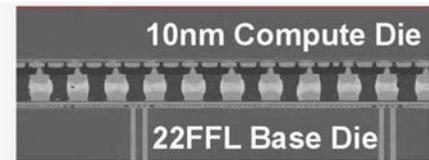
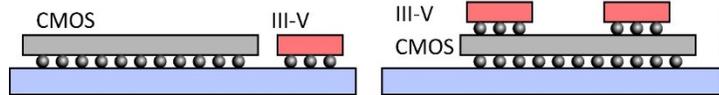
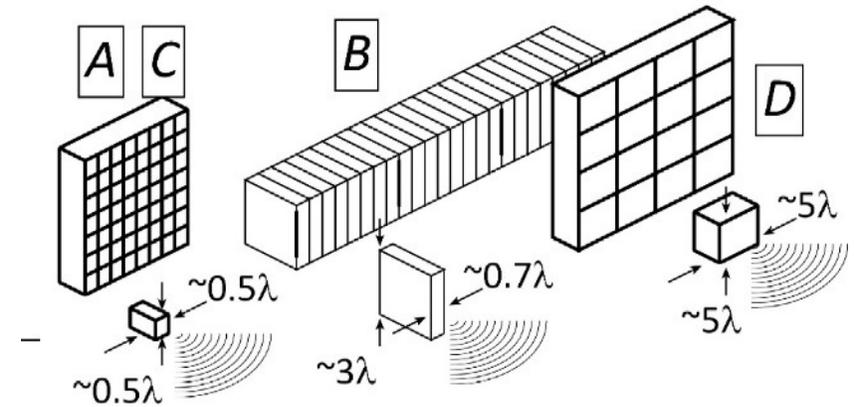
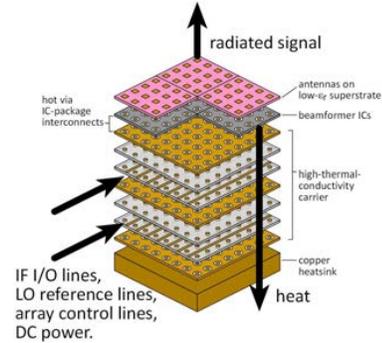
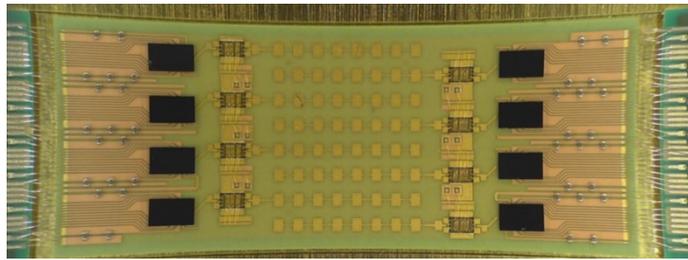
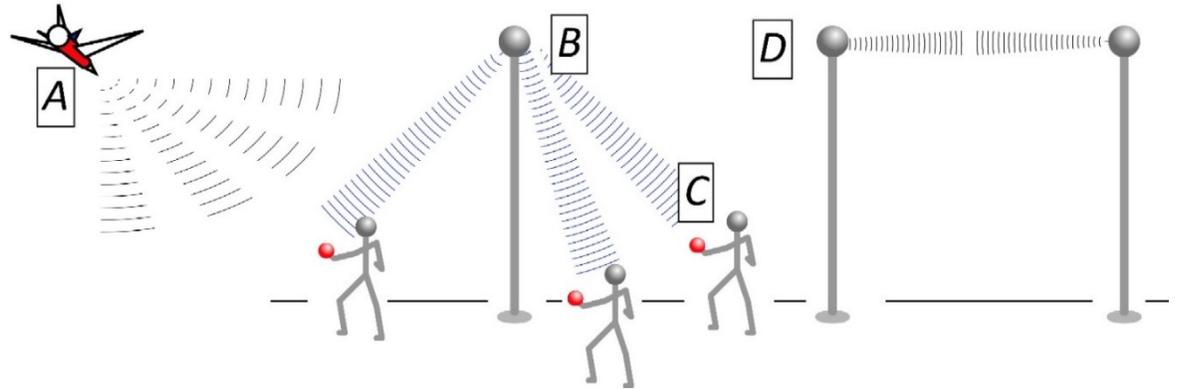
# The mm-wave packaging problem

How to make the IC electronics fit ?  
 How to avoid catastrophic signal losses ?  
 How to remove the heat ?



Not all systems steer in two planes...  
 ...some steer in only one.

Not all systems steer over 180 degrees...  
 ...some steer a smaller angular range

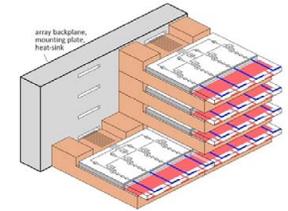


# Future wireless: many, many low-power channels

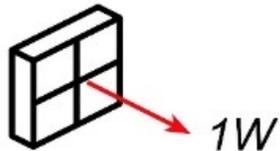
More & more channels @ lower (RF power, DC power, area, cost) /channel,

$$P_{received} = \frac{A_t A_r}{\lambda^2 R^2} e^{-\alpha R} \cdot P_{trans} \longrightarrow \# \text{beams} \cdot (\text{bit rate per beam}) \cdot kTF \cdot \text{SNR} = \frac{A_t A_r}{\lambda^2 R^2} e^{-\alpha R} \cdot P_{trans}$$

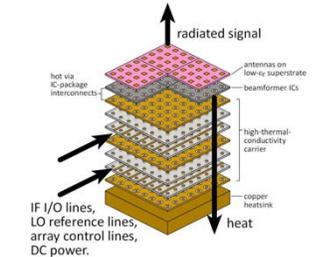
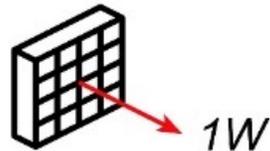
Proposed scaling law	change	Implication	change
carrier frequency	increase 2:1	capacity (# beams·bit rate per beam)	increases 4:1
aperture area	keep constant	number elements	increases 4:1
total transmit power	keep constant	RF power per cm <sup>2</sup> aperture area	stays constant
		RF power per element	decreases 4:1



100GHz



200GHz



**High-frequency arrays** : vast #s of elements, small area per element, low RF power per element

**Need:** dense mm-wave IC design → High gain/stage, small passive elements

**Need:** low-power mm-wave IC design (mixers, LNAs, Δφ...) → high gain/stage, ultra-low V<sub>DD</sub>,...

**Need:** efficient back-end processing; massive #s of low-SNR signals. New digital beamformer designs

**Need:** new low-precision array architectures.

# Advanced interconnects: not just for VLSI

## 5G/6G needs high-performance IC interconnects

low interconnect losses  
high interconnect & passive element density

## High integration density:

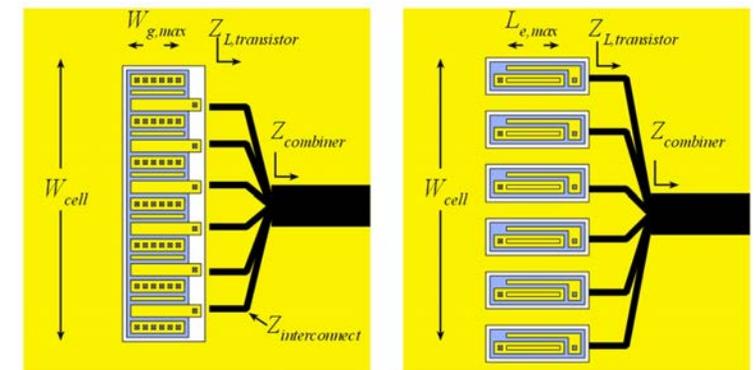
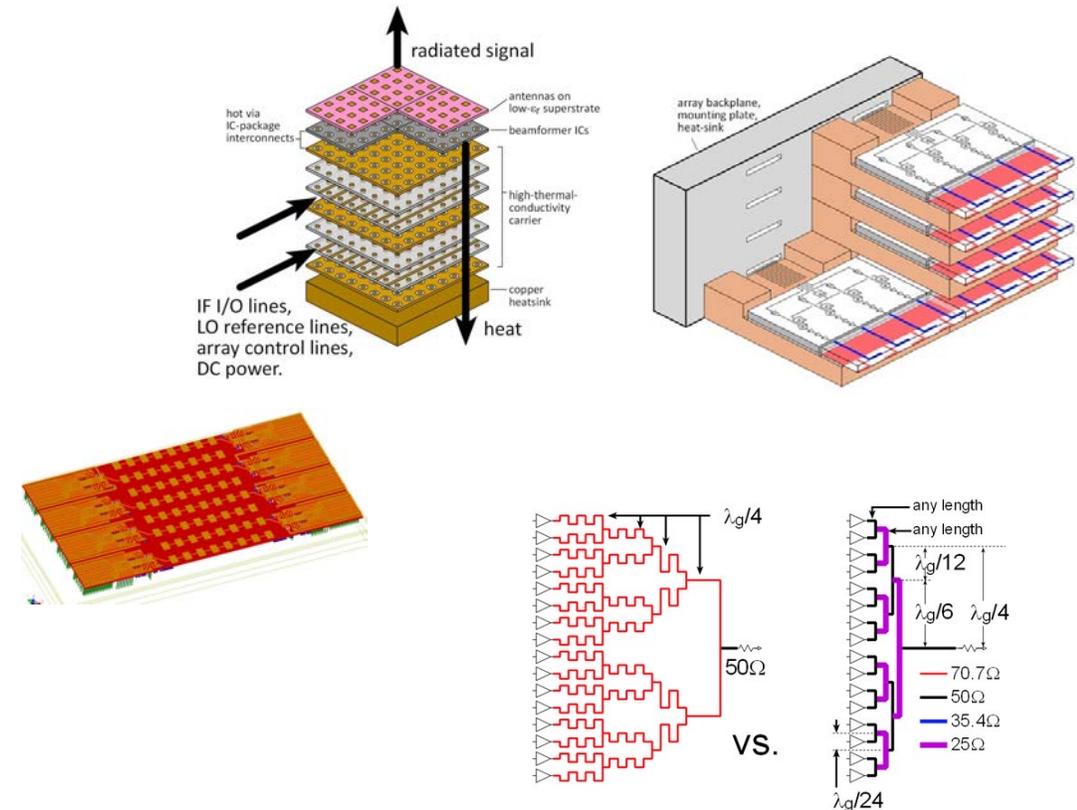
fitting transceiver into  $\lambda/2$  pitch  
transistor footprint  
50 $\Omega$  line interconnect pitch.

## High density for efficient power-combining

short lines = low-loss lines  
transistor power cells must be small to fit

## High density for efficient multi-finger transistors

short lines = low-loss lines



# Implications: massive MIMO beamforming

# channels / # signals is spatial oversampling:

**ADCs/DACs:** not many bits required

(Madhow, Studer, Rodwell)

**RF component linearity:** 1dB compression points can be fairly low

(Madhow)

**Phase noise:** phase noise can be moderately high

**Beamspace:**

lower frequencies, many NLOS paths, complicated channel matrix:  $O(M^3)$  to beamform

higher frequencies, few NLOS paths, simpler channel matrix: FFT,  $O(M \cdot \log M)$  to beamform

easier to separate signals in beamspace

fewer bits in signal; fewer bits in FFT coefficients.

(Studer, Madhow)

