Comments of the
Semiconductor Industry Association (SIA)
on the Department of Commerce "Notice of Request for Information (RFI) on Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry"

87 FR 3497 (Jan. 24, 2021) [Docket No. 220119-0024]

Submitted March 25, 2022

The Semiconductor Industry Association (SIA)[1] appreciates the opportunity to provide input on the Department's efforts to inform the planning and design of potential CHIPS for America Act programs authorized under Title XCIX of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (Pub. L. No. 116-283).

SIA welcomes the opportunity to assist the Commerce Department in the implementation of the historic investments included in the CHIPS for America Act. The CHIPS for America Act will help revitalize American semiconductor manufacturing by providing unprecedented incentives to promote the construction of new, expanded, and upgraded fabs and help revitalize U.S. technology leadership by making significant investments in semiconductor research. These initiatives are critical to strengthening the U.S. economy, national security, and technology leadership.

SIA has played an active role in the development and execution of many of the industry's past collaborative efforts and government-industry partnerships. We believe an organization representing the entire semiconductor industry, bringing together senior executives, technologists, and others, coupled with a successful history of collaborating with government, can be a most effective overall partner with the U.S. government in implementing the CHIPS Act.

While we respond to Commerce's specific questions below, we respectfully urge Commerce be guided by the following principles in implementing the manufacturing incentives and research initiatives.

[1] SIA is the voice of the semiconductor industry, one of America's top export industries and a key driver of America's economic strength, national security, and global competitiveness. Semiconductors – the tiny chips that enable modern technologies – power products and services that have transformed our lives and our economy. The semiconductor industry directly employs nearly a quarter of a million workers in the United States, and U.S. semiconductor company sales totaled $208 billion in 2020. SIA represents 98% of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. chip firms. Through this coalition, SIA seeks to strengthen leadership of semiconductor manufacturing, design, and research by working with Congress, the Administration, and key industry stakeholders around the world to encourage policies that fuel innovation, business, and international competition. Additional information is available at www.semiconductors.org.

General

- In order to best leverage and engage leading commercial companies, programs should be implemented in a streamlined, flexible, competitive, and equitable manner with limited bureaucracy and administrative burden. Once funds are dispersed, companies and consortia should be able to operate to the maximum extent under market principles and with limited constraints, consistent with ensuring the proper use of government funds. The CHIPS Act already has specific criteria to ensure the funds provided are properly used.

Manufacturing Incentives

- CHIPS Act grants must be prioritized to catalyze investments that will have the greatest impact on renewing U.S. innovation, increasing U.S. technology leadership, and stabilizing U.S. supply chains. As stated by the National Security Commission on Artificial Intelligence, "The United States should commit to a strategy to stay at least two generations ahead of China in state-of-the-art microelectronics and commit the funding and incentives to maintain multiple sources of cutting-edge microelectronics fabrication in the United States." The U.S. simply cannot afford to fall behind, or worse yet, permanently exit the race for semiconductor innovation leadership. At the same time, incentives for manufacturing should be provided to fill in the gaps and vulnerabilities throughout the entire semiconductor ecosystem and to expand semiconductor development and manufacturing in the United States across the full range of technologies, including analog, memory, and logic at the leading-edge, mainstream, and legacy nodes, and include advanced packaging/testing and key areas in semiconductor manufacturing equipment and materials.
- Incentives should apply broadly to encompass semiconductor fabs, packaging facilities, and research facilities, as well as facilities producing equipment and materials necessary for the fabrication of semiconductors and their assembly, packaging, and testing, and be open to global companies from allies and like-minded strategic partners.
- Given the varied capital and operational challenges that have worked to create gaps in the supply chain here in the U.S., flexibility on the proportion of U.S. government support (as opposed to a U.S. government match that cannot exceed a fixed percentage of the overall program) is needed, with that proportion driven by national and economic security factors.
- Funding provided under the CHIPS Act should be provided to projects that are commercially viable and sustainable over the long term. When funding manufacturing facilities, and consistent with Congressional intent, CHIPS Act funding should only be provided if the facilities can be constructed and begin manufacturing in an expeditious manner.

Research Programs and Workforce Development

- Research programs, including those associated with the National Semiconductor Technology Center (NSTC), should be industry driven in collaboration with government and academia with the goal of transitioning the most promising innovative research

technologies to prototyping and commercial production. Broad participation across all segments of the industry will be required to best identify the most promising emerging technologies and to provide a clear pathway for transition.

- The technical focus of the associated research programs, including those associated with the NSTC, should be guided by industry leadership at the highest levels and should be dynamic rather than static. There should be periodic opportunities for industry, with input from government and academic stakeholders, to reassess and redirect the focus of these efforts to ensure continued relevance to the commercial sector.
- The NSTC should prioritize high-impact, project-based research initiatives targeting ambitious goals, similar to the research structure at DARPA or to the kinds of projects that drive breakthrough solutions to "seismic shifts" identified by SRC in "The 2030 Decadal Plan for Semiconductors" report.[2] These projects should aim to be revolutionary, rather than evolutionary, within the context of a transfer to foundry.
- The National Semiconductor Technology Center (NSTC) and the National Advanced Packaging Manufacturing Program (NAPMP) should be viewed as interrelated parts of a holistic approach to advancing semiconductor innovation, rather than separate and distinct activities. SIA recommends the two programs be guided by a single strategy for industry as a whole.
- Critical operational issues associated with the NSTC and NAPMP – including the structure and governance of these programs, and the location(s) of facilities, and their degree of coordination and integration – should be guided by the technology agenda for these programs.
- The treatment of intellectual property (IP) should depend on the particular circumstances of the research program and the optimal path for commercialization. In many circumstances, putting research results in the public domain is most helpful to industry to utilize the results in commercial activity. In other circumstances, it is more effective to provide exclusive IP rights to the inventor or inventors of the IP so they can commercialize the results in their commercial activity. For example, earlier stage research with a larger portion of funding coming from grants may indicate that more IP rights should remain in the public domain, whereas later stage research or projects where most funding comes from specific companies may indicate the need for more exclusive IP rights to inventors. Lastly, there can be circumstances in which providing non-exclusive IP rights to the sponsors of the research provides the broadest path to commercialization.
- Substantial financial support should be devoted to (i) university-based semiconductor research activity, (ii) expansion of green card opportunities for STEM graduates, (iii) expansion of women and minority representation in STEM education and (iv) training for technicians utilizing, among other institutions, two-year colleges.
- Because of the global nature of the semiconductor industry and its supply chain, cooperation with friendly governments and likeminded strategic partners, can amplify and enhance the impact of research initiatives.

[2] See "The Decadal Plan for Semiconductors," January 2021, https://www.src.org/about/decadal-plan/

II. CHIPS Act

The CHIPS Act presents a generational opportunity to strengthen semiconductor manufacturing and research in the United States. It rightly takes aim at improving semiconductor R&D and manufacturing in the United States, capabilities common for the entire semiconductor industry and critical for the many industries and fields of innovation which rely on increasingly powerful, energy efficient semiconductors. Global leadership in semiconductor research, design, and manufacturing will provide major benefits to the nation's economy, standard of living and national security. Sound investment by both government and industry in these areas can produce returns that dwarf the initial investment.

To achieve these benefits, however, such investment must be carefully constructed, systematically measured, and ultimately commercialized.

The CHIPS Act establishes many programs to achieve meaningful improvements in semiconductor R&D and manufacturing in the United States. Areas such as advanced research, leading edge infrastructure, manufacturing and investment funds require features tailored to their particular character and circumstances. Hence, for example, awarding government funds to create or expand manufacturing facilities and infrastructure merits a different process or mechanism than undertaking collaborative research. Similarly, different treatment is necessary for pre-competitive research, prototyping, and proof-of-concept collaborations.

III. SIA's Consortium Experience

SIA's experience over the last 40 years has been primarily with research collaboration on an industry-wide basis that has included government and academic participants.

In the early 1960s, the growth of semiconductor firms was constrained by lack of advances in fundamental research and skilled workers. To address these needs for the entire industry, SIA formed an affiliated, non-profit corporation, the Semiconductor Research Corporation (SRC), to fund university research in the United States and thereby support university faculty and students. Unique among industries, semiconductor firms have continued to invest in SRC for 40 years. New research programs have been developed, foreign semiconductor participants have joined, and government departments and agencies have participated. This inclusive and collaborative SRC structure has proven to be flexible, durable, and scalable.

A new challenge confronted the U.S. semiconductor industry in the 1980s in the form of advanced manufacturing competition from the Japanese semiconductor industry and lagging technology development in U.S. semiconductor manufacturing equipment and processes. In response, SIA launched SEMATECH, a new consortium of industry and government that would conduct research at its own facility. Industry and DARPA jointly managed and funded SEMATECH through equal contributions, a model that departed from the traditional mode of government dictating how its funds are to be used. SEMATECH operated a research and manufacturing facility until it was shut down when SEMATECH's principal mission was completed.

In cooperation with SRC, SIA has launched several industry-wide consortia in pre-competitive, fundamental research that have included government agencies and universities. The Focus Center Research Program (FCRP), Semiconductor Technology Advanced Research Network

(STAR-Net), Joint University Microelectronics Program (JUMP) and Nanoelectronics Computing Research (nCORE) were all completed after successfully meeting their long-term research goals. SIA has also worked with different government departments and agencies to create new methods for government/industry collaboration. In particular, SIA assisted DARPA in devising a new form of Other Transaction Authority (OTA) to facilitate and streamline the formation of government/industry consortia and worked with the Energy Department to develop more flexible means for industry to fulfill policy and political requirements relating to domestic manufacturing and U.S. content.

Lastly, SIA in conjunction with SRC, has pioneered technology roadmaps for the semiconductor industry, including the International Technology Roadmap for Semiconductors (ITRS) and the new 2030 Decadal Plan for Semiconductors, to address the major technology challenges now facing the semiconductor industry.

IV. Principal Lessons Learned for Consortium Undertakings

In the course of SIA experience with industry-wide consortia, certain characteristics have emerged as particularly valuable in enabling a broad consortium, sustaining its operations and achieving significant benefits. Not every feature is relevant to all consortia, nor need they all be present in a single consortium. Many of the features below are fundamental, and each is capable of enhancing prospects for success in a consortium that can include industry, government and academia.

1. Formulate a clear objective for the consortium that (i) has urgency for industry, (ii) can be broadly applied and (iii) is measurable. Such an objective can attract a critical mass of participants, keep the consortium focused, and permit rate of return calculations to support continued investment.
2. Cultivate and rely on industry leadership for the direction, technical content and governance of the consortium. A “partnership of the willing,” in which risks and benefits are shared equally and direction is arrived at jointly, can elevate the chances of success. Having a core group of senior company officials committed to and engaged in the consortium is most desirable.
3. Encourage broad participation by offering appropriate tiers of participation based on the interests and capabilities –technical, financial, and otherwise-- of potential participants. An industry consortium generally should be open to the broadest range of participants, and encourage participation from global technological leaders, while taking into account access to intellectual property that is generated.
4. Seek government consortium participants who can bring funding to the consortium but within the constraints of the law are willing to share risks, responsibilities, and authority.
5. Base consortium decisions and actions to the greatest extent on technical merits. Non-technical conditions and constraints should be minimized.
6. Utilize a project-based approach that has a beginning phase, a reassessment phase, and a completion phase. A continuous level of activity without explicit goals is difficult to measure and sustain.

7. Proceed with a flexible agenda that makes explicit room for creativity and ambitious breakthrough ideas.
8. Maintain a focus on commercialization that will speed release of consortium results into a global market as the most effective means to assure the technical leadership of consortium participants and meet government needs.
9. Minimize consortia overhead, especially as it relates to facilities and infrastructure. The costs of semiconductor facilities and equipment are very high, and they can become obsolete very quickly. Leverage existing infrastructure, capabilities, and expertise where sensible. Incentivizing private sector entities to operate facilities or infrastructure is more efficient than leaving the responsibility with a consortium. Complex manufacturing, for example, will require coordination and partnership with leading edge facilities.
10. Enlist and underwrite the participation of undergraduate, graduate and post graduate students in the technical work of the consortium as a most effective way to develop new talent for the entire pool of participants. Additional programs and support of students can best be undertaken by existing industry institutions long dedicated to such activity rather than by new consortium itself.

V. Responses to Specific Questions from the RFI

Semiconductor Financial Assistance Program

1. *The term "semiconductor" is not specifically defined in Section 9902 of the NDAA; rather, the legislation leaves it to the Secretary of Commerce to define. What factors do you consider important in developing a definition of "semiconductor" for purposes of a semiconductor manufacturing incentives program?*

Semiconductors are highly specialized components that provide the essential functionality for electronic devices to process, store and transmit data. Most of today's semiconductors are integrated circuits, also referred to as "chips." A chip is a set of miniaturized electronic circuits composed of active discrete devices (transistors, diodes), passive devices (capacitors, resistors, inductors, MEMS) and the interconnections between them, layered on a thin wafer of semiconductor material, typically silicon. Modern chips are tiny, packing billions of electronic components in an area as small as only a few square millimeters.[3]
The industry generally adheres to the definition provided by World Semiconductor Trade Statistics, under which "semiconductor products" are defined as either:[4]

1. "Packaged or encapsulated die or chips with leads or contacts, which are tested and marked (or identified) to meet the product specifications (finished products)"; or

[3] SIA, Strengthening the Semiconductor Value Chain in an Uncertain Era, https://www.semiconductors.org/wp-content/uploads/2021/05/BCG-x-SIA-Strengthening-the-Global-Semiconductor-Value-Chain-April-2021_1.pdf (p. 9)
[4] WSTS, Product Classification 2021, https://www.semiconductors.org/wp-content/uploads/2021/02/Product_Classification_2021.pdf (p. 4)

2. "Die, chips or wafers, which have not been encapsulated but have been tested to meet the product specifications and are identified by the container or package in which they are shipped"

While industry taxonomies typically describe more than 30 types of product categories, semiconductors products under this definition can be classified into three broad categories: logic, memory, and discrete/analog/other (DAO), multicomponent (MCO)[5]. Notably, the WSTS definition does not include related items like printed circuit boards or solar panels as "semiconductor products". For more information on the various subcategories of semiconductor products, refer to pages 4 to 24 of the 2021 WSTS production classification.[6]

Despite the technical dimensions of the definition of semiconductors, the contours of the semiconductor industry in practice center on integrated circuits, discretes, optoelectronics, sensors, and actuators. We believe such a broad and loosely limited definition of the semiconductor industry should serve as the basis for the implementation of the CHIPS Act.

2. *Section 9902 permits a "consortium" of public and private entities to apply for funding. What factors would public and private entities consider determining whether to apply for funding as part of consortium? How would private entities determine whether to work with a public entity as part of a consortium? How would a private entity consider working with other private entities (such as customers, equipment manufacturers, or capital providers) as part of a consortium?*

There are many factors to consider regarding the choice to participate in a consortium. In the past it has generally been effective for companies to enlist in a broad coalition or consortium for semiconductor research which can then, based on technology road mapping and individual priorities, establish industry-wide projects or programs for participation by those most interested. Specific factors could include: Alignment with critical needs and interests, implementation, membership, technology agenda, sustainability. Intellectual property treatment and inclusivity, among others.

3. *Based on the criteria outlined in Section 9902 of the NDAA, what types of facilities, equipment, and other capacity aligned with the manufacture of semiconductors do you see as being most critical to the interests of the United States?*

[5] Multicomponents can be defined by reference to the U.S. International Trade Commission's Harmonized Tariff System notes at https://hts.usitc.gov/view/Chapter%2085?release=2022HTSARev2. Note 9(b)(iv)(3) defines the type of component that can be in a package to meet the definition of an MCO. However, the definition should be updated to refer to "semiconductor based" sensors, actuators, resonators, and oscillators rather than "silicon based" to include semiconductor materials such as Silicon Carbide.

[6] WSTS, Product Classification 2021, https://www.semiconductors.org/wp-content/uploads/2021/02/Product_Classification_2021.pdf

The CHIPS Act's authorizing legislation in the FY 2021 NDAA allows the Department of Commerce to consider how a covered activity is "in the interest of the United States" (§ 9902(a)(2)(C)(i)(II)). Such considerations may include national security, promoting economic growth, enhancing supply chain resilience, fostering U.S. technology leadership, and addressing the needs of the national security community, critical infrastructure, and key industries (e.g., aerospace, autos, communications, defense, etc.).[7] goals.

First, the U.S. needs to target its investments to, at a minimum, meet the basic domestic demand for semiconductor chips used in national security systems, advanced defense aerospace, and critical infrastructure, such as datacenters and communications networks[8] which is defined as sufficient domestic onshore manufacturing capacity and technical capability (e.g., research and development, associated IP, etc.) necessary to address the capacity and process node requirements for "critical applications" for over 10 different sectors of the U.S. economy. In its response to Executive Order 14017 on America's Supply Chains, the Department of Defense called for greater collaboration between the U.S. government and commercial and Defense Industrial Base companies to design and manufacture chips that are ready for adoption in DOD programs. Among its proposed action items, the report called for DOD investment authorities to lower barriers of entry for the private sector to work with the U.S. government, highlighting the need for public-private coordination in addressing critical supply imbalances.[9] These efforts could be further enhanced with augmentation to the existing DOD trusted foundry infrastructure, and progress towards quantifiable assurance could be viewed adding a tool to the DOD's semiconductor security toolbox alongside current TF approaches, thus enabling a comprehensive and layered approach.

Based on SIA analysis, critical applications of semiconductor technology across ten sectors of the economy collectively account for 30% of semiconductor demand in the U.S., or 8% of global demand. Looking further, 26% of this demand in "critical applications" is for memory and storage (13% for DRAM, 13% for 3D-NAND), 55% is for logic (or 30% for advanced node logic),

[7] SIA's response to this question should not be interpreted as an association position on any specific project. SIA will not be involved in advocacy in support of any individual project.
[8] Coined by the Cyberspace Solarium Commission: https://www.solarium.gov/public-communications/supply-chain-white-paper
[9] Department of Defense, Securing Defense Critical Supply Chains, https://media.defense.gov/2022/Feb/24/2002944158/-1/-1/1/DOD-EO-14017-REPORT-SECURING-DEFENSE-CRITICAL-SUPPLY-CHAINS.PDF (p. 37-38)

and 19% is for discrete, analog, and optoelectronics (DAO) chips.

CRITICAL APPLICATIONS
(coverage of all semiconductor needs)

End market	Subset of end market application considered as "critical"	% of US semi consumption
Aerospace & Defense	• All	3%
Industrial & Commercial devices	• Medical/healthcare • Energy • Security • Transportation • Industrial automation systems (advanced logic only)	4%
ICT infra: Networks	• Carrier infrastructure • All semiconductors for enterprise networks deployed in critical infra & essential industries (e.g. telecoms, energy, transport, banking...) and all advanced logic for all other networking applications	6%
ICT infra: Computing	• Government data centers (servers & storage) • All semiconductors for servers & storage for critical infra & essential industries (e.g. telecoms, energy, transport, banking...) and all advanced logic for all other datacenter applications	17%
	Total % of US semi consumption deemed as "critical" :	30%

1. Includes consumer electronics and smartphones
Sources: BCG analysis with data from Gartner, IDC and IHSMarkit

In reviewing applications for grants under the CHIPS Act, Commerce can consider how each segment and node size contributes to critical industries in the U.S. The following is an overview of the various critical needs that different semiconductor segments address:

- **Advanced Logic:** These chips are essential for national security and supply chain resilience, and Sec. Raimondo has noted the crisis of advanced logic in the U.S. with no domestic facilities able to operate at the leading edge. Key technologies of the future, such as AI, 5G, cloud computing, and autonomous driving, rely on these advanced semiconductors, which account for 34% of total U.S. semiconductor demand.[10]
- **Mainstream Logic:** These larger-node logic chips, such as microcontrollers, image sensors, and connectivity chips, are necessary for critical applications like automotive manufacturing, aerospace, robotics, and other industrial goods. These chips may also perform ancillary functions in networking, computer, PC, smartphone, and datacenter applications. Insufficient capacity for mainstream logic is a leading contributor to the broader chips shortage in downstream sectors, and capacity expansion in this technology area should be a central goal for the CHIPS act.
- **Advanced DRAM Memory:** High-end DRAM demand for national security and critical infrastructure is driven by applications in AI, datacenters, and supercomputing. Currently, 13% of U.S. semiconductor demand is for memory chips, with a significant portion of those chips used in data-intensive applications like data centers. This demand is expected to expand by over 9% through 2024, highlighting the need for expanded capacity.
- **Analog:** This category, which includes power electronics, radio frequency, and imaging and sensor semiconductors, is essential for current and future critical applications, such as electric vehicles, data center power management, 5G communications, and military

[10] SIA, Strengthening the Semiconductor Value Chain in an Uncertain Era, https://www.semiconductors.org/wp-content/uploads/2021/05/BCG-x-SIA-Strengthening-the-Global-Semiconductor-Value-Chain-April-2021_1.pdf (p. 47)

radar. Given the importance of these analog technologies for defense, aerospace, and national technology leadership, and the diversity of technologies in the analog space, we project that as global production capacity for analog rises, it is critical that the U.S. maintain a minimum of 20% of the global analog capacity in order to establish a viability baseline for these key sectors.

In addition to the critical applications needs defined above, the U.S. also has a significant shortage of capability in packaging. Innovations in how semiconductors are packaged have enabled the global semiconductor industry to achieve additional advancements on top of those traditionally gained during the "front-end" manufacturing process. Many packaging technologies exist today and selecting the correct one is no longer an afterthought but an integral part of semiconductor manufacturing. Unfortunately, the U.S. holds only a 9.48% share in the global advanced packaging market at $3.2 billion in 2021; meanwhile, China is forecast to reach $14.3 billion by 2026.[11]

4. *Based on the criteria outlined in Section 9902 of the NDAA, what do you see as presenting the biggest challenges for an organization to develop an application for funding as part of a consortium, and how long do you estimate it would take for an organization to prepare the required materials?*

There are many challenges in preparing an application, including:

- **Scope of work:** This includes determining technology focuses, up-front costs, annual costs, building and equipment costs, personnel requirements, and the nature of partnerships.
- **Value proposition:** Is the time, effort and expense involved in planning worth the potential outcome? How quickly will the investment pay off? Will it be a game-changer, or just improve the status quo marginally? Are there sufficient resources on hand to make this long-term bet?
- **Intellectual Property:** How will IP rights be organized?
- **Contracting:** As mentioned elsewhere in this response, using OTA will ease contracting challenges considerably by facilitating participation by "non-traditional" USG contract performers, such as non-profits, SMEs, and start-ups.

Regarding, the length of time required to prepare and file the required materials for applications for financial assistance, this will depend on the level of detail imposed by Commerce. See the end of the response to Question #8 for more details on the preparation necessary to plan and commence a project.

[11] *Business* Wire, Semiconductor Advanced Packaging Global Market Trajectory Analytics to 2026, https://www.businesswire.com/news/home/20220121005417/en/Semiconductor-Advanced-Packaging-Global-Market-Trajectory-Analytics-to-2026-IoT-Ecosystem-to-Rev-Up-Opportunities-in-the-50.6B-Industry---ResearchAndMarkets.com

Finally, flexibility on the proportion of U.S. government support (as opposed to a U.S. government match that cannot exceed a fixed percentage of the overall program) will impact how effectively a company can develop a viable program. This proportion ought to be driven by a dynamic factors like national and economic security implications, as opposed to arbitrary caps.

5. *Subject to the criteria and eligibility requirements outlined in Section 9902 of the NDAA, what other factors should the Secretary consider as important when reviewing applications for Federal financial assistance?*

The criteria and eligibility requirements set forth in Section 9902 of the NDAA generally set forth the appropriate criteria to guide Commerce in reviewing applications and making awards of financial assistance. These requirements offer a balanced approach to protecting taxpayer dollars and maximizing competitiveness as they currently stand, so Commerce should strive to implement standards no more or less stringent than the criteria laid out in law. The statutory criteria generally enumerate the relevant factors for Commerce to consider in making financial assistance decisions that will advance the economy, national security, American technology leadership, and supply chain resilience of the U.S. Additionally, companies throughout the semiconductor ecosystem should be eligible for grants, whether headquartered in the U.S. or an allied country.

Specifically, SIA agrees with the eligibility criteria in Section 9902(a)(2)(B), including the requirements to (i) make commitment to worker and community investment; (ii) secure educational and workforce training commitments from certain entities and institutions; and (ii) develop an executable plan to sustain the facility long term without financial assistance beyond the initial incentives. SIA stresses that access to adequate technical talent is key to effectively operating viable projects and developing a strong ecosystem that produces the anticipated benefits. We also support the provision in Section 9902(a)(2)(C) that prevents Commerce from providing financial assistance unless, as noted earlier, the project "is in the interests of the United States" and the applicant for that project has shown that it is responsive to, among requirements, "the national security needs or requirements established by the Intelligence Community (or an agency thereof)" or "the Department of Defense."

In reviewing applications for financial assistance, additional factors may also be considered. For example, the Secretary may consider the overall economic impact of the project, including job creation and other factors. Similarly, the Secretary should consider evidence of the applicant's capability to perform the task(s), as evidenced by past investments in U.S. semiconductor manufacturing facilities and prior success with this type of project. Another consideration may be the potential benefits to supply chain resilience and U.S. and North American-based OEMs/end-users, including how an investment would benefit final products assembled in the U.S and support from U.S.-based end-users in the public or private sectors. Finally, the

evaluation should include the potential for the project to complement the Advanced Packaging Manufacturing Program, National Semiconductor Technology Center, or other CHIPS Act Programs: The Secretary should consider how investments would leverage other federally funded programs through the CHIPS Act to ensure the maximum benefit of taxpayer funds. Finally, another important issue for Commerce consideration relates to the timing of projects that would be eligible for CHIPS grant funding. There are many uncertainties around when the funding bill will be passed, when Commerce will provide initial guidance on the grant application process and issue a Notice of Funding Opportunity, and when companies will have acquired appropriate state and local incentives. As a result of these uncertainties, companies may have a challenge defining the new, expansion, or modernization projects for which they apply. If Commerce rules prevent companies from starting a project before a grant award is made, then companies may delay the immediate investments that are be needed if the current chip shortage is to be curbed.

To that end, the Commerce Department should state that projects that are shovel ready or currently underway that meet the goals of the CHIPS Act should be eligible for funding. Specifically, Commerce should state that companies can order and pay for equipment and/or accept delivery of equipment prior to the awarding of a grant. While companies would not know if, or how large, a grant might be awarded, such guidance would provide companies with clarity as they prepare their CHIPS applications while encouraging companies to make investments as quickly as possible. (See the response to question #8 for more details about this point in the context of making input purchases.)

6. *Section 9902 defines a covered entity to include, among other things public-private consortia, which could include partnerships between semiconductor firms and customers, suppliers, investors, state and local governments, federally funded research and development centers (FFRDCs), and other entities. How can Section 9902 incentives be designed and deployed to encourage additional and new private capital investment in the semiconductor ecosystem? What can be learned from other technology infrastructure development programs that use such partnerships (e.g., data center facilities or communications infrastructure) that may be applicable to semiconductor facilities?*

SIA agrees that public/private consortia can leverage resources provided by multiple parties to tackle complex and expensive technology challenges that may otherwise remain unfunded. As one example, the RAMP-C program has established a partnership between large fabless design companies, foundry and EDA tool vendors, each investing a majority of their own resources to enable the entire CHIP process in the U.S. at state-of-the-art nodes. Furthering investment in this program can encourage more investment from the participants. Indeed, some participants in the RAMP-C program elected to join the consortium based on the expectation that funding from the CHIPS Act would help advance the program.

7. *How can federal financial assistance, consortia, or public-private partnerships be structured to maximize the initial scale of projects and to ensure ongoing reinvestment in project expansions, tool upgrades, and productivity improvements for the projects to remain economically viable and competitive over time? What opportunities exist for manufacturers to partner with private capital providers or use project financing to maximize the impact of the Federal financial assistance awards to achieve these objectives?*

To maximize impact, incentives should be targeted at semiconductor manufacturing and production capacity. Incentivizing core fabrication activities will stimulate growth in the related materials, parts, equipment areas that are required to sustain fabrication. Additionally, given the dramatic increase in the cost of newer semiconductor technologies, leveraging private capital providers is often an attractive way to accelerate the expansion of the U.S. semiconductor industry. Providing CHIPS Act grants for semiconductor projects within the United States will make it more attractive for private capital providers to invest in our domestic industry. Foreign direct investment (FDI) plays a critical role in U.S. semiconductor innovation, totaling $58B in 2020, and it is critical that the U.S. leverage every tool in its policy tool box to attract such capital flow.[12] By reducing business risk, CHIPS Act grants effectively "unlock" additional private capital investment. CHIPS Act grants level the playing field for private capital investors who might otherwise invest abroad or in other industries, making U.S. companies both more competitive and more attractive to private capital investment.

Moreover, to incentivize ongoing investments that require continuous capital injections and to further attract private capital providers, the single most important action is for Congress to provide tax credits for semiconductor manufacturing and design to supplement federal financial assistance under the CHIPS Act. CHIPS funding and tax credits are parts of a complementary, holistic strategy, and both are needed to produce robust, predictable, and durable incentives to restore U.S. semiconductor leadership. The original bipartisan CHIPS for America Act in the 116th Congress (S.3922/H.R.7178) included both direct grants and a tax credit for semiconductor manufacturing facilities and equipment. When the CHIPS programs were authorized as part of the FY 2021 NDAA, its tax provisions were removed for procedural reasons. Grants and tax credits for semiconductor manufacturing and design reinforce each other to enhance industry competitiveness and provide a holistic incentive framework. Grants provide a targeted, one-time incentive for manufacturing, facility, and equipment upgrades, while tax credits covering both manufacturing and design offer an ongoing, predictable incentive to continue the significant ongoing capex and opex investments needed to construct, upgrade, operate, and expand new and existing facilities and engage in advanced design to strengthen the entire ecosystem. The Senate first introduced a stand-alone manufacturing credit with the Facilitating American Built Semiconductors (FABS) Act (S. 2107),[13] and the newly

[12] Foreign Direct Investment in the United States, Global Business Alliance, 2021

[13] https://www.congress.gov/bill/117th-congress/senate-bill/2107?q=%7B%22search%22%3A%5B%22fabs+act%22%2C%22fabs%22%2C%22act%22%5D%7D&s=1&r=1

introduced and bipartisan House bill (H.R. 7104) improves this legislation by including a design credit.[14]

To further complement tax credits for semiconductor manufacturing, adjustments may be needed in laws and regulations governing free trade zones to allow, to the fullest extent possible, duty-free imports of components needed to stand up and operate facilities funded by the CHIPS Act. Doing so would help address the capital and operational expense challenges that have been factors in creating vulnerabilities in the U.S. supply chain.

Additionally, the size of leveraged funding is crucial to encouraging maximum private participation in semiconductor manufacturing and research projects. In particular, it is important that funding, both public and private, will be available over the time needed to construct facilities or commercialize technology. The complexity of semiconductor technology and its entire development cycle, plus the costs of R&D and prototyping, cause the dollar value of the funding available and the long-term prospects of continued funding to be critical to encouraging private sector participation. It takes many years and dollars to research, develop, prototype, transfer to foundry, package, and ship semiconductors to market. Thus, the size and certainty of funding are critical to enabling scalability and to continued investment. Commerce could also consider that offering grants to expand existing facilities may yield greater short-term increases in capacity, while the impact of grants for greenfield facilities may manifest over the longer term.

The experience of the Defense Advanced Research Projects Agency (DARPA) can provide a useful model for establishing a CHIPS Act program for investing in research results. DARPA has participated as a partner in the research consortium JUMP which has sponsored research at many universities. DARPA has taken some of the research results of particular interest and transferred them into existing DARPA programs. DARPA's action has not only benefited the potential value of its existing programs, but it has enhanced the prospects for commercialization of those research results. We note, however, that where DARPA has focused on technologies for low volume production intended to meet defense needs, the CHIPS Act efforts should aim for technologies that will ultimately be scaled to much higher volumes and provide commercial sector benefits.

In a similar way, a CHIPS Act program would establish an investment fund in the NSTC under § 9906(c)(2)(B) that would invest in the further development and commercialization of the research results from other CHIPS Act programs. The fund could stand alone or be integrated into various CHIPS Act programs. As a not-for-profit fund, it would be guided in its investment decisions by the research sponsors. This would ameliorate the so-called valley of death for the research results, promote the development and commercialization of the research and provide a validation for other private equity funding.

[14] https://www.congress.gov/bill/117th-congress/house-bill/7104/text

Finally, as noted in Question 4, the Secretary should consider differences in initial capital requirements and operating expenditures for additional manufacturing capacity of different sectors in the semiconductor supply chain when developing the appropriate federal contribution for proposed Section 9902 funding requests. National security and economic considerations suggest that the Secretary should not employ an arbitrary approach to determine the amount of federal contribution offered for a proposed Section 9902 funding request. Rather, discretionary considerations are needed to determine the amount of federal assistance offered, and these must be done on a case-by-case basis.

8. *How can Federal funds incentivize the creation of a broad semiconductor ecosystem that includes producers of semiconductor manufacturing equipment and other upstream suppliers? What are the largest supply imbalances with respect to manufacturing equipment, tools, materials, and chemicals that need to be addressed by US investment?*

To strengthen the U.S. semiconductor ecosystem, it is desirable not only to invest in expanding the number of fab facilities in the United States but also to pursue the mutual growth of materials, parts, and equipment suppliers.

The CHIPS Act was broadly drafted to define a "covered entity" as "a facility relating to fabrication, assembly, testing, advanced packaging, or research and development of semiconductors." This term has been intended to encompass semiconductor fabs, packaging facilities, and research facilities, as well as facilities producing equipment and materials necessary for the fabrication of semiconductors. The House-passed America COMPETES Act (H.R. 4521) amends this language and clarifies this intent by expressly defining a covered entity to include "semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment." SIA supports this amendment to ensure Commerce may include consideration for funding of key parts of the entire ecosystem.

In extending eligibility for financial assistance to equipment and materials, Commerce should focus on key gaps and vulnerabilities in the ecosystem. The following are among the most notable of these vulnerabilities.[15]

Semiconductor manufacturing uses over 50 different types of sophisticated wafer processing and testing equipment for each step in the fabrication process. However, while U.S. firms collectively account for more than a 50% share of the global market in five of the major manufacturing process equipment categories, the domestic industry remains reliant on foreign suppliers in a few critical areas:

- **Substrates and Substrate Materials:** Substrates, panels of resin embedded with wiring onto which central-processing units and other types of chips are attached, are foundational in producing a finished chip. While these specialty materials only account

[15] See SIA response to Commerce's April 2021 Supply Chain RFI: https://www.semiconductors.org/wp-content/uploads/2021/04/4.5.21-SIA-supply-chain-submission.pdf (p. 20-23)

for a tiny portion of the industry's total value added, semiconductors cannot be fabricated without them.

- **Photoresist:** The polymer coating which is cured via lithography to pattern the chip design on the wafer substrate. Coating and developing equipment. This equipment is vital to the lithography process, with >90% originating from outside the U.S.
- **Lithography:** Machines that transfer chip design from the mask set to the wafer, key lithography technologies include dry lithography, immersion lithography, and extreme UV lithography. Key firms for lithography are Nikon, Canon, and ASML.

Additionally, the industry relies on certain materials, chemicals, and gases for which there are no known alternatives. Even limited losses in these supplies can cause much larger indirect losses throughout the industry:

- **Process chemicals:** Sales of C4F6, which are particularly critical for certain advanced memory and logic chips, were approximately $250 million in 2019, with the top three suppliers located in Japan (40% of global supply), Russia (25%), and South Korea (23%), and severe disruption in any of these suppliers could constrain NAND production levels for 2-3 years.
- **Wet chemicals:** The low profits of the wet chemicals supply-chain (HF, H2SO4, HCL, H2O2, H3PO4, NH4OH) limits the incentive for North American chemical manufacturers to expand or maintain operations.
- **Industrial gases:** Semiconductor manufacturing requires the use of a range of gases, some of which are sourced from countries of high geopolitical risk.
- **Commodity chemicals:** Fabs also use commodity chemicals that may be produced by a wide range of suppliers. However, the semiconductor industry requires high purity chemicals (e.g., HCl, IPA, etc.) where there is a smaller group of qualified suppliers.
- **Sputtering targets:** Sputtering targets are used to form the barrier and seed layers in transistor interconnects, but there are few sputtering target manufacturers located in the U.S., and only one capable of production for the most advanced chips.

Correcting these supply imbalances for equipment and materials, however, requires that semiconductor companies be able to send strong demand signals to their suppliers. As mentioned in the response to question #5, with companies trying to plan for expansion using CHIPS funds and uncertainty around when monies will be appropriated, an issue facing many chip makers is the exceedingly long lead times for the aforementioned critical inputs – now sometimes exceeding 24 months. If CHIPS awards are not made until later this year, these lead times could delay completion of new or expanded fabs. To ensure timely completion, many manufacturers will need to place binding orders for construction materials/equipment in the coming months without any assurance that they will receive CHIPS funds to complete the process.

Historically, Commerce has granted pre-approval for pre-award costs to be used toward grant expenses ultimately covered by the covered project. It is critical that Commerce implement

rules to such ends for the CHIPS Act as well, so the supply and demand for critical semiconductor equipment and materials can be accurately predicted and provided for.

9. *How can the program ensure that semiconductor startups and small and midsized companies have access to commercial fabrication, assembly, testing and packaging facilities and associated technical expertise, including intellectual property products such as "Process Design Kits"?*

Semiconductor startups and small/midsized companies are key parts of the innovation ecosystem. SIA believes these companies' needs can best be addressed through the NSTC.

Many semiconductor startups struggle to survive the "valley of death" in prototyping and piloting. This term refers to the phenomenon where potentially groundbreaking technologies cannot be commercialized due to the high investment needs, technical challenges, and ecosystem infrastructure limitations smaller companies (and even many large companies) face. A primary purpose of the NSTC is to increase access to advanced facilities and equipment, so the costs of prototyping and piloting need not be borne by players that could otherwise not afford it. Additionally, by creating hubs of semiconductor research, it also provides participating companies with access to the industry's leading experts.

10. *Under the law, the Secretary may consider whether a covered entity includes a small business concern as defined under Section 3 of the Small Business Act (15 U.S.C. 632). Would it be beneficial for the Department to encourage large entities to partner with medium and small business suppliers?*

Yes, small and medium businesses and large businesses often work together in complementary ways. For example, small/medium size businesses often have deep expertise in particular technology areas but lack networks of potential clients or program management skills that would enable them to handle large projects. Conversely, large businesses often have general technology skills but also deep expertise in program management or running complex projects and organizations. Large businesses can also provide funding stability which can be very important to small organizations.

Bringing these two types of organizations can be mutually beneficial, as the large companies' organizational heft, program management skills, and networks can help fill small and medium businesses' skill, personnel, and continuity gaps. At the same time, small and medium companies can provide targeted expertise to complement the more general skills of the larger company, improving the latter's agility.

11. *Section 9902 requires a covered entity to make commitments to invest in workers and communities, including through training and education benefits and programs to expand employment opportunity for economically disadvantaged individuals. What constitutes a baseline commitment to worker training in the semiconductor industry and what other workforce investments should be considered? Are there international best practices or*

cooperation upon which your company finds beneficial? What other community investments should be considered beyond worker training and employment opportunities? How can worker training, other workforce commitments, and other community commitments be maximized and how should program participants be held accountable to their commitments? What types of programs exist, or could be expanded, to improve access for economically disadvantaged individuals to these workforce and community commitments and opportunities?

In evaluating whether an applicant has made a sufficient commitment to worker and community investment, Commerce should consider: (1) existing and planned internal workforce development efforts and (2) the applicant's demonstrated commitments to its surrounding community and local partners.

First, Commerce should assess the applicant's current training programs and educational benefits, as well as those proposed by the applicant in connection with the proposed project. The current training initiatives employed by an applicant such as apprenticeship or internship programs demonstrate the applicant's commitment to developing a skilled pipeline.

Second, Commerce should also assess the applicant's external commitments to workforce development including training programs and focused efforts on recruiting and attracting underrepresented individuals in the semiconductor industry. Commerce can assess the impact of these efforts in terms of the quantity of programs or training provided, the potential number of individuals participating in or impacted by the efforts, or the number of individuals the applicant seeks to employ in apprenticeship or internship type roles. Given the array of approaches to achieving these community and workforce investment goals, Commerce should not prescribe or prioritize a particular type of effort, but instead evaluate the effectiveness of the proposed effort and require applicants to commit to these efforts as a part of the award requirements.

Please refer to Question #9 under the NSTC section and to the workforce section for additional details regarding this question.

12. *Section 9902 requires a covered entity to have secured commitments from regional educational and training entities and institutions of higher learning to provide workforce training to be eligible for funding. Looking at the semiconductor sector broadly, what are the greatest workforce development needs, and how can Federal financial assistance meet those needs? What specific types of workforce training programs would be the most beneficial to companies in these sectors? What existing workforce training programs have proven effective and should be expanded, including international exchanges or best practices? How could a program best ensure that workforce training and development meet critical national needs?*

To support long-term growth of the domestic semiconductor industry, skilled individuals will be needed in an array of positions. Semiconductor jobs are split across a range of occupations,

with the largest two segments being production occupations – such as factory technicians and line workers – at 38 percent and engineering occupations – such as electronics and electrical engineers and chip design engineers – at 26 percent.

Given this employment profile, the semiconductor industry requires talented and qualified workers throughout the educational spectrum. In the research and design stages of the process, the industry requires the best and brightest scientists and engineers with advanced degrees in the STEM fields. Engineers with such education remain in short supply in the U.S. workforce as the semiconductor industry competes with other powerhouse software companies who have more consumer facing brands engineers are more familiar engaging with. Engineers without such education cannot acquire it by on-the-job training, or by a short course in a vocational setting. These skills can only be acquired in the course of a multi-year, structured academic program that, in turn, relies upon the engineer-to-be already having the requisite math and physics academic building blocks. Access to these highly educated engineers is critical to the development of our future generation of products and technology and to our ability to maintain the US semiconductor industry as the global leader.[16]

- *Attracting and retaining U.S. semiconductor talent*
  There is bipartisan support for reforming current green card policies for highly skilled immigrants, and strong government leadership is needed to make progress on this issue. The government should act swiftly to end per-country green card caps and exempt advanced STEM degree graduates of U.S. universities from existing green card caps.
- *Drastically increasing the pipeline of diverse and underrepresented minorities in U.S. STEM students interested in semiconductor fields*
  STEM education programs should be rigorously evaluated, and funding should be allocated to scale up successful models for broader implementation. Several government-funded programs, and industry funded programs, are available that seek to strengthen the pipeline of U.S. STEM talent, and these are ripe for larger investments to expand their impact. For example, the Department of Defense's Scalable Asymmetric Lifecycle Engagement (SCALE) program is a public-private-academic partnership that supports university engineering departments and matches participating students with private sector employers. While the program first received seed funding from DOD's Trusted & Assured Microelectronics in FY 2019, the 2021 report by the National Security Commission on Artificial Intelligence (NSCAI) recommended fully funding the production phase of SCALE at $24.7 million per each of its five technical verticals over five years.
- *Supporting existing industry programs that produce highly and specially trained talent for the semiconductor industry.* Several programs, such as the university research

[16] SIA, NIST Workforce RFI, https://www.semiconductors.org/wp-content/uploads/2018/11/NIST-workforce-RFI-august-2018.pdf (p. 5)

programs managed by the SRC, have proven their capability over many years to produce university-trained talent for the semiconductor industry. Supporting such existing mechanisms through CHIPS Act programs, rather than inventing new mechanisms, can be highly effective for the semiconductor industry.

- *Leveraging federally funded R&D to develop the domestic semiconductor workforce* Increased federal investment in semiconductor research is critical in addressing the future workforce in the industry. Government investment in semiconductor research provides the "pipeline" of highly educated talent that can drive innovation in the semiconductor industry for decades to come. Federally funded projects provide learning opportunities and experience that firms cannot provide or fund on their own (e.g., Exascale, Quantum Computing, or Electronics Resurgence Initiative programs). Unfortunately, federal investment in research relevant to the semiconductor industry has been flat or declining in recent years. This decline in federal research investment is particularly harmful given that our global competitors are increasing their commitment to funding research, placing U.S. leadership in the semiconductor industry at risk.
- *Expand training programs for technicians.* Semiconductor facilities and equipment require constant maintenance and repair on a twenty-four hour, seven-day-a-week basis. Creating and funding programs of advanced technical training, especially in collaboration with junior colleges, could facilitate on an expedited basis the expansion of semiconductor manufacturing in the United States.

13. *What is the industry's environmental footprint in terms of its land and resource use, air quality and water quality impact, hazardous or other special-handling material needs, and greenhouse gas emissions impact? What is the industry currently planning or implementing on these dimensions and how will the environmental footprint likely change over the next decade as a result? What effect will semiconductor chip customers' "net zero" announcements or other related incentives have on the industry's environmental footprint? What opportunities exist for the industry to move to a smaller and more sustainable footprint, and how can such opportunities be used to create a stronger domestic market for chips produced with a smaller footprint?*

The complex process of fabricating semiconductors results in a range of environmental impacts, and the increasing process complexity associated with fabricating more advanced chips will pose challenges in reducing these impacts. While a detailed overview of the environmental footprint of the industry is impossible within the scope of this RFI response, a high-level summary includes the following.

Climate – Semiconductor manufacturing is a relatively minor contributor to emissions of global warming gases (Scope 1 emissions). In the U.S., data from the Environmental Protection Agency indicates the industry accounts for approximately 0.2 percent of overall emissions from industrial sources, which comprise 22 percent of overall U.S. emissions). These emissions are primarily from the use of perfluorocompounds (PFCs) and other fluorinated greenhouse gases, a category of high-intensity global warming gases, during the fabrication

process. The complex process of fabricating semiconductors at the nanoscale requires the use of gases with very specific chemical and physical properties, but many of these gases have long atmospheric lifetimes and are potent greenhouse gases. Unfortunately, there are no known substitutes for these gases, and advancements in transistor density and process complexity necessitate the increased use of many of these gases.

The global semiconductor industry, under the auspices of the World Semiconductor Council (WSC), has voluntarily worked to reduce emissions of PFCs for over two decades. In the late 1990s the industry set a goal of reducing emissions by 10 percent by 2010, and in 2011 the WSC announced it far surpassed this PFC reduction goal, achieving a 32 percent reduction in PFC emissions despite rapid industry growth and increasing product complexity.[17] The WSC set a new 10-year voluntary goal calling for the implementation of best practices in new fabs.[18] The industry has implemented these best practices and successfully reduced its normalized emissions, although progress in achieving further emissions reductions has slowed due to a number of technical challenges.

At the same time, technologies enabled by semiconductors have the potential to make significant contributions towards solutions to global climate change. The deployment of information and communications technology (ICT) throughout the economy can achieve dramatic improvements in energy efficiency and the production of clean energy. According to the World Economic Forum, semiconductor-enabled technologies such as digital technologies can reduce greenhouse gas emissions by 15 percent - almost one-third of the 50 percent reduction required by 2030.[19]

To achieve further reductions in the climate impact of semiconductor manufacturing, SIA calls for research on alternative gases and materials in the fabrication process that have reduced global warming potential compared with current processes, while still meeting the functional requirements of the industry. In addition, research will be needed on further improvements to the energy efficiency of semiconductor devices.[20]

Chemicals –Semiconductor device manufacturing is the process used to fabricate integrated circuits for use in electronic devices. The semiconductor manufacturing process has been

[17] Joint Statement of the 15th Meeting of the World Semiconductor Council, available at http://www.semiconductorcouncil.org/wp-content/uploads/2016/07/WSC_2011_Joint_Statement.pdf

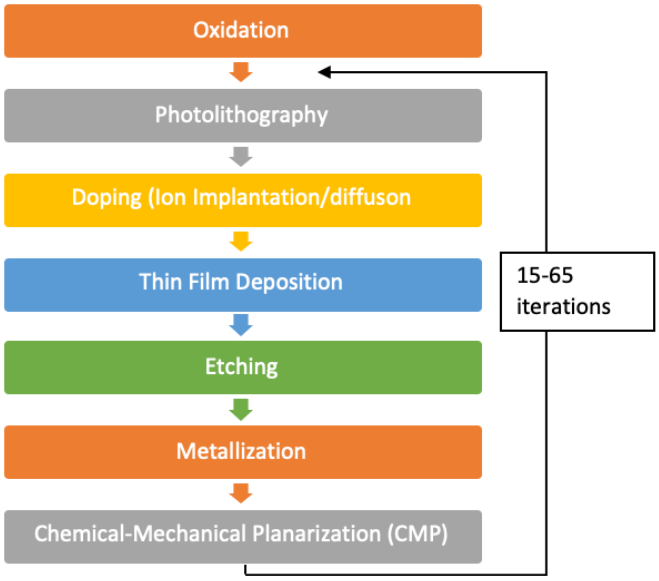
[18] World Semiconductor Council "Best Practice Guidance for Semiconductor PFC Emission Reduction" (May 18, 2017) available at http://www.semiconductorcouncil.org/wp-content/uploads/2017/07/Best-Practice-Guidance-of-PFC-Emission-Reduction.pdf

[19] World Economic Forum, Why Digitalization is the Key to Exponential Climate Action, https://www.weforum.org/agenda/2019/01/why-digitalization-is-the-key-to-exponential-climate-action/

[20] Semiconductor Research Corporation (SRC), The Decadal Plan for Semiconductors, available at https://www.src.org/about/decadal-plan/. The plan identifies the need for new computing paradigms to dramatically improve energy efficiency as one of the five "seismic shifts" facing the industry.

recently reviewed in two OECD documents.[21,22] In general, the basic steps in semiconductor manufacturing are depicted in Figure 1.

Figure 1. Basic steps in semiconductor manufacturing



The process involves hundreds of carefully controlled steps to deposit, modify, and remove chemicals – in exactly the right amount, in exactly the right place, at exactly the right time – on a thin silicon wafer to create numerous patterned layers of the integrated circuit, typically many thousands of times thinner than that of a human hair. To achieve the precision of semiconductor manufacturing and satisfy rigorous performance needs, the fabrication process requires the use of specialized liquids, solids and gases that possess chemical and physical properties needed to satisfy rigorous performance needs. The fabrication process uses these chemicals under rigorous conditions with extensive and typically redundant controls. Modern high-volume manufacturing fabs use enclosed, interlocked, ventilated, and automated manufacturing equipment (tools) which separate employees from the product wafer and process chemicals and route tool exhaust to the appropriate fab abatement equipment when necessary.

Chemicals such as sulfuric acid, hydrochloric acid, hydrofluoric acid, ammonium fluoride, tetramethyl ammonium hydroxide, and hydrogen peroxide are used in high volume. But some of the chemicals used by the industry, such as Per- and polyfluoroalkyl substances (PFAS), have been identified as being of concern in terms of environmental and health impacts. As summarized in a paper to be published shortly, “Fluorochemicals in lithographic patterning and semiconductor processing: Chemical and environmental considerations” by

[21] EMISSION SCENARIO DOCUMENT (ESD) ON CHEMICAL VAPOUR DEPOSITION IN THE SEMICONDUCTOR INDUSTRY. ENV/JM/MONO (2015)5

[22] EMISSION SCENARIO DOCUMENT ON PHOTORESIST USE IN SEMICONDUCTOR MANUFACTURING (as revised in 2010). ENV/JM/MONO (2004)14/REV1

Professor Ober of Cornell University and colleagues, "[t]he use of fluorochemicals in lithography and semiconductor patterning plays a critical role in the success of semiconductor technology." Prof. Ober and his colleagues state: "The addition of small quantities of fluorinated materials enables patterning capabilities that are otherwise not possible to achieve and this leads to superior device performance. The compact size of the fluorine atom and its strong electron withdrawing characteristics make it stand out in the periodic table and gives fluorocarbon materials unique properties, unmatched by other chemical compounds."

While the industry continues to use chemicals in its operations it has made great strides in phasing out specific chemicals of concern, such as elimination of long-chain PFAS. Under the auspices of the World Semiconductor Council (WSC), the global semiconductor industry in 2017 announced it successfully phased out uses of PFOS, and the industry is now working to eliminate uses of PFOA by 2025.[23] Further reductions will require research into new detection and treatment methods for the use of these chemicals, and over the longer-term research on more environmentally benign alternatives that meet the industry's performance requirements.

Air – As with any industrial operation, semiconductor fabrication results in air emissions subject to various federal, state, and local permit requirements. Fabs are equipped with acid, base and solvent systems. Acid and base exhaust systems are treated via wet scrubbers prior to discharge. The solvent exhaust system is typically abated using a rotary concentrator thermal oxidizer. There are currently no semiconductor fabs in the U.S. designated as "major sources" of hazardous air pollutant emissions.

Water – The major use of water in a semiconductor manufacturing facility is the production of ultrapure water (UPW) which is used in the manufacturing process. Semiconductor facilities have minimized chemical consumption in the production of UPW by replacing membrane systems with ion exchange. Reverse osmosis (RO) systems have been optimized to reduce the amount of reject water. RO reject water and reclaimed industrial wastewater is used as the source of water for scrubbers, cooling towers and landscape irrigation.

The industry also discharges wastewater, in most cases to local wastewater treatment plants. Waste segregation and wastewater treatment practices vary based on the processes that occur in the manufacturing facility and local discharge limits. SIA conducted a survey of their members to identify wastewater treatment methods. All respondents send process wastewater containing inorganic liquids to industrial waste treatment systems for elementary neutralization (pH adjustment). Facilities may segregate specific inorganic wastes if required to meet local limits established for the POTW based on the receiving water quality or if a specific waste stream can be cost effectively reused or recycled. Inorganics which may be collected and treated/recycled include:

[23] See WSC Joint Statement available at http://www.semiconductorcouncil.org/wp-content/uploads/2018/05/22nd-WSC-Joint-Statement-San-Diego-CA-FINAL-1.pdf.

- Ammonia containing waste for treatment or recovery,
- Fluoride treatment/removal via precipitation,
- Phosphoric acid collection for offsite recycle or disposal,
- Concentrated copper metallization solutions[24] for onsite or offsite treatment/recovery, and
- Dilute copper containing wastewater for treatment via carbon adsorption and ion exchange, or flocculation and precipitation.

Direct dischargers have additional waste treatment such as metals precipitation, hydrogen peroxide destruction, ammonia segregation for treatment or recovery, biological treatment for organics and ammonia, and chlorination/dechlorination.

Waste –Waste segregation practices vary based on Federal and state requirements. All facilities have dedicated solvent (organic) waste drains and collection systems. The makeup of the solvent waste stream varies widely based on the ability of the facility to cost effectively segregate specific solvent wastes to be sold as a product or for recycle. Organic waste which may be collected for recycle/reuse include isopropyl alcohol and n-methyl pyrrolidone (nMP).

The industry is continually working towards improving its environmental profile, but more research will be needed to address some of the key challenges. For example, to facilitate semiconductor manufacturing in the U.S. while achieving our environmental protection goals, research is needed in alternatives to certain critical chemicals with an improved EHS profile, as well as research on effective treatment technologies to minimize the risks of continued use of these chemicals. Similarly, in order to grow semiconductor manufacturing in the US while continuing to meet our climate reduction goals, research is needed on alternative gases with lower global warming potentials (GWPs), alternative processes that reduce emissions of greenhouse gases, and effective abatement devices.

National Semiconductor Technology Center

1. Based on the functions outlined in section 9906 (c) of the NDAA the Department's current vision of the NSTC is as a hub (or multiple hubs) of talent, knowledge, investment, equipment, and toolsets that tackles Moore's Law transitions, post-CMOS research into new materials, architectures, processes, devices, and applications, and that bridges the gap between R&D and commercialization. What attributes are most important for the NSTC to possess or provide to the community (e.g., ease of access, a broad suite of leading edge tools managed as central facility, a collaborative research environment)? What key factors are critical for the NSTC to address the current gaps in the semiconductor R&D ecosystem?

The National Semiconductor Technology Center must implement a far-sighted research agenda that both comprehensively addresses the full stack of research needs and efficiently maximizes

[24] Copper metallization is used on some but not all semiconductor fabs.

the impact of federal investment. The NSTC should focus on strengthening the U.S. R&D ecosystem's ability to research, prototype, and commercialize technologies that are three to fifteen years from production, depending on the technology area.[25] This future focus for pathfinding and exploratory research is important given the extended timelines over which semiconductor R&D occurs –the investments necessary for today's major technological advancements were made years ago. Rather than replicating capabilities currently found overseas, the NSTC should build and strengthen the U.S. R&D ecosystem's capabilities in emerging areas like advanced packaging, heterogeneous integration, and masking infrastructure in which regional leadership has yet to be determined.[26]

Critically, these efforts must focus on technologies that promise fundamental breakthroughs in the industry, not merely incremental improvement.[27] In order to achieve such breakthroughs, the NSTC should encourage the participation from global industry leaders. This will help strengthen the innovative fabric of the United States and ensure the NSTC is a true global leader in its research and development. Beyond the ambition of its goals, the NSTC must also take advantage of its high perch by supporting full-stack innovation. It must convene companies to solve complex technology problems that require collaboration across the full computing stack as all but a few companies are capable of advancing tools, designs, manufacturing capabilities, and packaging single-handedly.[28] This inclusive, full-stack approach is needed for disparate element to combine into a functional new technology,[29] and it must be started from the very beginning of the research and development stage.[30]In particular, NSTC's efforts could focus on areas such as path-finding, advanced node R&D, material exploration for advanced and mainstream nodes, or other fields that require bold investment such as EUV facilities and advanced process integration capabilities. Additionally, NSTC could pursue architecture or process flow innovations at mainstream nodes.

To reach these goals efficiently, the NSTC should leverage existing resources and carefully tailor the distribution of its funds. More will be discussed on the use of current programs in Question #3, but as the NSTC upgrades institutions' capabilities it must ensure that access to prototyping facilities, advanced simulation software, tools, and personnel remain accessible to researchers and startups.[31,32] Furthermore, to steward public investment well, the NSTC must strike a balance between spreading funding evenly and not concentrating investments in a single

[25] Others similarly say the NSTC should focus on the "transition of viable technologies with a 5-10-year horizon to 300mm development and high-volume manufacturing" ("ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 13)
[26] SIA BCG Research Report (Not Yet Finalized)
[27] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 6
[28] SIA BCG Research Report (Not Yet Finalized)
[29] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 11
[30] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 9
[31] SIA BCG Research Report (Not Yet Finalized)
[32] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 10

technology or location.[33] To effectively build a fab-centered R&D infrastructure, it is necessary to co-locate the NSTC hub(s) where existing facilities can be used to the maximum, and to consider the current ecosystem of leading universities and research laboratories. This will be essential to attracting top talent.[34]

The goals of the NSTC are not best defined by the government. Nor should the government attempt to dictate how the goals will be reached. Instead, the government should proceed in partnership with industry and academia to jointly define the NSTC goals and formulate, award and evaluate projects and programs based on technical merit.

As the NSTC sets out to implement its goals, it must address a range of needs both vertically across the stages of research and development and horizontally across semiconductor segments. Vertically, the NSTC must ensure capabilities for pathfinding research, research infrastructure, development infrastructure, collaborative development, and workforce.[35] These resources will in many cases serve generalizable use cases that a range of companies could leverage. One of the most important resources that the NSTC should provide access to is R&D fab infrastructure capability. Access to fabrication and production is necessary to ensure that all participants are able to introduce new custom designs to production and testing. Additionally, however, some NSTC facilities must specialize into ”Centers of Excellence” that focus on advanced memory, fabless design, and analog/mixed-signal technologies, respectively. The response to Question #10 will further elaborate upon this point.

The U.S. semiconductor industry faces a “valley of death” in prototyping and piloting potentially groundbreaking technologies due to the high investment needs, technical challenges, and ecosystem infrastructure limitations these innovations face.

Numerous different U.S. government entities provide public investment in semiconductor R&D. However, while these bodies have critical missions and often take steps to collaborate, their important needs and objectives are still distinct from those of private industry. As a result, gaps may emerge in which adequate R&D investment does not reach the technical areas critical to supporting continued US economic competitiveness.[36] A new federally supported public-private partnership must facilitate this investment by mitigating the development risk for groundbreaking innovations by fostering the infrastructure, multidisciplinary partnerships, and industry-driven agenda necessary to commercialize promising technologies.[37]

Finally, within the framework provided above, certain capabilities will be especially critical:

- Advanced node manufacturing is largely inaccessible to startups, making it harder for U.S.-based semiconductor startups to iterate on and develop their ideas domestically.

[33] SIA BCG Research Report (Not Yet Finalized)

[35] SIA BCG Research Report (Not Yet Finalized)
[36] SIA BCG Research Report (Not Yet Finalized)
[37] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 13

The lack of R&D-related infrastructure hinders the overall ecosystem's ability to provide advancements.[38] To that end, the NSTC must provide access to tools for both large and small companies.[39]

- Accessing wafer starts can be an expensive and difficult task in the transition from laboratory technology to prototyping and very early piloting, so the NSTC could coordinate access for researchers at public institutions as well as large and small companies by purchasing wafer starts for multi-project wafer runs at fabs.[40]

2. As authorized, the NSTC would have to be able to work with a wide range of research groups from industry, academia, and government, some of whom will be contributing valuable intellectual property. What approaches to intellectual property should be in place to protect the foundational contributions of members while enabling maximum collaboration and innovation amongst the research community supported by NSTC? What IP issues create unique challenges for middle- and late-stage prototyping collaborations versus early-stage research, design and proof-of-concept collaborations?

The NSTC's approach to intellectual property should be predicated on industry ownership of and flexible marketplace access to collaboratively generated IP.

To maximize industry participation and remove potential chilling effects on innovation, the rights for IP generated from NSTC-directed research areas should be structured favorably for commercialization by the companies who participated in the relevant research effort. This model is consistent with past federal efforts by agencies like NASA, which agreed to allow companies involved in the Commercial Orbital Transportation Services (COTS) program to retain the IP they generated.[41]

Ownership of IP by NSTC participants is critical to incentivizing private-sector contributions, and it facilitates yet further capabilities for the NSTC. By making collaboratively developed EDA IP available on a cloud-based access-controlled environment, large and small companies could obtain or exchange these design tools as on a marketplace to address their specific needs.[42]

In other circumstances, commercialization of research results can be achieved more widely and promptly by granting non-exclusive licensing rights to the sponsors of the research results. Such companies typically have a need for the technology, have closely monitored its development and are prepared to commercialize it.

[38] SIA BCG Research Report (Not Yet Finalized)
[39] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 10
[40] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 23
[41] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 18
[42] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 14

In any event, the IP rights should be designed for the particular research circumstances at hand by those funding and participating in the research project.

3. The federal government has several programs that support microelectronics and associated R&D across many agencies, federal labs, university labs, corporate labs, and other for-profit and nonprofit entities. What existing domestic R&D activities, assets, intellectual property, knowledge and expertise should be incorporated or otherwise connected to the NSTC, and are any international in nature? How should the NSTC interface with federal labs, university labs, corporate labs and other existing institutions of R&D and prototyping to ensure that R&D projects are supported throughout the technology maturation process so that public research funds are able to improve R&D productivity and attract additional private and venture investment?

University research funding and government programs play substantially different roles in semiconductor research from what is envisioned for the NSTC. Government programs like those of NSF and DOE tend to focus on fundamental research, early idea development, and laboratory proof of concept demonstrations. Universities have a similar focus, and the Semiconductor Research Corporation focuses its support on those institutions. Other government programs like DARPA are project-driven and mission-focused, so the extent to which these support the maturation of a wide range of innovations may be limited. Furthermore, industry focuses mainly on low-risk technologies that have already demonstrated scalability, and only a few large integrated device manufacturers (IDMs)[43] in the U.S. have the resources to bridge this lab-to-fab transition gap.[44]

To support U.S. economic and technological competitiveness most effectively, the NSTC should augment rather than replicate these organizations. In other words, the NSTC should support pre-competitive research and go one step further. The NSTC should bring together research centers across government, academia, and global industry to assess which technologies of commercial interest to companies in the U.S. may need and provide support to bring the technologies to maturation. As mentioned in Question #11, the selection and support for startups in the context of the investment fund should be guided by similar principles.[45]

Coordinating the NSTC with existing resources should be a two-way street. First, the NSTC should leverage existing facilities from across the nation by constructing annexes or rehabilitating fabs to target gaps in the ecosystem. The annex construction approach would be

[43] Semiconductor firms generally organize their activities around the two main stages of semiconductor production: design and manufacturing. Companies that focus only on design are referred to as "fabless" firms, while companies that focus only on manufacturing are called "foundries." Semiconductor firms that do both are called Integrated Device Manufacturers, or IDMs.

[44] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 9-10

[45] SIA BCG Research Report (Not Yet Finalized)

much lower in cost than building greenfield facilities,[46] and these upgrades would become operational much more quickly than brand new centers, offering more immediate access to pathfinding infrastructure for a range of organizations.[47] The NSTC should also seek to coordinate access to its facilities with those of the larger ecosystem by leveraging its connections, and facility access could be considered part of the NSTC's funding award for research priority areas.[48]

Second, applicants for NSTC funds should be asked to show how their covered projects would coordinate with other NSTC-related investments and activities. Applicants should also explain how their projects would interface with other federal research programs, including JUMP, ERI/ERI 2.0, the DOE National Laboratories, NIST's microelectronics and metrology efforts, NSF's National Nanotechnology Coordinated Infrastructure, and other DOD projects (SHIP, RAMP, RAMP-C). Other programs from the FY 2021 NDAA can also leverage the experience of federal agencies. For example, NIST already has experience convening private and public entities to establish industry-wide standards. In 1997, NIST began a decade-long effort with industry and the cryptographic community to develop a voluntary Advanced Encryption Standard (AES), which intended to develop a standard specifying encryption algorithms capable of protecting sensitive government information.[49] The semiconductor industry similarly needs support in standardization as it has specialized to the point where some companies only design the differentiating aspects of a chip's system and therefore do not plan the fabrication of their designs. In order to fully implement and package these multi-faceted chiplets, the National Advanced Packaging Manufacturing Program under §9906(d) should partner with NIST and industry groups to develop standards that support the interoperability of silicon components across the ecosystem. As another example, DOD's response to EO 14017 stressed that the Department should work with industry to develop assurance and security standards for microelectronics that assure both commercial and defense interests.[50]

4. How should the NSTC connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

[46] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 24
[47] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 6
[48] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 23
[49] https://csrc.nist.gov/projects/cryptographic-standards-and-guidelines/archived-crypto-projects/aes-development
[50] https://media.defense.gov/2022/Feb/24/2002944158/-1/-1/1/DOD-EO-14017-REPORT-SECURING-DEFENSE-CRITICAL-SUPPLY-CHAINS.PDF (p. 39)

As programs from the FY 2021 NDAA are set up and receive funding, the NSTC should coordinate its efforts with those of the other government and industry programs.[51]
The National Network for Semiconductor R&D is intended to enable lab-to-fab transition of microelectronics innovations in the U.S. and expand U.S. microelectronics leadership. Towards this, it is instructed to enable exploration of new materials, devices, and architectures and to accelerate transition of novel technologies to manufacturers via domestic prototyping capabilities. These tasks will be best accomplished in close partnership with the NSTC, and likely leveraging the prototyping capabilities that will be created as a part of the broader NSTC and NAPMP efforts. As the primary activities of the NSTC will focus on the prototyping and early piloting stages of technology development, it represents the final destination of laboratory-stage technology developed within the National Network for Semiconductor R&D. Within this frame, the NSTC serves as a key node at the later TRL stages of the National Network. Altogether, the unique capabilities of NSTC and NAPMP enable advanced prototyping and fills the gap, or missing capability, in today's American semiconductor ecosystem, and would serve both commercial and government needs.

It is important to note that the NSTC is not the only important potential node for the National Network for Semiconductor R&D described in the CHIPS act. Two other potential CHIPS Act programs of note are a Manufacturing USA Institute and a Multilateral Semiconductor Security Fund. The former creates a new research institute within the NIST network focused on semiconductor manufacturing, and it would make a powerful partner for the NSTC in workforce training, the development of new capabilities, and as a supplier of ideas and technology into industry, the NSTC, and the NAPMP. The existing Manufacturing USA Institutes can also serve as a model for consideration by the NSTC in specific program areas. Currently, SIA member companies lead the ETAB Committee for each of the five microelectronics focused institutes (AIM Photonics, ARM Robotics, CESMII, Power America, and NIIMBL) in accordance with those companies' relevant expertise in the institute's focus. Companies would be similarly well suited to lead the NSTC's efforts in the research priorities relevant to their work. In a similar case of programmatic relevance to the NSTC, the Multilateral Semiconductor Security Fund serves to de-risk semiconductor supply chains away from China and toward allied regions, so close cooperation with the NSTC's own investment fund will maximize the technological and geostrategic value of federal and private investments.[52]

Beyond the programs of the CHIPS Act, in its report under Executive Order 14017, DOD emphasized the need to leverage digital engineering to plan the progression from design to use of advanced microelectronics, as well as to share these roadmaps with industry to increase the

[51] For an example of public-private partnerships, see the case study of Applied Materials' META Center and NY CREATES, which shortened the time to transition innovative technologies from lab to fab. ("ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 15)
[52] SIA BCG Report (Not Yet Finalized)

latter's visibility into DOD's future technology needs across multiple node sizes.[53] To those ends, DOD could coordinate its own work with industry as the NSTC sets an independent research agenda, and leverage the NSTC's prototyping resources toward both commercial and government priorities. Again, these efforts could be further enhanced with augmentation to the existing DOD trusted foundry infrastructure.

5. How should the NSTC ensure that it can identify and invest in what comes next after the first wave of needs are identified in the initial years? To what extent does the semiconductor ecosystem need a long-term roadmap of application requirements, technical needs, and gaps in materials, tooling and equipment, and process capabilities in order to guide future R&D investments? How can the NSTC's investments best support an open roadmap of this type, and how should the NSTC interface with other governments or allied international R&D programs, such as those established under Section 9905 of the FY2021 NDAA, to enable such a roadmap? What existing technology forums, roadmaps, or other initiatives should be incorporated into such efforts?

In discerning in which areas to prioritize investment, NSTC leadership should be guided by input on an industry-wide basis including leaders in academia. Input developed on an industry-wide basis has already identified some of the key imperatives for next-generation semiconductor innovation.[54] The NSTC should, however, continue to solicit input from all stakeholders, including research bodies and initiatives such as the IEEE HI roadmap.[55] Additionally, future input from the DoD National Network for Microelectronics Research and Development should be encouraged. Currently, information and communication technologies are facing five major seismic shifts. The technology goals outlined in *The Decadal Plan for Semiconductors* seek to address these challenges with groundbreaking advancements beyond incremental improvements in chip design, making these suitable paradigms to inform the NSTC's priorities.[56]

1. The Analog Data Deluge – Fundamental breakthroughs in analog hardware are required to generate smarter world-machine interfaces that can sense, perceive, and reason.
2. The Growth of Memory and Storage Demands – The growth of memory demands will outstrip global silicon supply, presenting opportunities for radically new memory and storage solutions.
3. Communication Capacity vs. Data Generation – Always-available communication requires new research directions that address the imbalance of communication capacity vs. data-generation rates.
4. ICT Security Challenges – Breakthroughs in hardware research are needed to address emerging security challenges in highly interconnected systems and AI.

[53] https://media.defense.gov/2022/Feb/24/2002944158/-1/-1/1/DOD-EO-14017-REPORT-SECURING-DEFENSE-CRITICAL-SUPPLY-CHAINS.PDF (p. 37 & 39)
[54] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 20
[55] https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html
[56] https://www.src.org/about/decadal-plan/

5. Compute Energy vs. Global Energy Production – Ever-rising energy demand for computing vs. global energy production is creating new risks, and new computing paradigms offer opportunities to dramatically improve energy efficiency across multiple node sizes.

The NSTC should vet and select technical objectives worthy of becoming priority research areas and allocate appropriate overall levels of funding for each of them. The results should be followed by an open competition whereby organizations of various types and sizes can submit proposals to research, prototype, and scale technologies aligned with a given research area.[57] Additionally, the NSTC should maintain an industry aligned strategic roadmap which sets initial vision and objectives but is also reviewed on an annual basis to account for new discoveries and changes in application needs. This should result in course corrections rather than holistic changes in strategy.

6. The NSTC is envisioned as a public-private partnership. What are the most suitable models of public-private partnership for the R&D and prototyping gaps that the NSTC is envisioned to address? What are the roles of the public participants and the private sector participants in this partnership, including any international participants? How should governance structures, program objectives, investment criteria, and oversight and accountability requirements be structured to maximize the transformative potential of the NSTC in the US R&D ecosystem?

Public-private partnerships (PPPs) encompass a range of organizations operated by private sector stakeholders but who are largely publicly funded. Examples of PPPs include the Federally Funded Research and Development Centers (FFRDCs) and SEMATECH, which can be funders or performers of R&D. FFRDCs, which include the national labs, are public-private partnerships operated by academic institutions or private companies funded by and performing research for the federal government. In contrast, SEMATECH initially received half industry funds and half government funds, but it ultimately became an industry consortium funded privately through member dues.[58]

For the semiconductor industry, a partnership or consortium wherein governance and decision-making at the highest level are done jointly by the participants, including the government, has worked well in the past. Participation is open to all global industry members with a participant's status determined in accordance with its interests and contributions. The consortium strives to operate on the basis of technical merits for the benefit of the industry as a whole. The consortium can rely on its own staff for the management of operations or retain an outside firm to manage operations.

Different structural proposals have been offered by various stakeholders, and these largely suggest either 1) full centralization, 2) full distribution, or 3) a mix of centralized and distributed

[57] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 18

[58] SIA BCG Research Report (Not Yet Finalized)

capabilities. In a vacuum, the full centralization of NSTC facilities would theoretically be the most cost-efficient approach as this would create automatic network efficiencies and avoid the need for redundant facilities in different locations. On the other hand, a fully distributed network may require greater redundancy in facilities, but it may provide the opportunity for centers with ° of specialization in certain research areas. In reality, however, much of the fabrication infrastructure needed for the NSTC already exists at various academic and company facilities, so the cost of establishing distributed centers as annexes to present facilities may be less the than the total cost of standing up a centralized NSTC. Regardless of which of these approaches the NSTC takes, however, its structure should be informed by a number of basic tenets whereby the NSTC will

- Convene industry, academia, and government and grant each an input in its governance.[59]
- Leverage existing U.S. semiconductor facilities at the beginning to expediently expand lab-to-fab capacity.[60]
- Maintain core centers across the U.S. where the best physical and human resources exist.[61]
- Coordinate NSTC member technical agendas and roadmaps.[62]
- Coordinate with U.S. government programs.[63]
- Coordinate with international facilities in like-minded nations.[64]
- Empower agile executive leadership while not being controlled by one entity, whether public or private, and including broad industry, academic, and government voices on its board.[65]
- Facilitate easy access to NSTC capabilities for universities and small businesses.[66]
- Develop IP management or licensing models for prototyping and piloting.[67]

[59] See SIA BCG Research Report (Not Yet Finalized); AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 15; "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 11

[60] See SIA BCG Research Report (Not Yet Finalized); "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 11

[61] See SIA BCG Research Report (Not Yet Finalized); "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 11

[62] See SIA BCG Research Report (Not Yet Finalized); "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 11

[63] See SIA BCG Research Report (Not Yet Finalized); "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 11

[64] See SIA BCG Research Report (Not Yet Finalized); "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 11

[65] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 15

[66] See "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 11

[67] See AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 20; "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 11

- Support education and workforce development across the semiconductor ecosystem.[68]
- Provide opportunities for broad industry participation, including international partners.

As a PPP, the NSTC must make sure to engage numerous stakeholders in its leadership.[69] These groups include:

- Researchers collaborating on “lab-to-fab" transfer, including those at universities, the National Labs, and industry.
- Providers of materials and equipment seeking to integrate new technology into their commercial offerings for semiconductor design, manufacturing, and testing.
- Users like IP developers, fabless companies, and system developers collaborating on assessing new tech tools, features, and architectures and driving tech development toward offerings they can adopt for their products; and
- Manufacturers to scale the new semiconductor technology to commercial production.

This inclusion of a wide range of stakeholders with unique offerings and needs would facilitate establishing the NSTC as a dynamic market with program-subsidized and customer direct-pay business models as methods to access offerings. This method of engagement can also provide a sustainability model for the NSTC as government support tapers off.[70]

For the NSTC to be successful in revitalizing U.S. leadership in advanced semiconductor R&D and improving supply chain resiliency, it must be structured as a public-private partnership mandated in the CHIPS legislation with broad industry participation. An industry-led NSTC consortium is the most promising model. However, establishing an NSTC consortium would be very challenging under a typical process pursuant to the Federal Acquisition Regulations (FAR), as it would likely result in a web of prime and subcontractor relationships, require a sizable new government program office, and make broad industry participation harder due to complex federal contracting rules. Commerce should use an alternate process to join with industry in establishing the NSTC with a consortium model that maximizes participation by industry, government, academia, and workforce partners.

The House-passed America COMPETES Act includes language granting Commerce *Other Transaction Authority (OTA)*, and we hope that a final conference bill will also include such a provision. OTA provides statutory authority for a federal agency to enter into alternative contractual agreements outside the FAR. Congress first authorized OTA over 60 years ago, but the basis for streamline government engagement with industry consortia derives from the enabling legislation for SEMATECH. SIA worked closely with DARPA to develop this form of OTA and it has been used successfully by many collaborations between government agencies and

[68] See SIA BCG Research Report (Not Yet Finalized); AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021 25-26; “ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA”, FEBRUARY 2022, 11
[69] “ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA”, FEBRUARY 2022, 12
[70] “ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA”, FEBRUARY 2022, 14

the semiconductor industry. More broadly, OTA has been updated and extended in various forms to eleven different federal agencies. However, the Commerce Department currently does not have OTA.

OTA is the best option for the NSTC for multiple reasons:

- It enables a public-private partnership mandated by CHIPS. A consortium governance model with multiple levels for industry and government participation is the most feasible way to achieve a broad public-private partnership mandated by the CHIPS legislation. A consortium could include a governing council in which industry participants, academic partners, and government agencies could have a voice and participate in guiding the NSTC Technology Roadmap.
- It maximizes participation by semiconductor industry players. OTA would sanction pathways for semiconductor industry players to participate in the NSTC outside the rather complex administrative process created by the FAR. Under the FAR, industry participants would likely need to enter a contractual relationship directly with the government or as a subcontractor to an NSTC member. Federal contracting burdens (i.e., cost accounting standards) would be a deterrent for many companies to participate in the NSTC, inhibiting the inclusion of a diverse array of industry and academia participants in the NSTC. FAR requirements would make it especially difficult for the NSTC to include small and medium sized companies, new startup firms and potentially materials and tool suppliers that may be neither heavily capitalized nor accustomed to government contracting. Participation by these essential members of the semiconductor supply chain is critical to the success of the NSTC.
- It allows innovation to proceed at the pace of industry and be guided by broad industry engagement. All of the industry must be able to access the NSTC to foster innovation. Under the FAR, many aspects of the NSTC's work and governance would flow through a government contracts office, so a new NSTC program office would be needed to manage that work. That program office would be constrained by federal hiring rules and budgeting processes, and it would limit much of its engagement to NSTC contractors. Innovation would only proceed at the pace of decisions made in those offices. Under an OTA, a NSTC consortium could manage day-to-day activities through its own industry staff, and it could build a framework that eases and maximizes engagement with industry, academic, and workforce partners. Commerce could exercise strong oversight by direct participation in consortium governing councils.

7. What operational and organizational characteristics, business processes, and practices will be important in ensuring that the resources of the NSTC are broadly accessible and available to the broader U.S. semiconductor R&D community including both small and larger, more established entities? How can the NSTC ensure that smaller and medium sized companies and startups have access to facilities, expertise, and intellectual property that public funds support?

The NSTC's purpose is ultimately to fill in gaps in the current semiconductor ecosystem and to enhance the basis for technology leadership, so particular attention must be paid to those actors that face the steepest barriers. Startups historically struggle to access existing

commercial fab facilities. Larger companies can afford to pay more and run higher volumes of wafers, so these managing groups may rescind a startup's reserved fab access to pursue higher returns. This in turn creates risk for startups as they cannot be certain about their fab access.[71]

The NSTC would address this difficulty through partnerships, market-based infrastructure, and open competitions that invite participation from groups large and small. An NSTC network could include publicly owned regional hubs that partner with universities, private industries, and consortia across the nation. These hubs would upgrade U.S. R&D facilities where global leaders already collaborate with engineers and scientists, and in doing so they would open the door to these facilities and talent pools to smaller groups that may previously have been shut out.[72] Furthermore, the NSTC's pathfinding infrastructure should be accessible for all eligible players in the ecosystem,[73] regardless of company size or location. Access can be facilitated by a market-based structure with program-subsidized and customer direct-pay business. Either direct revenue or subsidized support would facilitate access for start-ups and academia, and as previously mentioned this method of engagement can provide a sustainability model for the NSTC as government support tapers off.[74] Lastly, as the NSTC sets out in pursuit of its research priority areas, it should offer open competitions where groups ranging from academia to startups and large companies can offer proposals to capture these innovations.[75] This model would allow the ecosystem to crowd-source the creativity of multiple innovators in pursuit of NSTC-established groundbreaking goals. The NSTC can also support large companies performing research and early prototyping within their own facilities, thus providing an easy glide path to upscaling and piloting.

8. For those who currently participate or have participated in a "research consortium" (either domestic or international) made up of public and private partners, what are the important lessons learned or best practices that the NSTC should follow?

A number of past and ongoing PPPs offer lessons on how to structure the NSTC.[76] In the 1980s, the US military needed semiconductor materials with performance beyond the limits of silicon. The Office of Naval Research (ONR) and DARPA accordingly identified and facilitated academia-industry collaboration to advance compound semiconductor materials through the phases of innovation and tailor them to industrial uses. The resulting materials, like gallium nitride are widely deployed today for civilian and military uses, including several of strategic importance. In the same decade, new applications also drove the need for continued transistor scaling. While

[71] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 23
[72] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 7
[73] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 23
[74] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 14
[75] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 14
[76] See SEMATECH (U.S.), Imex (Belgium), Semiconductor Research Corporation (U.S.), VLSI (Japan), Fraunhofer-Gesellschaft (Germany), AIM Photonics (U.S.), NextFlex (U.S.), and the DOE National Labs (U.S.)

EUV's potential was known, many in the industry considered EUV infeasible given technical and other challenges. Nevertheless, DARPA funded the Advanced Lithography Program which conducted early research into EUV reflectometry. Private industry and several FFRDCs made investments into tools and related developments necessary for EUV's success. SEMATECH, a non-profit consortium that performed R&D to advance chip manufacturing, partnered across industry and academia for over 15 years to access and build out infrastructure and expertise that individual companies alone considered too risky. Following this, co-investments with ASML, Intel, Samsung, and TSMC dedicated between $10B and $17B over 15 years to mature EUV into a commercially viable technology.[77] These efforts ultimately demonstrated the viability of EUV technology. Although economic viability of EUV was predominantly pioneered outside the U.S., the development of this key technology area with our international partners ultimately provided an enormous technological benefit for the U.S. technology ecosystem. NSTC should encourage private investments by all entities that are using its equipment or facilities. These investments could be scaled based on the type of entity and type of access or research request. Overall, common needs, principles and objectives are required for the benefit and sustainability of any organization. Fair and open access as well as frank and objective discussion must be fundamental to the principles as well as for the advancement of semiconductor leadership for the country. Without common needs, focus will diverge and long-term success suffer. Very clear expectations and objectives which are well communicated to all participants along with common ethical practices and policies. IP can be problematic and expectations/policies need to be very clear and clean up front.

9. What attributes or capabilities of the NSTC would make it attractive and beneficial for companies, universities, and other agencies to want to send employees for assignments at the NSTC? What types of research and training opportunities should be made available at the NSTC for students and early career staff?

First, NSTC's focus should be on pre-competitive prototyping research and development, some of which can be done at universities or some corporate facilities. Its fundamental mandate concerns transitioning technologies from validation in a laboratory to scale-up in a fab. It is important to recognize that this mission differentiates the NSTC from the fundamental research mandates of other USG initiatives or of international efforts such as IMEC. This work should provide many research opportunities for young researchers, as a part of an NSTC-funded project. The ability for the NSTC to serve as a nexus of innovative technology development, draw research funding, and provide key training opportunities for future work in the semiconductor industry makes it potentially attractive to university employees, especially professors, research staff, postdoctoral researchers, and graduate research assistants. The capacity to support mission-relevant lab-to-fab technology transitions would make the NSTC a potentially attractive assignment for mission-focused agency employees such as those at the DOD, DOE, and NASA. In order to best draw potential employee assignments from private

[77] https://www.eetimes.com/intel-again-cuts-stake-in-asml/#:~:text=In%202012%2C%20Intel%2C%20Samsung%20and%20TSMC%20all%20invested,their%20stakes%20in%20ASML%20by%20at%20least%2050%25.

companies, the NSTC needs to have a clear benefit to the workforce pipeline for those companies and the term of assignment for the employees needs to be flexible and have the opportunity to be relatively short term. It is critical that employees sent for assignment can return to their industry positions with relative ease. The NSTC can also serve as a center for collaborative interaction between different firms and agencies, thus promoting technology and knowledge transfer, which is valuable to the engineers themselves.

The ability for the NSTC to help address U.S. workforce training needs is especially critical. A recent White House agency announcement fact sheet describes a variety of beneficial actions the executive branch plans to take to address the increasing U.S. STEM demands. Within this broad set of activities,[78] the NSTC could promote a range of programs to expand the supply of the U.S. semiconductor R&D workforce:

- **Invest in US STEM education**. The NSTC could support curriculum development and standardization at the high school, undergraduate, and graduate levels to expand the pipeline of workers with prerequisite STEM skills.[79] Additionally, building the awareness of what microelectronics enables and importance to daily lives can motivate or excite students to learn more and move into this area. Starting at the middle-school level is not too early. These students "see" the apps on their phones but don't realize the microelectronics it takes to support them.
- **Attract STEM graduates to the industry**. The NSTC could educate students about career opportunities in the semiconductor industry through apprenticeships, internships, and mentorship programs.[80] By offering a path for graduate students and postdocs to also commercialize their own startups and IP, the NSTC could offer further incentive for U.S. students to remain in the industry and foreign students to remain in the U.S.[81]
- **Promote flexible work authorization**. The NSTC could promote flexible work authorization programs – like optional practical training periods - that enable foreign nationals to work in the US if they graduate from U.S. universities with skills critical to industry.[82]

Additionally, while the supply of highly skilled R&D workers currently threatens to limit the pace of innovation, the NSTC should also work with industry, community colleges, and vocational schools to develop and to enhance curricula for training programs for technicians critical to semiconductor manufacturing.[83] (Maricopa Community College's Associate in Applied

[78] https://www.whitehouse.gov/briefing-room/statements-releases/2022/01/21/fact-sheet-biden-harris-administration-actions-to-attract-stem-talent-and-strengthen-our-economy-and-competitiveness/

[79] See SIA BCG Research Report (Not Yet Finalized); American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 25; "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 13

[80] See SIA BCG Research Report (Not Yet Finalized); American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 25; "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 13

[81] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 13

[82] See SIA BCG Research Report (Not Yet Finalized); American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 26

[83] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 26

Science (AAS) in Electronics Technology program offers a model for how these local programs could be shaped.)[84] [85] [86]

10. For organizations that currently utilize an external semiconductor "fab" as part of their R&D efforts, what services or processes are currently missing in the U.S. ecosystem that the NSTC should provide? Are there specific toolsets that the NSTC should own and operate or provide access to?

Both companies with manufacturing presences and fabless companies may at times be unable to secure the manufacturing capability need to prototype and pilot new areas of research, but it may prove extraordinarily challenging and prohibitively costly to build and to maintain centrally owned (or NSTC-owned) toolsets. To that end, the NSTC should provide access to fabrication facilities, design tools and IP, cloud compute and design infrastructure, and top design and foundry technology experts to assist companies large and small in designing and developing prototypes. These tools should be available as in a marketplace where companies can acquire solutions for their acute needs.[87]

NSTC should have leading edge fabrication tools for deposition, patterning and etch. NSTC provided fabrication facilities should enable multi-product wafer runs and low-volume manufacturing for prototyping.

To effectively address complex needs across the industry, several NSTC "centers of excellence" should focus on critical strategic technologies. These will be organized by leading companies and universities in the respective areas under the coordination of the larger network.[88]Importantly, the capabilities at some centers of excellence may be generalizable to multiple technology areas, or they may only be applicable to one type of technology. Whether generalizable capabilities will be open to a variety of uses or not may depend on nature of the technologies in question and on the IP structures and capacity utilization of each center.

11. As authorized, the NSTC could establish an investment fund, in partnership with the private sector, to support startups and collaborations between startups, academia, established companies, and new ventures, with the goal of commercializing innovations that contribute to the domestic semiconductor ecosystem, including advanced metrology and characterization for leading-edge manufacturing processes, and for security and supply chain verification. How should this investment fund be structured, and what should be the roles of the public and private sectors in capitalizing, operating, and overseeing the fund and selecting its investment

[84] https://www.maricopa.edu/degrees-certificates/science-technology-engineering-mathematics/electronics-technology-3220-aas
[85] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 14
[86] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 19
[87] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 14
[88] "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 25

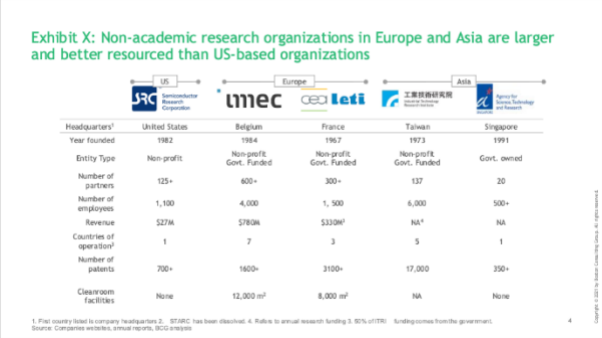
targets? Should the investment fund focus on early-stage investing, late-stage investing, or other stages of the process? How should the fund interact with existing private capital, both venture capital and established investment capital, and how can the fund sustain itself through its investments?

The NSTC investment fund should serve to facilitate the growth of startups born out of both the private sector and other federal research efforts. By offering support to early-stage companies as they approach the prototyping and piloting stages, the fund can de-risk these companies for private sector capital, catalyzing private investment in areas that the market has traditionally been unwilling to enter.[89]

To accomplish this, the fund should seek out organizations pursuing next-generation semiconductor technology with comparable ambition and projected impact as the NSTC's own priority research areas. The fund may look to groups that provide funding for basic research, such as universities, DARPA, the National Laboratories, the Semiconductor Research Corporation, etc., to identify promising startups. By doing this, the fund can avoid mimicking the mission of these groups and focus its efforts on transitioning innovations through prototyping and piloting. The fund's support should ultimately act as an incubator, providing hands-on and in-kind services like access to facilities and wafer runs, and it should seek to connect startups with larger entities involved in the NSTC's priority research areas.[90]

12. How should the NSTC's investments and focus overlap or complement the investments and capabilities of foreign institutions such as the Interuniversity Microelectronics Center (imec) in Belgium or the French Laboratoire d'électronique des technologies de l'information (CEA-Leti)?

Private industry works with non-academic research organizations in the U.S., like the SRC, and in allied nations, such as IMEC and CEA-Leti, for basic research. While the SRC is based in the US, it is smaller than non-academic research organizations in Europe and Asia, making international cooperation of critical importance. (See chart comparing global non-academic research organizations.)[91]



Headquarters[1]	United States	Belgium	France	Taiwan	Singapore
Year founded	1982	1984	1967	1973	1991
Entity Type	Non-profit	Non-profit Govt. Funded	Non-profit Govt. Funded	Non-profit Govt. Funded	Govt. owned
Number of partners	125+	600+	300+	137	20
Number of employees	1,100	4,000	1, 500	6,000	500+
Revenue	$27M	$780M	$330M[3]	NA[4]	NA
Countries of operation[2]	1	7	3	5	1
Number of patents	700+	1600+	3100+	17,000	350+
Cleanroom facilities	None	12,000 m²	8,000 m²	NA	None

1. First country listed is company headquarters 2. SITARC has been dissolved. 4. Refers to annual research funding 3. 95% of ITRI funding comes from the government.
Source: Companies websites, annual reports, BCG analysis

[89] AMERICAN INNOVATION, AMERICAN GROWTH: A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER, NOVEMBER 2021, 22

[90] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 22-23

[91] SIA BCG Research Report (Not Yet Finalized)

We also recommend that NSTC seek to collaborate with these and other international partners to ensure it is prioritizing long-term solutions, not duplicating current research efforts, and engaging these partners to collaborate on NSTC projects domestically.

Advanced Packaging Manufacturing Program

1. *Please describe the application areas that are essential to long-term national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:*
    a. Analog device packaging
    b. Automotive
    c. Defense and aerospace
    d. Energy generation, transmission, conversion, and storage
    e. Harsh environments
    f. High performance computing, quantum computing, data centers
    g. Integrated photonics
    h. Integrated power electronics
    i. Internet of Things
    j. Mature packaging
    k. Medical, health & wearables
    l. MEMS and sensor electronics
    m. Mobile telecommunications
    n. Other?

Microelectronics leadership requires a range of packaging technologies in addition to high density multi-die heterogeneous integration which will be essential for compute and AI/ML workloads with associated memory and I/O connectivity. Specifically, power electronics requires unique solutions to high current, high voltage, isolation and thermal/mechanical management. Analog solutions for real world interfaces include communications and sensing via electric, magnetic, optical fields to address the wide range of applications. The co-package of the sensor itself plus precision electronic processing will present challenges in enabling the sensing parameter while protecting supporting electronics from stress, temperature and other environments. In all cases, co-packaging of multiple technology capability is required along with CMOS and other semiconductor devices such as SiGe, GaN, InP and silicon photonics. The packaging solutions will need to incorporate a range of technologies including organic substrates, advanced lead frames, flip chip, die-on-die, chiplet, isolation and thermal materials to name a few.

For example, compute-intensive applications require access to significant amounts of memory, making improvement in logic-memory bandwidth critical. This application highlights an important trend towards chiplet-based architectures (a “chiplet” is an integrated circuit block specifically designed to work with other chiplets to form a larger more complex system). Improving high-speed bandwidth across the chiplet interconnections presents an important

packaging challenge. This trend towards chiplets is an opportunity for the nation to regain leadership in packaging and heterogenous integration.

The above list itself is sufficiently comprehensive for now, but these areas are as critical for the NSTC concerns as they are for packaging. While setting a list of specific downstream sectors has value, any current list should not be considered "final", and the overall governance structure of the NSTC-related efforts should include mechanisms to refine and/or expand this list as needs are identified by industry and government participants.

Grouping areas should be determined by industry and government participants as the structure of the NSTC-related efforts are being determined. It makes sense to include voices from mission agencies (DOD, NASA, DOE) for those areas that are especially relevant to their mission and funding. For these areas especially, direction should be determined by both industry and government needs. For areas outside of the needs of mission agencies, industry should take a larger role in determining the needs and directions.

All considered, a recent presentation from Yole[92] at the SIA "Trends and Challenges in Semiconductor Advanced Packaging" webinar, groups the primary application areas as:

- Automotive & Mobility
- Industrial
- Mobile & consumer
- Telecommunications & infrastructure
- Defense & aerospace
- Medical

At the same webinar, Amkor[93] described the primary advanced packaging platforms as:

- Chip scale to fan-out
- MEMS packaging
- Flip chip
- Heterogeneous integration / 3D architectures
- System in package

2. *Please describe the R&D core-competencies that are essential to national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:*
    a. Alternative materials to mitigate impact of supply chain disruptions o Artificial intelligence for design of packaging
    b. Assembly and test
    c. Emerging materials

[92] https://www.semiconductors.org/wp-content/uploads/2020/09/Guillaume-Assogba_Yole_A-Yole-Perspective.pdf

[93] https://www.semiconductors.org/wp-content/uploads/2020/09/John-Stone_Amkor_Trends-and-Challenges-in-Semiconductor-Advanced-Packaging.pdf

d. Heterogeneous integration, chip stacking, and related technologies.
e. High-density substrates
f. Metrology
g. Modeling and simulation
h. Package-level design/codesign tools for electrical, thermal and mechanical design of complex packages
i. Printed circuit boards
j. Safety and security
k. Software, firmware, new concepts in programming
l. Standards
m. Test solutions to assure yield in complex packages
n. Thermal solutions
o. Tooling
p. Other?

This list of core competencies is sufficient for now, and most of the identified core-competencies are critical for the five advanced packaging platforms described above. However, any current list should not be considered "final", and the overall governance structure of the NSTC-related efforts should include mechanisms to refine and/or expand this list as needs are identified by industry and government participants.

The packaging-related efforts are especially valuable, in the context of the broader CHIPS efforts, as an integrating stage for the technologies that will come out of the NSTC ecosystem. These technologies will have unique needs which will dictate the most important set of core-competencies. As such, it should not be considered an entirely separate entity, but rather a key component of the technology development process.

Within this, heterogeneous integration (HI) will be a key pillar of future microelectronics and drive multiple technology needs in packaging including 2.5D and 3D die stacking integration, power integration with thermal management from low to high current, and voltage and power dissipation. Multi-physics knowledge and collaboration will be required to address the co-design environment with NAPMP or in coordination with NSTC. Additionally, multiple advanced packaging approaches need to be supported.

Part of the value of government/industry partnerships is the possibility to convene a critical mass of technology stakeholders to help develop open standards for integration. These standards should be led by industry needs in most cases, with government serving primarily as a convening authority.

It makes sense to include voices from mission agencies (DOD, NASA, DOE) for those standards that are especially relevant to their mission and funding. For these areas especially, direction should be determined by both industry and government needs.

3. *A proposed National Advanced Packaging Manufacturing Program could be oriented to address multiple needs, including but not limited to prototyping, the provision of pilot lines, workforce development, and supply chain development. Please describe the most critical needs on which the program should focus.*

Addressing a lack of robustness in the supply chain is a primary concern. Large OSAT firms (manufacturing mostly outside of the US) are dominating the supply chain and their lead on the smaller firms is growing.[94] Of the top 8 OSAT companies by revenue, 3 are based in China and the largest US-based OSAT company, Amkor, mostly does not produce in the US. In addition to the lack of advanced manufacturing capacity in the U.S., there is also a lack of advanced prototyping capability. The result is that despite significant innovations in packaging driven by U.S. based companies who lead in chip design and advanced systems, the designs are often demonstrated in offshore facilities. The situation in advanced packaging has many similarities to front-end wafer fabrication.

Workforce development will be critical in all scenarios, but a coordinated workforce effort across all CHIPS related activities is the best approach.

Determination of the needs that a National Advanced Packaging Manufacturing Program would serve should be done alongside the determination of the broader structure of the CHIPS activities. That is to say, the structure of the NSTC and manufacturing incentives should be part of the consideration of what needs to address with the packaging program.

As above, determination of needs should be industry led for the most part, with input from mission agencies to address specific mission needs.

4. *What attributes are the most important for a National Advanced Packaging Manufacturing Program to deliver? Examples include but are not limited to:*
    a. "Leading edge" tools
    b. Characterization services
    c. Collaboration across multiple universities and multiple companies
    d. Development of education and workforce development infrastructure, including building a pipeline of skilled workers
    e. Easy to access facility, with different processes and tools
    f. Expert resident staff for custom development
    g. International participation
    h. Intellectual property protection for inventors
    i. Open access to intellectual property
    j. Post fabrication infrastructure
    k. Other?

[94] https://www.semiconductors.org/wp-content/uploads/2020/09/Santosh-Kumar_Yole_Advanced-Packaging-Current-Trends-and-Challenges.pdf

Appropriate handling of IP will be of paramount concern for any industry participation. Beyond this, determination of the attributes that a national advanced packaging manufacturing program would serve should be done alongside the determination of the broader structure of the CHIPS activities. That is to say, the structure of the NSTC and manufacturing incentives should be part of the consideration of what needs to address with the packaging program. As above, determination of attributes should be industry led for the most part, with input from mission agencies to address specific mission needs.

That said, the ability to provide access to an open library of integratable chiplets would be very powerful for unlocking access to heterogeneous systems innovations for research groups, start-ups, and even larger companies. Such an effort would include examples c, d, f, g, h, and i as noted above. See page 5 of Day One Project's Institute for Scalable Heterogeneous Computing for a more thorough description.[95]Availability of "leading-edge" tools and characterization services in prototyping facilities that span advanced packaging, assembly and test will also be critical to ensuring leadership for the U.S. in this area. Universities, start-ups and large companies (including many of the largest in the world) do not have access to flexible packaging prototyping facilities in which they can develop and demonstrate new packaging-based innovations.

5. *What factors are critical to enable a National Advanced Packaging Manufacturing Program to provide a successful packaging R&D hub(s)?*

The largest factors governing a successful R&D hub are quite similar to those that allowed many of the Manufacturing USA hubs to be successful: appropriate IP handling, integration with local innovation and workforce ecosystem, access to funding (both government and industry) with minimal contracting restriction, and strong leadership informed by industry needs and a clear portfolio strategy. The National Advanced Packaging Manufacturing Program must identify requirements and integrate capabilities from a variety of end-users and applications in order to focus efforts and resources on approaches that can scale.

6. *Identify processes, equipment, measurement capabilities, environmental conditions, and training facilities that are most crucial for facilities provided by a National Advanced Packaging Manufacturing Program. How might organizations access such facilities?*

The facilities provided should address the primary advanced packaging platforms of:

- Chip scale to fan-out
- MEMS and sensor packaging
- Flip chip and die-on-die
- Heterogeneous integration / 3D architectures
- Photonics/optical integration

[95] https://www.dayoneproject.org/post/an-institute-for-scalable-heterogeneous-computing

- Power packaging for high voltage, high current, isolation, and thermal management
- System in package

These facilities should be capable of addressing the needs of the advanced packaging roadmap as identified by Yole.[96] These include processes, equipment, measurement capabilities and environmental conditions that are very different from traditional packaging facilities. These facilities must provide infrastructure and a home to demonstrate first-of-a-kind technologies that will enable the roadmap. For a more thorough description of the important processes, equipment, measurement capabilities, and environmental conditions, the IEEE heterogeneous integration roadmap should be considered.[97]

Specific determination of the facilities that a national advanced packaging manufacturing program would need should be done alongside the determination of the broader structure of the CHIPS activities. That is to say, the structure of the NSTC and manufacturing incentives should be part of the consideration of what facility needs the packaging program would face. As above, determination of needs should be industry led for the most part, with input from mission agencies to address specific mission needs.

Such facilities will be best provided by participating industry stakeholders who grant access, by government labs with appropriate capabilities, and by participating universities. Industry stakeholders may need support from NSTC to expand and to accommodate capacity.

7. *How closely aligned should the capabilities enabled by a National Advanced Packaging Manufacturing Program be with those provided by the NSTC?*

The NAPMP should be closely aligned with the NSTC. The packaging program will take technologies developed within the NSTC and package/integrate those technologies into useful components/systems. The NSTC will receive feedback from the packaging program to development technologies tailored to specific integration strategies, or to address specific downstream needs. Packaging R&D and semiconductor R&D should be co-located for the case of advanced logic and HI. Hubs to support packaging for other semiconductor technologies such as memory, analog / mixed signal, sensors, flexible substrates, power electronics, and advanced SiP technologies do not necessarily need to be co-located with a semiconductor hub. With that said, neither should be totally dependent on the other. The NSTC should be able to leverage packaging capabilities and technologies beyond those of the packaging program, and the packaging program should be able to use technologies developed outside the NSTC. We should expect that the packaging program will be focused on different challenges that are more related to end-product and system level challenges vs. the NSTC. For example, IC-substrate

[96] https://www.semiconductors.org/wp-content/uploads/2020/09/Santosh-Kumar_Yole_Advanced-Packaging-Current-Trends-and-Challenges.pdf
[97] https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html

architecture and designs need to support a variety of use conditions related to the many market segments that will benefit from advanced packaging.

8. *How should the National Advanced Packaging Manufacturing Program connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?*

As programs from the FY 2021 NDAA are set up and receive funding, the NAPMP should coordinate its efforts with those of the other government and industry programs.[98]
The National Network for Semiconductor R&D is intended to enable lab-to-fab transition of microelectronics innovations in the U.S. and expand U.S. microelectronics leadership. Towards this, it is instructed to enable exploration of new materials, devices, and architectures and to accelerate transition of novel technologies to manufacturers via domestic prototyping capabilities. These tasks will be best accomplished in close partnership with the NAPMP, and likely leveraging the prototyping capabilities that will be created as a part of the broader NAPMP efforts. As such, there should be an overlap in TRL coverage, with earlier level TRL at the National Network, transitioning to higher TRL in the advanced packaging program. Basic research and development at TRL 1-4 can inject new ideas towards future electronics while NSTC and NAPMP would facilitate advancing the TRL to 5-8 level better proving technologies towards commercial manufacturing. Representatives from the DOD should participate in the NAPMP to ensure coordination between the two efforts.

9. *Describe anticipated needs in education and workforce development, including retraining and upskilling, in the semiconductor packaging area. How adequate is it currently, and what are future expectations of need? How should the workforce training pipeline be developed?*

We defer to our member companies' individual responses. That said, current workforce development for microelectronics packaging is insufficient for the needs of the industry – both current and future. Typically, microelectronics education focus is on devices, design and systems with little on packaging. Packaging requires several different disciplines including electrical, mechanical, chemical, physics and industrial engineering. Importantly, there needs to be collaboration across these disciplines for effective manufacturing worthy packaging solutions. In addition to formal training, additional skills are needed including problem solving, failure analysis, diagnostics, modeling (electrical, thermal, stress/mechanical, optical, materials)

[98] For an example of public-private partnerships, see the case study of Applied Materials' META Center and NY CREATES, which shortened the time to transition innovative technologies from lab to fab. ("ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 15)

Semiconductor Workforce

1. *What are the greatest occupational or skills shortages facing employers in the semiconductor sector? What are the consequences of those shortages with respect to the domestic operation of employers in the sector? Considering all aspects of building, equipping, and running semiconductor manufacturing and R&D facilities, what actions have been taken to address these shortages, how effective have they been, and what gaps remain?*

A recent report by the Center for Security and Emerging Technology characterizes the U.S.'s supply of high-skilled semiconductor workers through domestic STEM pipelines and immigration.[99] These inflows of talent will have to increase in order to meet current and expanding demand across the industry. In research alone, the CHIPS Act incentives are expected to generate over 66,000 R&D jobs.[100]

Additionally, as companies break ground on new projects spurred by the CHIPS incentives, the industry will create over 235,000 construction jobs in the six-year build-out phase. Ongoing operational needs will generate 525,080 jobs, many of which will be in manufacturing.[101] Purdue University ran a workshop to assess needs for Microelectronics and Advanced Packaging workforce development.[102] The workshop provided useful assessment of the need and some suggestions for additional measures to build the semiconductor workforce.[103] Also, the demand for technical hourly workforce continues to grow with limited amount candidate pool available in the market. Along with that, other manufacturing and commercial industries with high hiring demands who are pulling from the same talent pool hence causing further shortages of entry-level talent.

2. *What strategies have been most effective in addressing the shortages? Which states or countries have created the most effective strategies for different types of workforce needs to build, equip, and run semiconductor manufacturing and R&D facilities? What industry or other credentials do employers use, or could use, to train and hire workers to fill needed positions? To what extent do employers in the semiconductor sector partner with government institutions such as local workforce boards, economic development organizations, or Manufacturing Extension Partnership centers, or international partners to establish training and/or skill certification programs? To what extent do employers in*

[99] https://cset.georgetown.edu/wp-content/uploads/CSET-The-Chipmakers.pdf (p. 14-20)
[100] https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf (p. 18, §4.4)
[101] https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf (p. 18)
[102] https://engineering.purdue.edu/Engr/AboutUs/News/Events/purdue-microelectronics-and-advanced-packaging-workforce-development-workshop
[103] Microelectronics and Advanced Packaging Workforce Development Workshop," Nov 2021

the semiconductor sector partner with other employers to create joint training programs?

There are several programs across the country that have been successful in addressing these shortages. As one example, the Department of Defense's Scalable Asymmetric Lifecycle Engagement (SCALE) program is a public-private-academic partnership that supports university engineering departments and matches participating students with private sector employers. This program has seen early success in building a STEM workforce in each of its five technical verticals at both the undergraduate and graduate levels. Another example is Maricopa Community College's Associate in Applied Science (AAS) in Electronics Technology program, which offers a model for how more local educational programs could be shaped.[104] *There is a huge opportunity to partner with local community colleges and high schools to train and develop talent to cater to skills required in semiconductor manufacturing. Veteran engagement and skill bridge programs is a huge area of develop talent pool and help veterans transition into civilian workforce.*

3. *What types of apprenticeship programs or existing partnerships involving workforce development issues in the semiconductor sector should the Department be aware of? What role can unionized labor play in worker training and workforce development, including for economically disadvantaged individuals?*

The Taiwan Semiconductor Research Institute (TSRI) is the product of the consolidation of two national labs in Taiwan, and it serves as a powerful model for what services a workforce collaboration between government and industry ought to offer. The TSRI offers a comprehensive range of training programs, comprising a series of courses ranging from device fabrication to circuit systems, and TSRI partners with universities that offer courses on fundamental theories to complement the practical lessons offered by the institute. Beyond education, TSRI facilitates critical hands-on opportunities by providing advanced process equipment and a complete measurement and design environment that students and trainees can use. Because the training courses include both introductory and applied/laboratory lessons, learners are able to complete their own chip designs, which teaches them the critical tacit skills needed to add value in the industry at the highest levels.[105]

4. *What have been successful mechanisms used by employers in the semiconductor sector to work with local high schools, career and technical education programs, community colleges, or universities to recruit and train workers?*

One major U.S. semiconductor firm runs a $1.4 million annual educational assistance program where hundreds of employees are supported each year to pursue master's degrees, bachelors, associates, and certificate programs in job-related fields. Similarly, another firm supports its

[104] https://www.maricopa.edu/degrees-certificates/science-technology-engineering-mathematics/electronics-technology-3220-aas
[105] https://www.tsri.org.tw/en/training.html

own employees' up-skilling with a $30,000 annual tuition reimbursement program. Beyond tuition assistance, another U.S. firm hires over 170 Co-Op/Intern students each year, while another firm spends over $1.5 million annually to support approximately 70 interns across the U.S. Much more work is needed, however, to fulfill the current and expected demand for STEM talent in the semiconductor industry, and the impact of such company efforts can be amplified by partnerships with federal, state, and local initiatives like those of DOD SCALE and Maricopa Community College. Companies are partnering with community colleges and universities to develop targeted programs and curriculum to feed into their talent pool. This allows companies to make early investments in talent to educate and train them based on skill needs to perform jobs.

5. *Are there any current or planned initiatives in the semiconductor sector to strengthen and expand the recruitment of women and underrepresented minorities, including promotion of such careers at K-12 levels?*

One SIA member offers online resources for students, educators, researchers, and entrepreneurs in developing their skills in the semiconductor industry. It helps train and certify students on intelligent system design technologies, learning computational software skills for transitions into industry, and these are complemented by scholarship and internship opportunities that directly support the pipeline of new and diverse STEM talent.[106]

Additionally, one major U.S. semiconductor firm runs a $4.5 million multi-year program with 6 historically black colleges and universities (HBCUs) to increase the pipeline of African Americans in engineering fields. This program has increased black enrollment in these fields by as much as 55 percent in some partner universities. The same firm also runs a $5 million partnership with a local public school district to encourage underrepresented youth to pursue further education in STEM fields. Over four years, underrepresented minority students enrolled in computer science classes in the district increased by 17 times, and girls enrolled in computer science increased by 33 times.

Lastly, FIRST Robotics is a hands-on learning program that prepares K-12 students for jobs in engineering and other STEM fields. It organizes students into teams that design, program, and build robots, and these teams compete on local and national levels.[107]
These types of long-term investments have a proven track record and a scalable model of such programs across the U.S. should be considered to attract more underrepresented minorities to the semiconductor sector.

6. *To what extent, and for what occupations, do organizations in the semiconductor sector use the H1-B Program to fill positions?*

[106] https://www.cadence.com/en_US/home/company/cadence-academic-network.html
[107] https://www.firstinspires.org/robotics/frc

H1-Bs are not the semiconductor industry's largest source of foreign talent. SIA advocates for eliminating the counterproductive per-country cap on employment-based visas in favor of a fair, "first come, first served" system, providing U.S. semiconductor companies with greater access to top talent from around the world needed to compete and innovate.

The Equal Access to Green Cards for Legal Employment (EAGLE) Act of 2021 (H.R. 3648) would phase out the 7 percent per-country limit on employment-based immigrant visas and raise the 7 percent per-country limit on family-sponsored visas to 15 percent. This would create a "first come, first served" visa system for high-skilled immigrants who are already living, working, and paying taxes in the United States, rather than the current, country-based system that unfairly pushes certain workers to the back of the line based solely on their country of birth.

7. *Are there opportunities to design the semiconductor incentive program to ensure that worker skills shortages do not hinder companies from expanding operations?*

In order for the incentive programs to maximize impact and ensure quick growth of the semiconductor manufacturing industry in the U.S., it is important to not attach worker quotas based on arbitrary policy goals unrelated to the industry. While the semiconductor industry aims to promote diversity and inclusivity, we believe such values are already appropriately addressed in the authorizing legislation. Any restriction, requirements, quotas or caps would hold back quick growth in the U.S.
An on-going investment strategy through the incentive pool is going to be very important to support a sustainable growth model. Also, casting a wider net to cover universities, community colleges, high schools, K-12 programs, veteran initiatives, etc. through the incentive program is going to be crucial to develop and funnel a diverse and consistent flow of talent pool for long-term needs.