Creating a Skilled Worker Pipeline for Microelectronics

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A ready workforce is required for the U.S. to lead high-performance microelectronics for decades to come

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Develop meaningful program for US citizen students to establish relationships with potential employers, which lead to employment after graduation.

**SCALE BLUF**

**SCALe**

Scalable Asymmetric Lifecycle Engagement

**Public-Private-Academic Partnership**

A Ready Workforce

**Scalable:** Extend the program across multiple universities.

**Replicable:** Extend the program across other technology areas.

**Asymmetric:** Produce clearable, knowledgeable workforce

**Nationally coordinated and regionally executed:** network of stakeholders and universities.
Scalable Asymmetric Lifecycle Engagement (SCALE)  
A Public-Private-Academic Partnership (PPAP) Approach to Workforce Development

Government Oversight Committee (GOC): Provides education & workforce development priorities & objectives, technical direction, partnering requirements, programmatic oversight, and funding. GOC consists of service and government representatives to include Air Force, Navy, Army, MDA, NNSA, NASA, and others.

University Consortium Lead: Ensures GOC objectives are met, funding dispersal, and programmatic execution in each technology area. Position can be re-competed as needed (5 years).

Technology Area Leads: Coordinates efforts in their technology area across the consortium, including standardized curricula, continuous learning, certifications, immersive training, internships, and placement.

Leverage T&AM Technical Execution Areas to Develop Communities of Interest
Assesses and aggregates needs within & across stakeholder constituencies
Provides data-driven microelectronics workforce recommendations

Rad Hard: Vanderbilt, AFIT, St. Louis, Brigham Young, Arizona State, Georgia Tech, Purdue, NM State, Univ of TN-Chattanooga, Indiana Univ.
Advanced Packaging: Purdue, Georgia Tech, SUNY-Binghamton, Arizona State
SoC: Ohio State, Purdue, UC-Berkeley
Embedded Systems/Trusted AI: Indiana University, University of Notre Dame, IU-PU Indianapolis
Supply Chain: Purdue, University of Florida

T&AM = Trusted & Assured Microelectronics

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## SCALE Measures of Success

### Scalable Asymmetric Lifecycle Engagement (SCALE)
_A Public-Private-Academic Partnership (PPAP) Approach to Workforce Development_

<table>
<thead>
<tr>
<th>Metric</th>
<th>FY20</th>
<th>FY21</th>
<th>FY 22 (2/1/2022)</th>
<th>FY24 Goal</th>
</tr>
</thead>
<tbody>
<tr>
<td># SCALE Students</td>
<td>25</td>
<td>104</td>
<td>202</td>
<td>200</td>
</tr>
<tr>
<td># Gov’t/DIB Partners</td>
<td>15</td>
<td>26</td>
<td>52</td>
<td>40</td>
</tr>
<tr>
<td># University Partners</td>
<td>6</td>
<td>9</td>
<td>16</td>
<td>15</td>
</tr>
<tr>
<td># Internships</td>
<td>40</td>
<td>65</td>
<td>145-243</td>
<td>200</td>
</tr>
<tr>
<td># Courses</td>
<td>1</td>
<td>4</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td># Students Reached through Courses</td>
<td>25</td>
<td>2740</td>
<td>2740</td>
<td>3250</td>
</tr>
</tbody>
</table>

**Attract, Produce, and Maintain a Ready Workforce**
Summary

• A skilled technical workforce is required to ensure success of DoD modernization initiatives
• T&AM workforce needs encompass those disciplines with the lowest representation of domestic students
• T&AM has invested in the SCALE to:
  - Place cleared personnel in DoD and DIB laboratories
  - Deliver tailored curriculum and provide student access to SOTA tools and processes to produce a readier workforce
  - Scale to meet the national needs; nationally coordinated and regionally executed
Back-up Slides
T&AM WFD Mission

• **Mission:** attract, develop, and maintain a skilled technical workforce to support DoD Trusted and Assured Microelectronics (T&AM)
  - Establish a scalable and replicable framework to address regional workforce needs across the US in key microelectronics technology areas

• **Goals:**
  - Cultivate a replicable and scalable Public-Private-Academic Partnership (PPAP) model to **attract** Science, Technology, Engineering, and Mathematics (STEM) students into TA&M fields of study
  - **Develop** a clearable, knowledgeable workforce to support and execute DoD program workforce modernization needs in microelectronics
  - **Maintain** an agile and adaptive workforce that meets current as well as future U.S. Government needs

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**Attract, Produce, and Maintain a Ready Workforce**
The PPAP Model – A National Network

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# SCALE University Partners

## Target Institutions

<table>
<thead>
<tr>
<th>KEY</th>
<th>Government</th>
<th>Federally Funded Research and Development Centers</th>
<th>Industry</th>
</tr>
</thead>
</table>

### Partners (Institution Topic Areas*)

| P1  | Purdue University, West Lafayette, IN (RH, HIAP, SC, ESS, SoC) |
| P2  | Air Force Institute of Technology, Wright-Patterson Air Force Base, OH (RH) |
| P3  | Arizona State University, Tempe, AZ (RH, HIAP, SC) |
| P4  | Brigham Young University, Provo, UT (RH) |
| P5  | Carnegie Mellon University, Pittsburgh, PA (ESS, **) |
| P6  | Draper Laboratory, Cambridge, MA (RH) |
| P7  | Georgia Institute of Technology, Atlanta, GA (RH, HIAP, SC, ESS, SoC) |
| P8  | Indiana University, Bloomington, IN (ESS, **) |
| P9  | Massachusetts Institute of Technology, Boston, MA (ESS, **) |
| P10 | Sandia National Laboratory, Albuquerque, NM (RH) |
| P11 | Sandia National Laboratory, Livermore, CA (RH) |
| P12 | St. Louis University (RH) |
| P13 | State University of Binghamton, NY (HIAP) |
| P14 | University of California, Berkeley, CA (ESS, SoC) |
| P15 | University of California, San Diego, CA (ESS) |
| P16 | University of Florida, Gainesville, FL (SC) |
| P17 | University of Michigan, Ann Arbor, MI (RH) |
| P18 | Vanderbilt University, Nashville, TN (RH) |
| P19 | The Ohio State University, Columbus, OH (SoC) |

*RH = Radiation Hardened, HIAP = Heterogeneous Integration/Advanced Packaging, SC = Supply Chain, ESS = Embedded Systems Security, SoC = System on Chip

**Institution was part of the launch partnership for SoC
Engagements and Co-Sponsors

Department of Defense
DoD STEM
National Security Commission for Artificial Intelligence

Office of Personnel & Laboratories

Draper

Sandia National Laboratories

National Nuclear Security Administration

NAVSEA

NSF

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CSME – SCALE Synergy

• Access SOTA commercial technology capabilities
  - Designers need to be trained in a “zero-trust” approach with multiple commercial partners

• CSME provides SCALE graduate trainees experience with cutting-edge research in secure IC design
  - Skills will be relevant to both on-shore and off-shore foundries

  ▪ Opportunity to participate in IC tape outs using TSMC technology*
  ▪ SCALE provides DoD internships, mentoring, relationship building

* No anticipated restrictions on ability to work with other foundry technologies after graduation

Source: N. Petta, OSD

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Federal, industry, and state co-investment to support US training fellowships and research vectors defined by investors. Unique access to State-of-the-Art technology nodes to promote secure microelectronics ecosystem. RFP process will be used to solicit proposals from member universities, which are selected through a competitive process evaluated by investors. University cost-share required on funded projects. State funds stay within state.

Purdue hosts CSME with Co-Directors: Appenzeller, Raghunathan; Universities that participate in Microelectronics Workforce Consortium eligible to join CSME

**HI/AP Focus Area**

Purdue Lead: Ganesh Subbarayan
Team: Purdue, SUNY, GA Tech

*US pipeline, curriculum, internships undergrad and grad curriculum*

~$525K/yr for Y2-4; Y5 not yet funded

**SOC Design Focus Area**

Ohio State Lead: TBD
Team: Ohio State, Purdue, GaTech

*US pipeline, curriculum, internships undergrad and grad curriculum*

~$500K/yr for Y1; Y2-5 not yet funded

**Center for Secure Microelectronics Ecosystem (CSME)**

OSD/DoD co-investment in US graduate training fellowships and research at State-of-the-Art with respect to commercial nodes and secure microelectronics

~$1.0MK/yr for Y1 ($250K HI-AP, $750K SOC); Y2-Y4 funded for HI-AP; Y2-5 for SOC and Y5 for HI/AP not yet funded

$1M/year = 18-20 graduate fellowships

TSMC, founding industry member

$1 million/year with a commitment for 5 years – plus in-kind contributions of multi-project wafer runs

*Active Discussions*: Intel, IBM, Synopsys, Draper and others

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CSME will investigate, design and evaluate technologies that ensure the security principles of confidentiality, integrity and availability for Integrated Circuit (IC) design, fabrication and packaging.

**IC Design**
- **RV1** Holistic approaches for zero-trust IC fabrication
- **RV2** Performance and cost tradeoffs of security techniques
- **RV3** Design, verification, testing and characterization of foundational secure circuit primitives
- **RV4** Unique opportunities for secure microelectronics with beyond-CMOS devices
- **RV5** Extended lifetime and behavior under extreme conditions for advanced technology nodes
- **RV6** Materials Assurance for Trusted Package Behavior
Execution Goals:

- Develop the Trusted AI Consortium and Public-Private-Academic Partnership (PPAP) Model
- 5 Graduate Research Projects across 3 Universities
- Research Projects are providing the tools, methodologies, and frameworks to assure AI:
  - Develop tools, techniques, and procedures to measure human trust of AI/ML algorithms linked with the trustworthiness of the AI/ML system to help inform stakeholders about the correct levels of trust across the developmental process
  - Develop methods to reduce Data Source Bias and create Modularity
  - Develop a Cybersecurity and Risk Model to ensure ML algorithms maintain robustness in situations where a given set of sensors used to train the system are no longer used in the system:
  - Develop ways to measure a system’s success during the full lifecycle
- USG oversight of projects and student interaction
- Sponsoring US student team at Indy Autonomous Challenge (IAC)
- Add additional staff for SCALE advocacy and strengthening the PPAP

AI/ML algorithms ultimately get executed in hardware, which is the root of trust and foundational to the success of any system. To expedite the deployment of trusted AI/ML solutions for embedded systems applications, AI/ML algorithms being executed must be trusted. The intent of the embedded systems security consortium aims to develop the workforce with the necessary skills to ensure the secure operation of microelectronics in these systems.
Enhancing the US Asymmetric Advantage in a Trusted AI Workforce

Prior State (Past)
- Infrequent security training
- Public domain fundamental knowledge
- Basic research and commercial products

FY-21 Model (Current)
- Train all US citizen students and faculty in ITAR, EAR, CCL
- Identify curricular gaps targeting DOD/GOV/DIB prioritized KSAs
- Mentored, DOD-relevant differentiated research projects
- Establish multi-university consortium and cross-university collaborations

Enhanced (Future)
- Train all US citizen students and faculty in OPSEC & design for security
- Continuously update and combine courses for highly asymmetric curricula
- DOD mission-relevant senior design projects
- Expand mentored, DOD-relevant differentiated research projects

Human Trust of AI/ML, Measures ● Metrics, and Testing ● Data Source Bias and Modularity ● Cybersecurity + Risk Model

Level of Asymmetry

A Ready Workforce

OPSEC Training
Trusted AI Curriculum
Trusted AI Projects, Research, and Internships
Workforce Recommendations for the National Security Commission for Artificial Intelligence (NSCAI)

Recommendations will be incorporated in NSCAI’s Q3 report (Sept 2020)
Chairman

Recommendations for the Microelectronics Workforce Prototype, SCALE

“At minimum, $24.7 million per year over the next decade of additional funds are needed to address each critical technical area - $122.36 million per year over the next decade of additional funds are needed to initiate a parallel AI-specific consortium…” https://www.nscai.gov/home
# Projected Yield for 10-YR Investment

<table>
<thead>
<tr>
<th>Year One</th>
<th>Year Ten</th>
<th>Year Thirty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,000 GOV Work Years, at minimum, completing the maximum service agreement of 4:1</td>
<td>10,000 GOV Work Years, at minimum, completing the maximum service agreement of 4:1</td>
<td>Assume 50% attrition rate after the 4 year service and total service of 30 years for remaining population: 42,500 GOV Work Years</td>
</tr>
<tr>
<td>Assume equal number of graduates joining the DIB</td>
<td>Assume equal number of graduates joining the DIB</td>
<td>Assume equal number of graduates joining the DIB and same attrition rate</td>
</tr>
<tr>
<td>Total: 2,000 Work Years</td>
<td>Total: 20,000 Work Years</td>
<td>Total: 85,000 Work Years</td>
</tr>
<tr>
<td><strong>Total/Vertical: 400 Work Years</strong></td>
<td><strong>Total/Vertical: 4,000 Work Years</strong></td>
<td><strong>Total/Vertical: 17,000 Work Years</strong></td>
</tr>
</tbody>
</table>

*Does not include personnel continuing to work after the 4-year service period.*

## Years 1 - 10

- Incoming employees familiar with applied research that aligns with DoD priorities
- Recruiting advantage through early (K-12) exposure to the program
- Security-policy savvy hires already trained in ITAR, EAR, CCL, and related regulations

**Assumes Annual Investment Over 10-Years**

**Assumes 50 Students/Year Per Vertical with a Scholarship for Service**

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