Consolidation: 1998 through present

NIST

SRC nanoelectronics programs were crucial in a time of uncertainty and significant consolidation.

NRI and nCORE have created an environment that influences research well beyond the programs that they directly fund.

Number of Semiconductor Manufacturers with a Cutting Edge Logic Fab										
SilTerra										
X-FAB										
Dongbu HiTek										
ADI	ADI									
Atmel	Atmel									
Rohm	Rohm									
Sanyo	Sanyo									
Mitsubishi	Mitsubishi									
ON	ON									
Hitachi	Hitachi									
Cypress	Cypress	Cypress								
Sony	Sony	Sony								
Infineon	Infineon	Infineon								
Sharp	Sharp	Sharp								
Freescale	Freescale	Freescale								
Renesas (NEC)	Renesas	Renesas	Renesas	Renesas						
Toshiba	Toshiba	Toshiba	Toshiba	Toshiba						
Fujitsu	Fujitsu	Fujitsu	Fujitsu	Fujitsu						
TI	TI	TI	TI	TI						
Panasonic	Panasonic	Panasonic	Panasonic	Panasonic	Panasonic					
STMicroelectronics	STM	STM	STM	STM	STM					
HLMC	HLMC		HLMC	HLMC	HLMC					
IBM	IBM	IBM	IBM	IBM	IBM	IBM				
UMC	UMC	UMC	UMC	UMC	UMC		UMC			
SMIC	SMIC	SMIC	SMIC	SMIC	SMIC		SMIC			
AMD	AMD	AMD	GlobalFoundries	GF	GF	GF	GF			
Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung
TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC
Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel
180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm

https://en.wikichip.org/wiki/technology_node

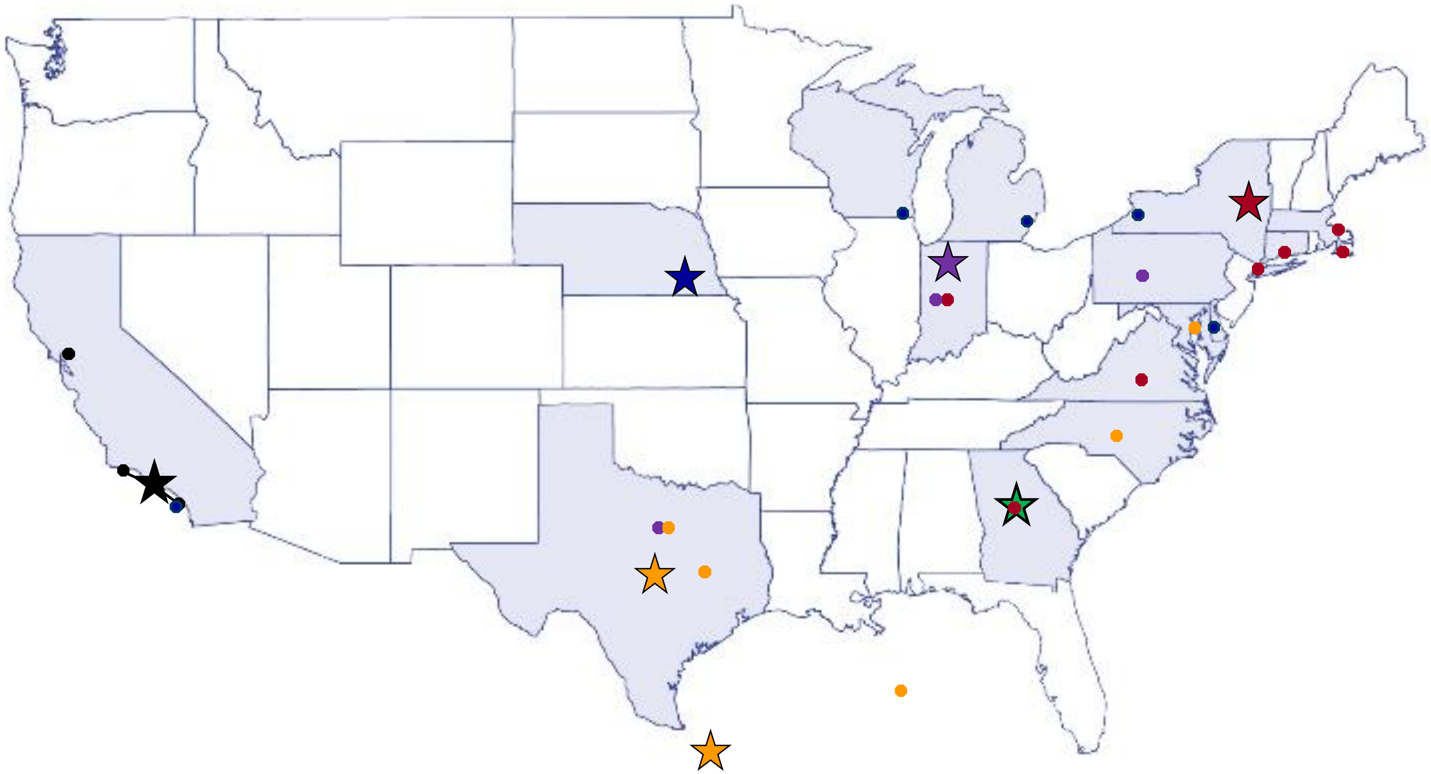
NIST Partnerships - NRI

Nanoelectronics Research Initiative (NRI) *(Funding Period: 2006-2019)*
Search for the low-power switches beyond CMOS

2013–2017 — CNFD

- ME-MTJ
- FeFET & FTJ
- Spin wave

U. Nebraska-Lincoln
U. Delaware
U. Wisconsin-Madison
U. Oakland
SUNY Buffalo
UC-Irvine



2008–2012 — MIND (Nanoelectronics • Architectures; Midwest Institute for Nanoelectronics Discovery)

Notre Dame
Purdue **Penn State**
UT-Dallas

- Tunnel FET
- NanoMagnet Logic

2006–2017 — INDEX

SUNY-Albany
Purdue **Columbia**
Harvard **U. Virginia**
Georgia Tech
MIT

- Graphene PN junction
- Charge-spin logic

2006–2012 — WIN (Western Institute of Nanoelectronics)

- SpinFET
- Spin wave
- NanoMagnet Logic
- Spin Hall devices

UC Los Angeles
UC Berkeley
UC Irvine
UC Santa Barbara

2006–2017 — SWAN (South West Academy of Nanoengineering)

- BisFET
- Interlayer Tunnel FET

UT-Austin **Rice**
UT-Dallas **NCSU**
U. Maryland **Texas A&M**

2015–2017

Benchmarking
Georgia Tech

NIST Partnerships - nCORE

Innovative Materials and Processes for Accelerated Compute Technologies (IMPACT)
Stanford, Purdue, RPI, UCSD, Notre Dame, Yale, U Maryland

NEW LIMITS: NEW materials for logIc, Memory and InTerconnectS (NEW-LIMITS)
Purdue, UTD, Michigan, Penn State, Stanford

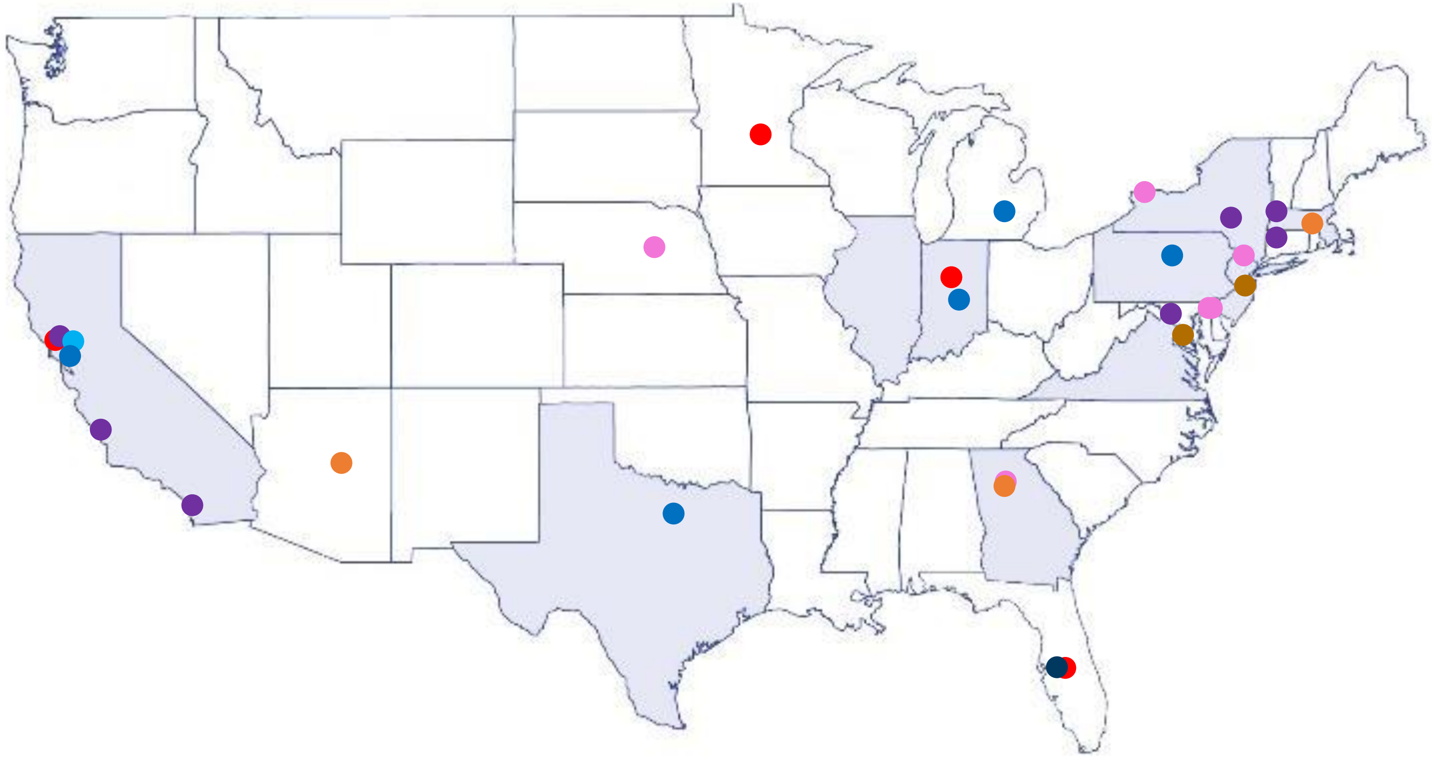
SMART: Spintronic Materials for Advanced infoRmation Technologies)
University of Minnesota, Georgetown, University, Pennsylvania State University, MIT, University of Maryland

Probabilistic Spin Logic for Low-Energy Boolean and Non-Boolean Computing (CAPSL)
Purdue, Minnesota, Berkeley, UCF

A new non-volatile electrochemical transistor as an artificial synapse: device scaling studies
Stanford

Metal-insulator transitions for low power switching devices
UCSB, Ohio State

Energy-efficient analog computing with emerging memory devices
UCSB, UMass



Durable, Energy-Efficient, Pausable Processing in Polymorphic Memories (DEEP3M)
Cornell

Interconnects Beyond Cu
Columbia, RPI, UCF, MIT

Nanophotonic Neuromorphic Computing
Princeton, GWU

Non-Volatile In-Memory Processing Unit: Memory, In-Memory Logic and Deep Neural Network
UCF

Energy-Efficient Artificial Intelligence with Binary RRAM and Analog Epitaxial Synaptic Arrays
ASU, MIT, Georgia Tech

Antiferromagnetic Magneto-electric Memory and Logic (AMML)
UNL, U Buffalo, Georgia Tech, NYU, U Delaware

nCORE and NRI Statistics

NIST

Preserving U.S. leadership:

- Exploring new approaches to low-energy devices and technologies that can outperform tradition Silicon CMOS technologies
- Growing the future STEM workforce

Data	NRI (2006 – 2019)	nCORE (2018 – 2022)
Participating universities	60	30
Participating students	757	248
Student internships	159	16
Student hiring - To industry - To academia - To government / national labs	 257 118 31	 38 15 3
Number of industry sponsors	6 at the start; 4 at the end	12
Industry liaisons	144	217
Publications	1,564	1275
Patents	29 issued	7 issued, 46 applications filed

nCORE Sponsors

intel, IBM, Micron, arm, Analog Devices, Raytheon Technologies, Lockheed Martin, Northrop Grumman, SK hynix, Samsung, EMD Performance Materials, tsmc

2D Materials and Devices are getting ready for the next stage

Joerg Appenzeller

School of Electrical and Computer Engineering
& Birck Nanotechnology Center
Purdue University, West Lafayette, IN 47907

appenzeller@purdue.edu

SRC-SIA Webinar
September 29, 2022

<u>The problem:</u>

BEOL RC delay issues are becoming the bottleneck for chip performance since

a) the resistivity (not just the resistance) of copper interconnects and vias increases when scaling
b) a substantial portion of the space in interconnects and vias needs to be reserved for liners and Cu diffusion barriers

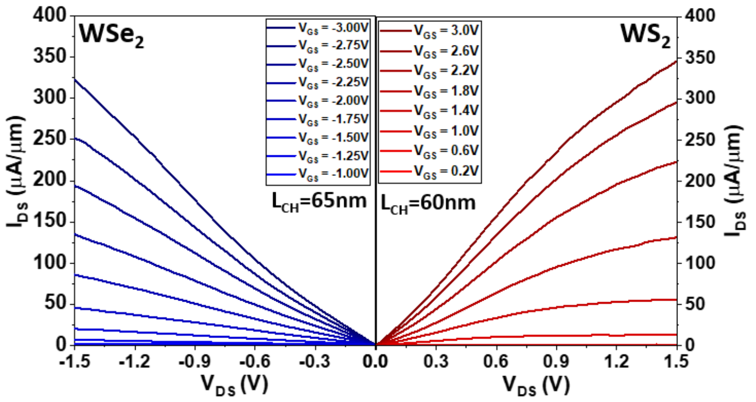
- NEW LIMITS has demonstrated BEOL compatible growth of 2D materials (e.g. TaS_2) that show the desired performance specs in terms of adhesion, diffusion barrier properties and resistivity!

Two-dimensional (2D) materials and their applications - *Logic*

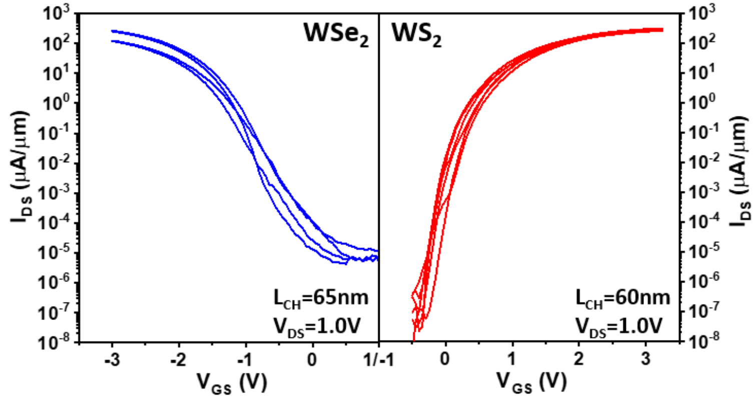
The problem:

BEOL compatible high performance CMOS solutions are rare since

a) low temperature growth negatively impacts the transport properties
b) achieving high performance in both novel n-FETs and p-FETs is challenging



- ➢ NEW LIMITS has demonstrated output and transfer characteristics in WS$_2$ and WSe$_2$ FETs showing the desired current drive capability at scaled voltages for both, n-type and p-type 2D-based FETs!



The problem:

BEOL compatible fast, non-volatile memory solutions operating at small voltages with good retention and endurance are challenging since

a) conventional resistive random access memory (RRAM) is showing degradation over time and is challenging to scale
b) Phase change memory (PCM) are relatively slow and show reliability issues

- NEW LIMITS has demonstrated reproducible ~ns switching speeds in novel $MoTe_2$ memory elements that operate based on an electric-field induced crystal-phase to crystal-phase transition!

Unleash Innovation

Paradigms for Building Realistic Modeling Capabilities in the Next Decade

Blanka Magyari-Köpe

Technical Manager
R&D TCAD, TSMC

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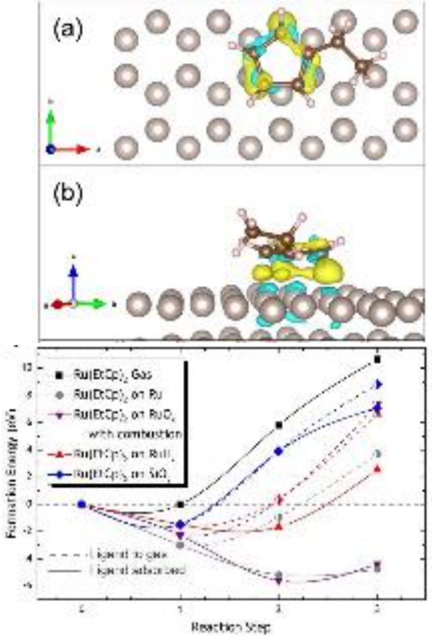
TSMC Property

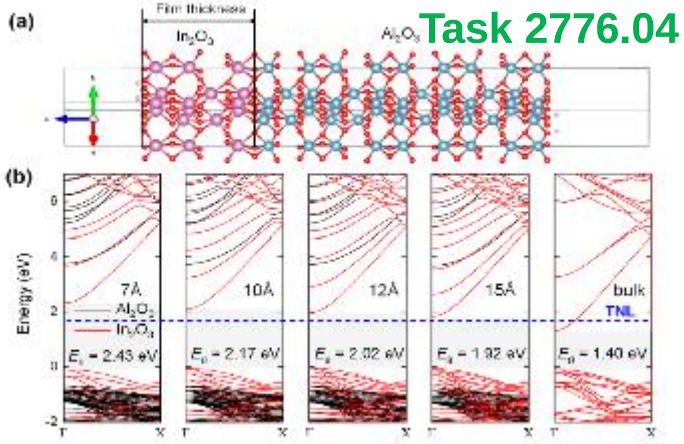
Highlights on nCore/JUMP Material Simulations Projects and Application Areas

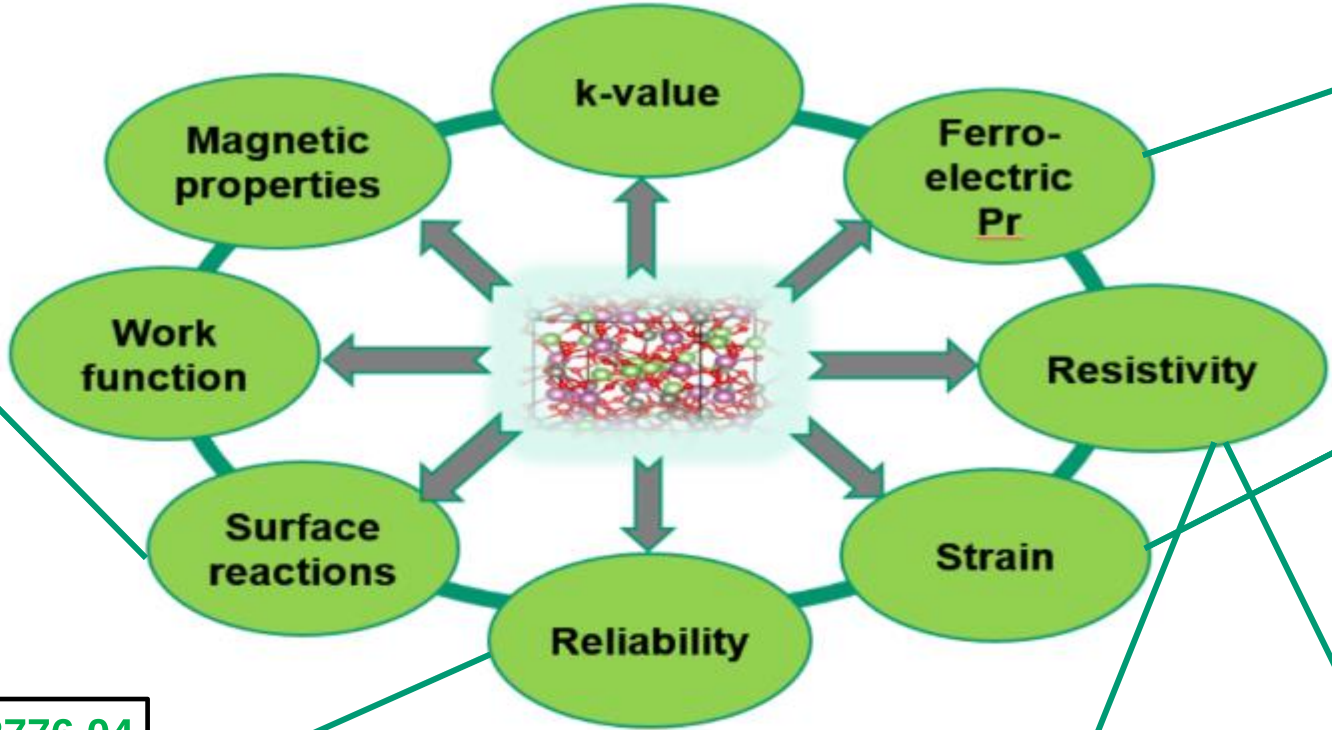
Unleash Innovation

Task 2776.02

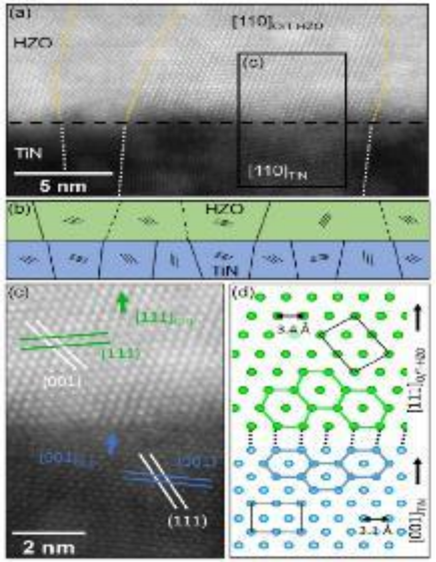


Task 2776.04

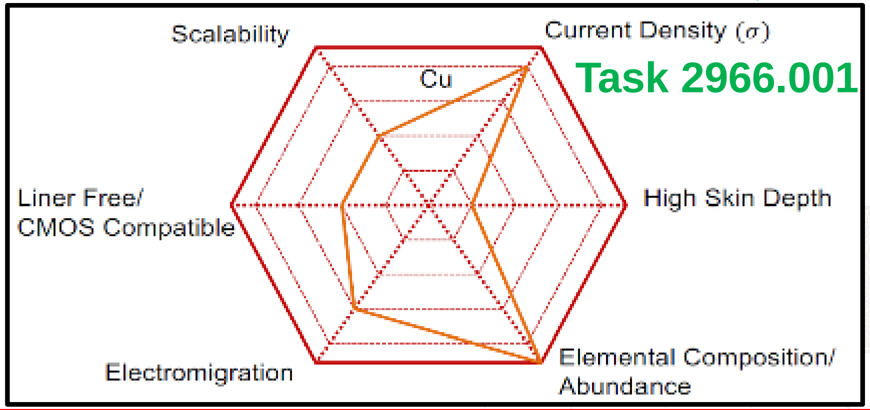




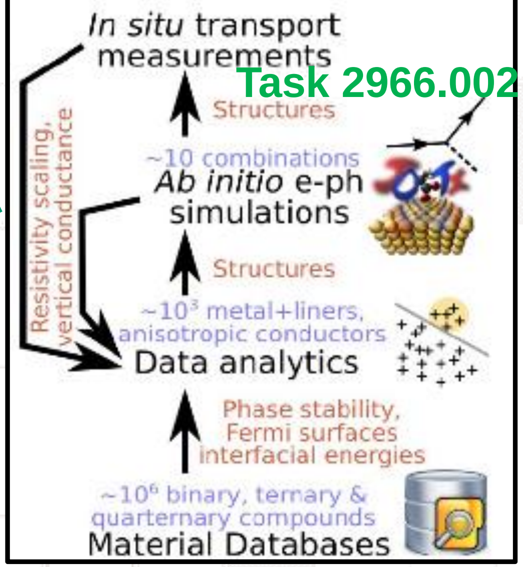
Task 2776.073



Task 2966.001



Task 2966.002

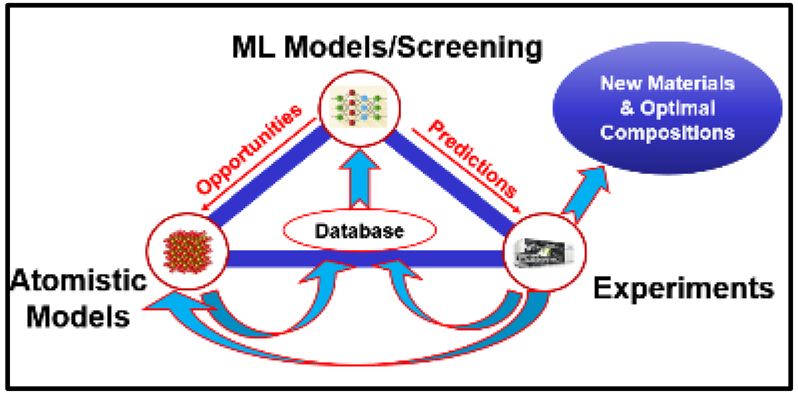


Decadal Plan: Building a Functional Virtual Fab

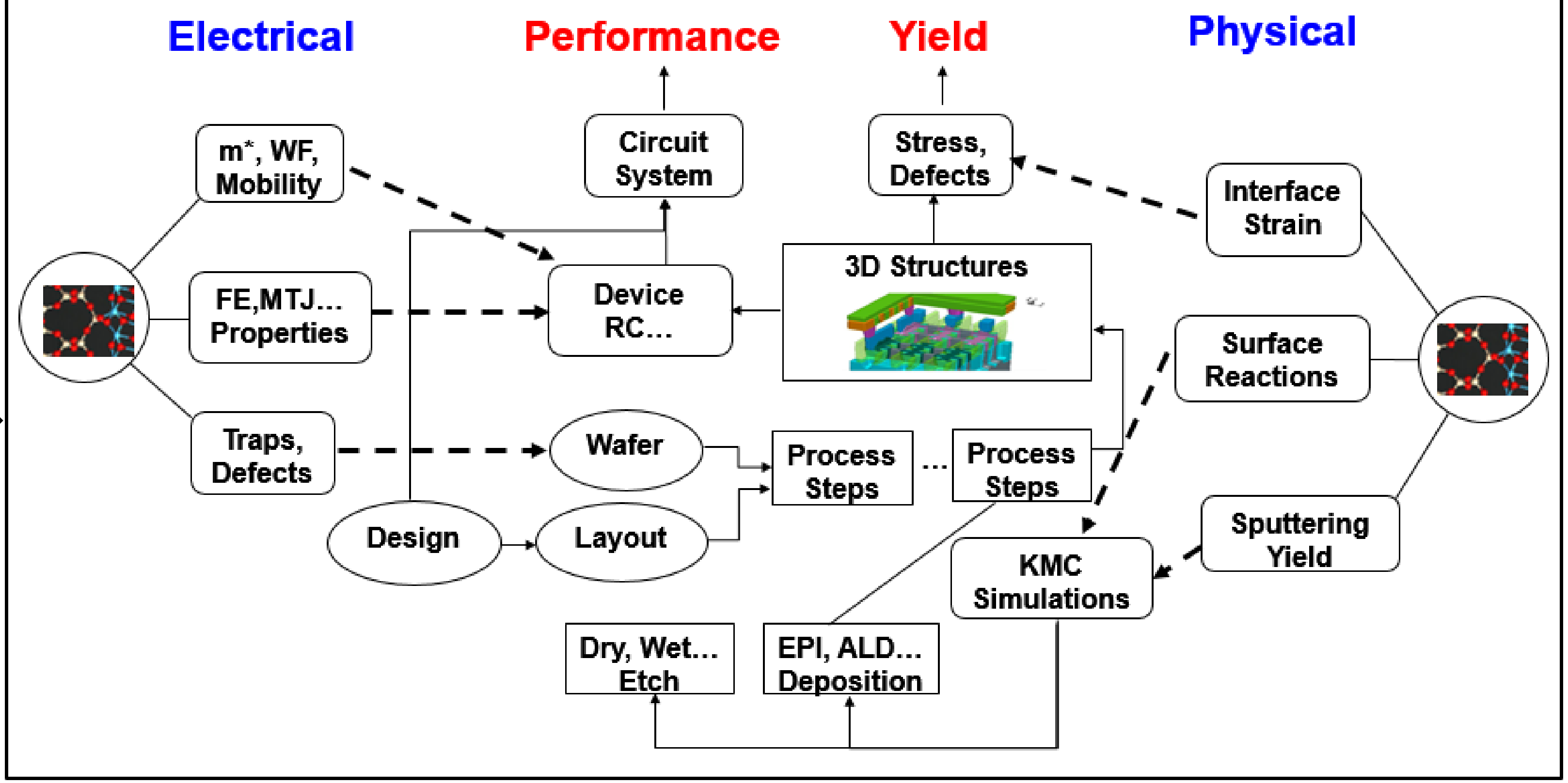
From fundamental material properties to system level

Using old tricks and incorporating novel techniques:

1. Automation
2. High-throughput screening
3. Multiscale
4. Machine learning



Virtual Fab Concept

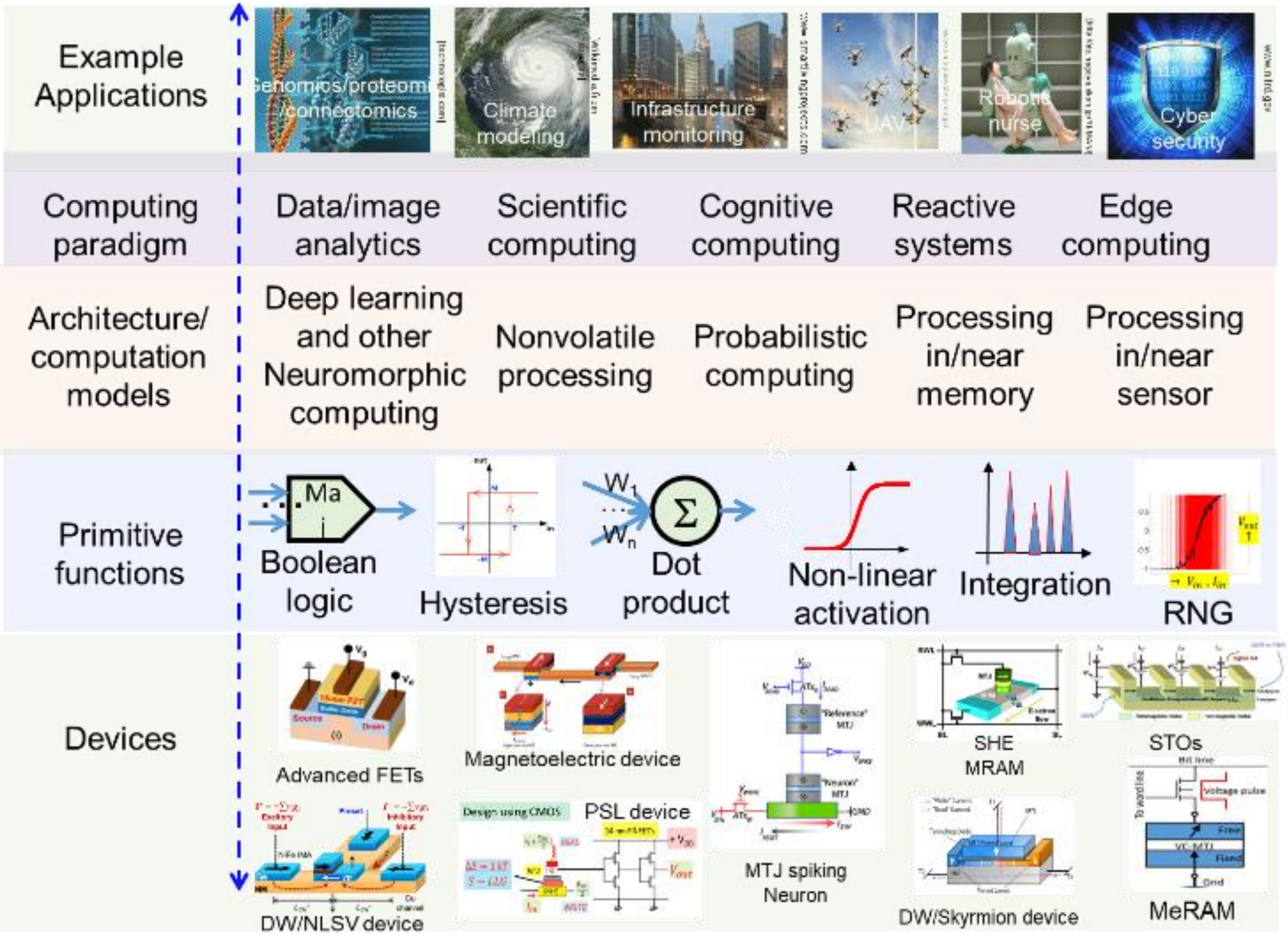


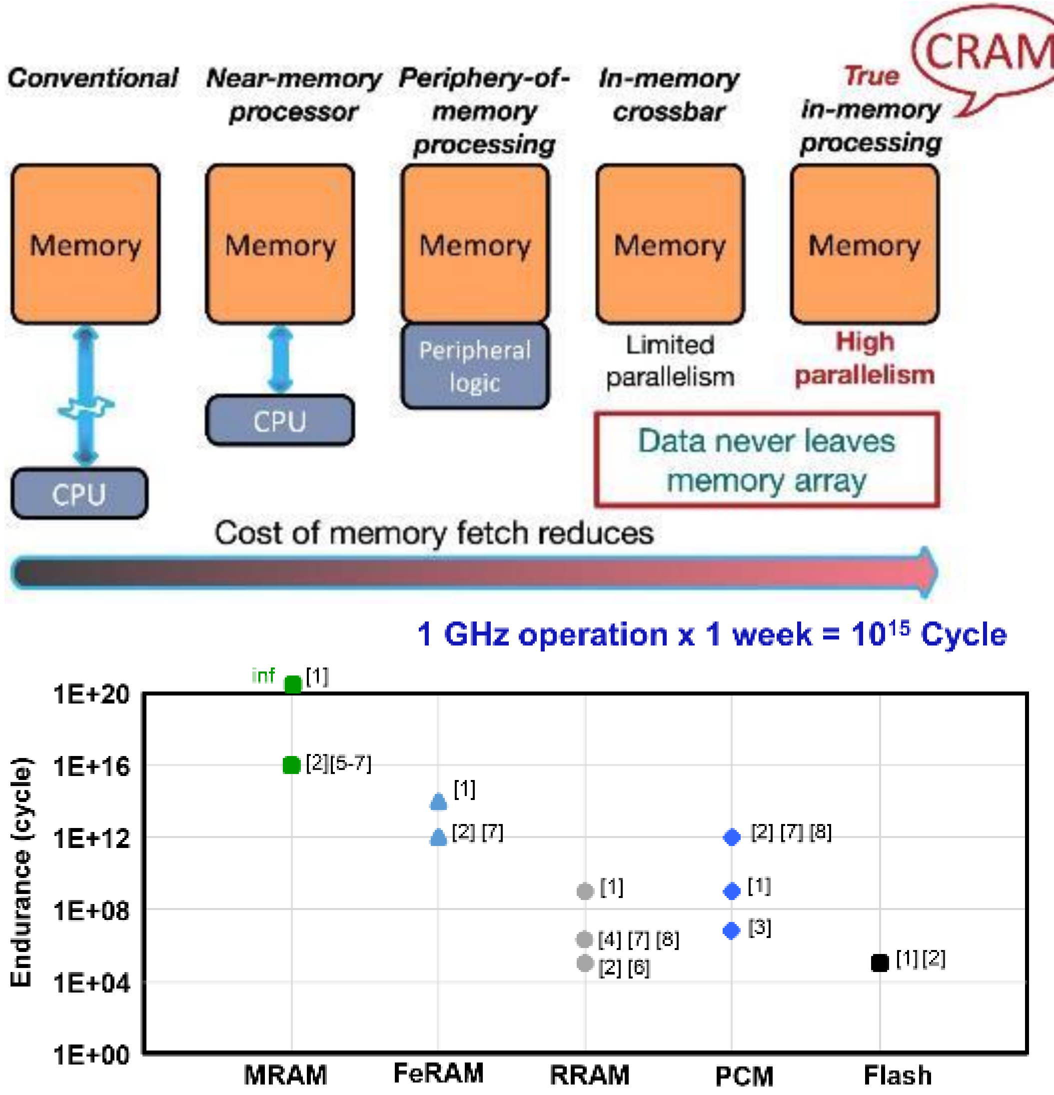
From New Physics, Novel Materials to Super-Performance and Energy Efficient Devices (SPEED) and Enabled Extremely Energy-Efficient Systems

Jian-Ping Wang
Distinguished McKnight University Professor & Robert F. Hartmann Chair
Electrical and Computer Engineering Department
University of Minnesota

SRC-SIA Webinar on Collaboration towards Decadal Plan goals
09/29/2022

Address the Energy Consequences of Information from a Vertical Integrated Effort



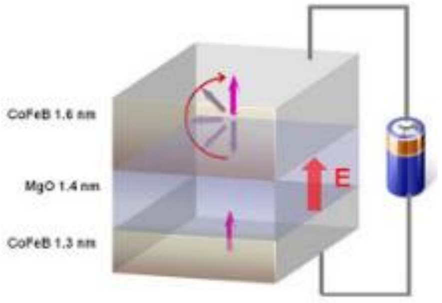


J. P. Wang, et al, Proceeding of DAC 2017, article 16, “Spintronics: A Potential Pathway to Enable an Exponential Scaling for the Beyond-CMOS Era”

New Physics: Voltage-Controlled Exchange Coupling (VCEC)

Two-terminal

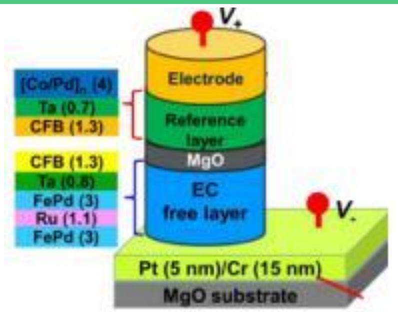
VCMA + STT



- p-MTJs switched by VCMA + STT

W. Wang, et al., Nat. Mater. (2012)

VCEC + STT (PMA + pSAF)

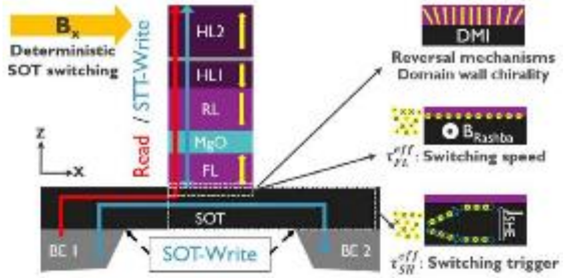


- SAF free layer, **solution for fast switching and immunity of external field**;
- SAF p-MTJ switched by VCEC with current density **~ 10^5 A/cm²**
- **10x reduction** of the current density vs state-of-art; **50 ps** switching (predicted)

D. Zhang, et al, JP Wang, Nano Letters (2022)

Three-terminal

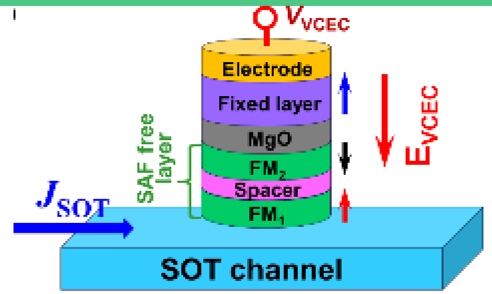
STT+SOT (PMA)



- p-MTJ field-free switched by STT + SOT.

K. Garello, et al., IEEE Symposium on VLSI Circuits (2018); M. Wang, et al Nat. Electronics (2018);

VCEC+SOT (PMA + pSAF)

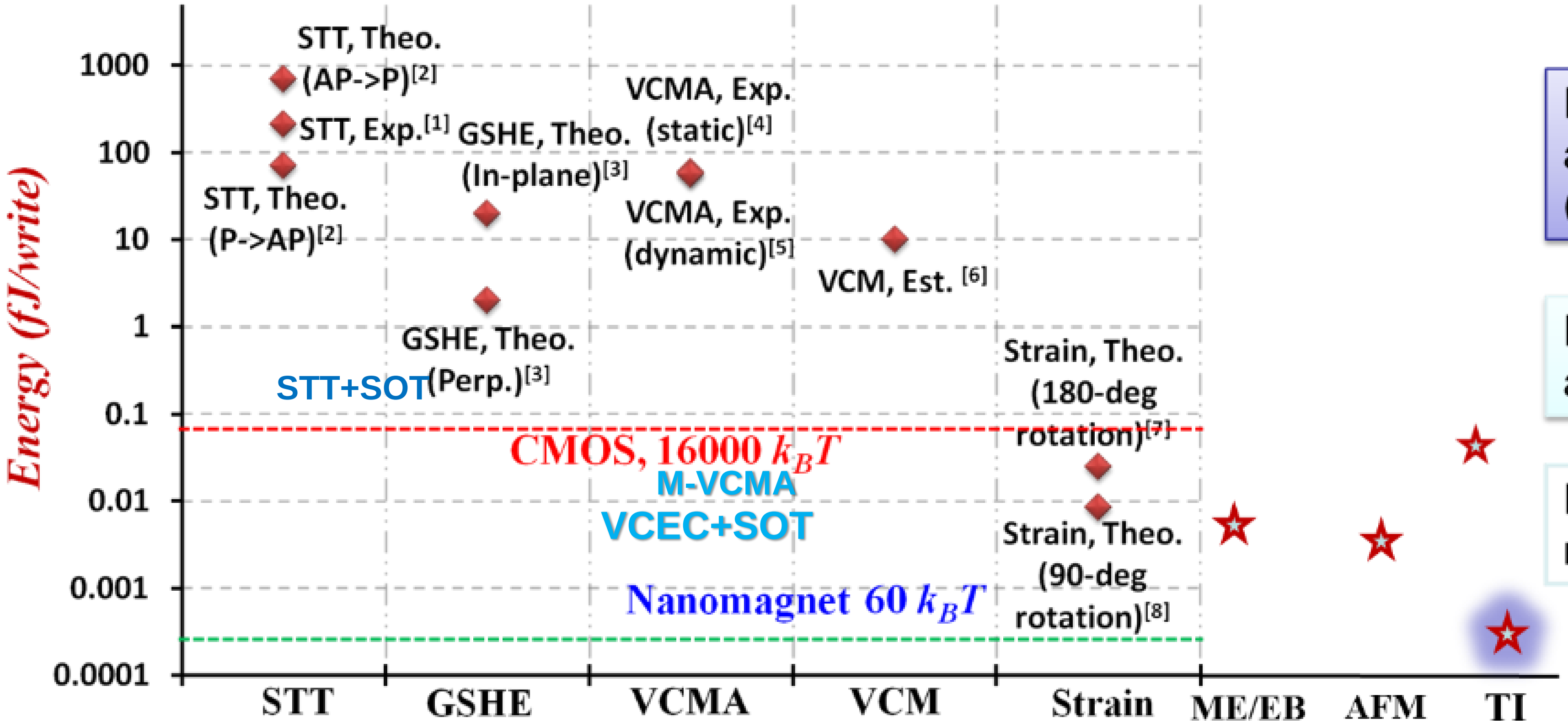


- SAF p-MTJ switched by VCEC + SOT; **VCEC ~ 10^3 A/cm²**
- **100x reduction** of the current density vs state-of-art
- **A solution for the external-field-free switching with large SOT**
- SOT can provide ultrafast speed (~10ps);

B. Zink, et. al. J. P. Wang, Advanced Electronic Materials (2022)

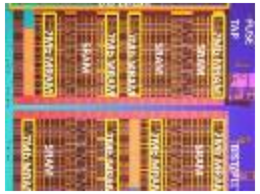
J. P. Wang, U. Minnesota

New Materials & Switching Mechanisms



SOT

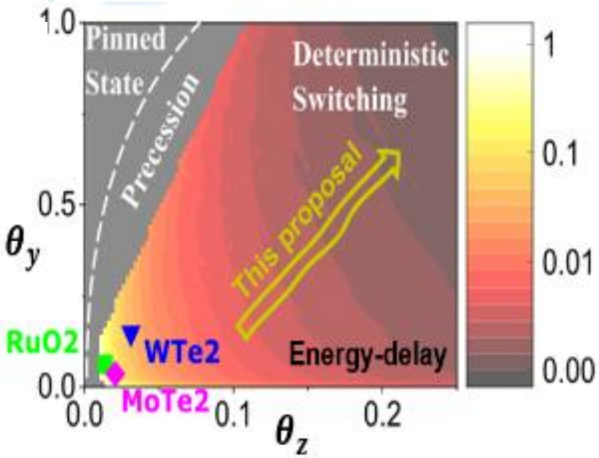
First application (STT-RAM)



For example MRAM in 22-nm FinFET process (Intel) & many others

New/Specific applications

Drop-in replaceme



ME/EB: Magnetoelectrical/Exchange bias
AFM: antiferromagnetic
TI: Topological materials

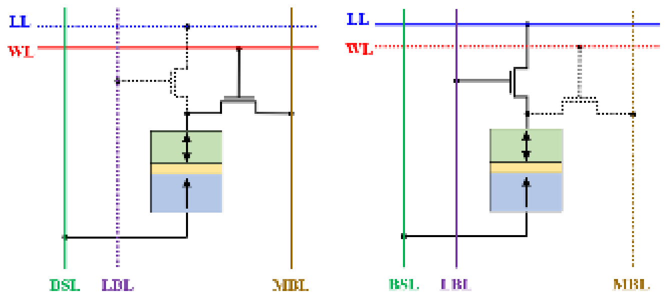
- New topological materials predicted by nCORE/SMART center can enable 1000x energy-delay reduction
- Topological materials based devices: the MESO device concept proposed by Intel and the CoMET device concept proposed by Minnesota outperform CMOS operation energy.

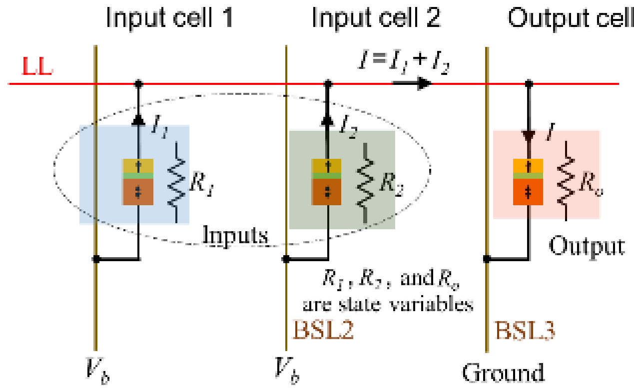
J. P. Wang, U. Minnesota

Device Functionality Enabled Energy Efficient Architecture: Spike Neural Networks (SNN) in Computational Random Access Memory (CRAM)

CRAM–SNN energy consumption is **100x** less than state-of-art SNN designs due to seamless memory access and more efficient topology

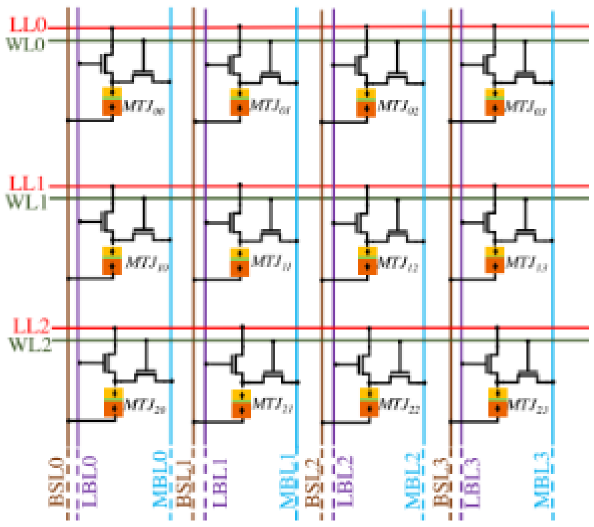
Memory write/read + Logic



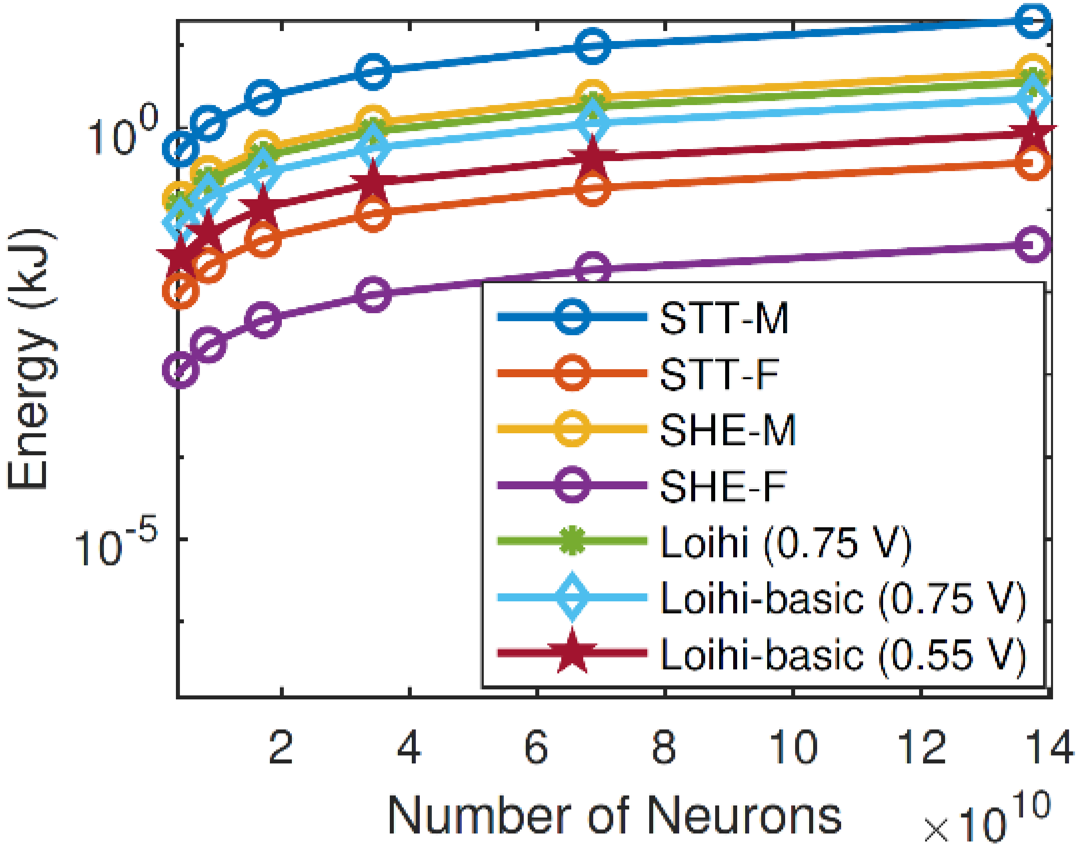


*J. P. Wang and J. D. Harms, US Patent 9,224,447 B2 (**2015**)*

Spin-transfer-torque (STT)-CRAM



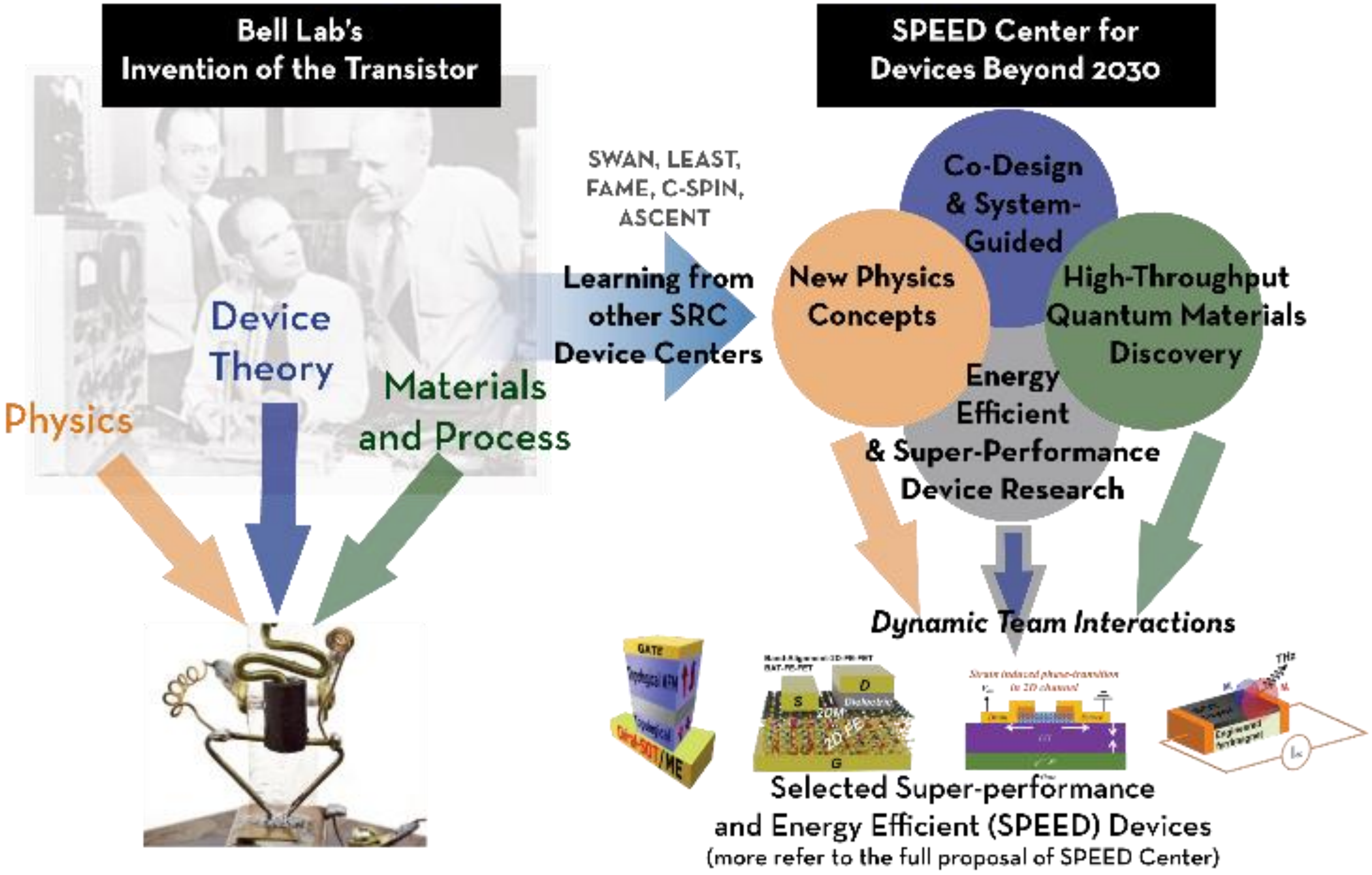
Z. Chowdhury et al, U. Karpuczu, J. P. Wang, *IEEE Computer Architecture Lett*, 17, (**2017**) 42.

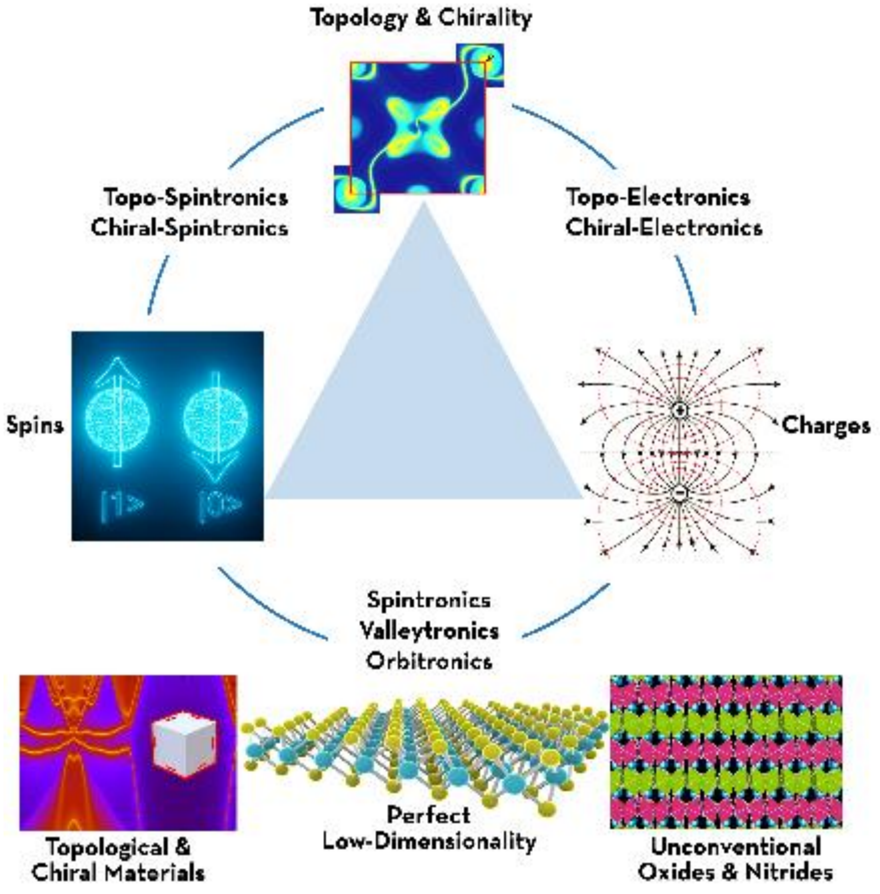


Cilasun et al. Sapanekar, Wang, Karpuczu, “Spiking Neural Networks in Spintronic Computational RAM”, ACM TACO 2021

J. P. Wang, U. Minnesota

Collaboration Towards Decadal Plan Goals:
From New Physics, Novel Materials to
Super-Performance and Energy Efficient Devices
and Enabled Energy-Efficient Systems

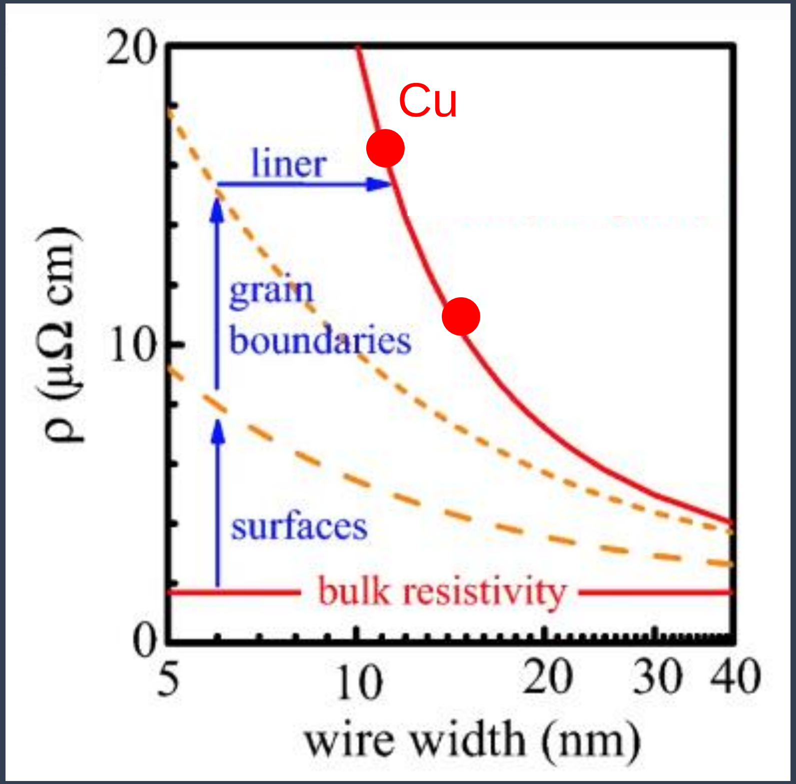




SPEED Consortium (current): 23 PIs at 13 universities

J. P. Wang, U. Minnesota

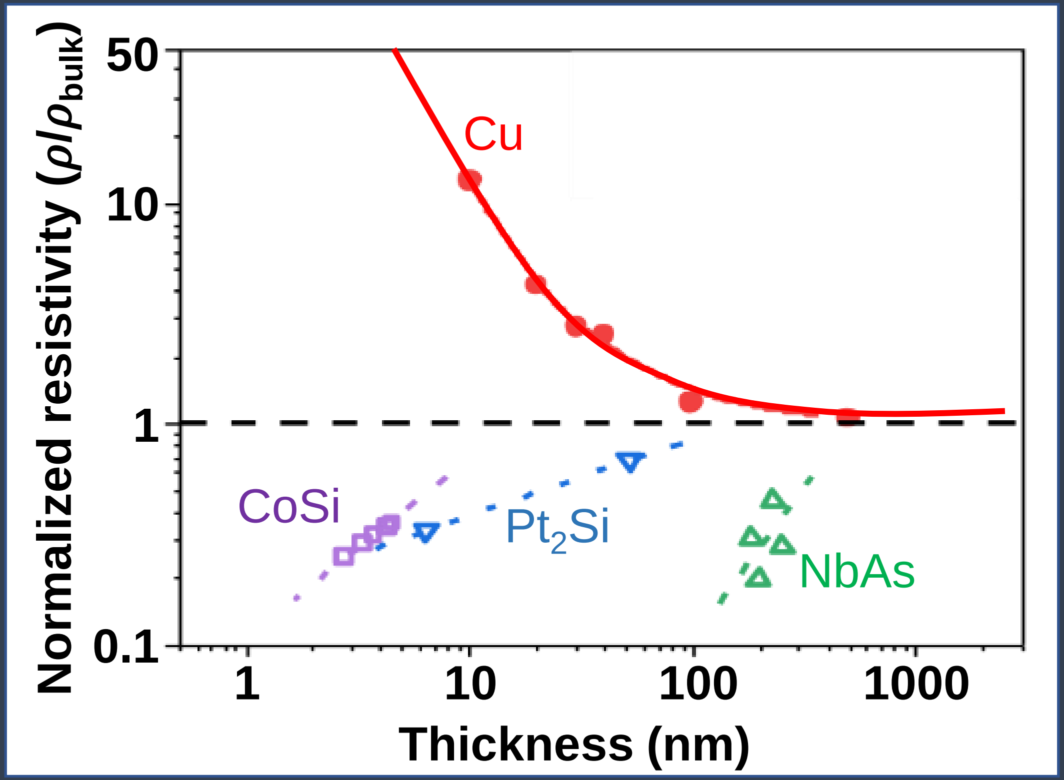
Interconnect Challenge



Gall, et. al. *MRS Bulletin* **46** 959 (2021)

- Unacceptable signal delays
- Dynamic power dissipation

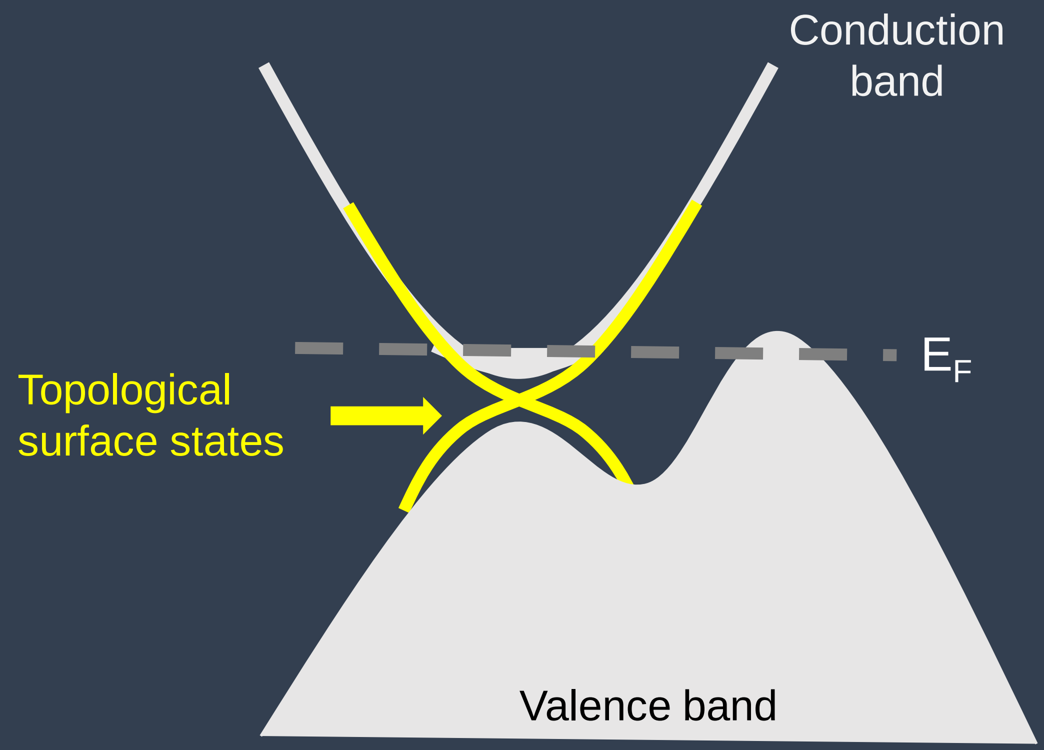
Ideally, decreasing ρ for decreasing dimensions



Nature Materials 2019, 18, p.482
APL 2008, 92, p.203114
Crystal Design & Growth, 2009, 9, p.4514

CoSi, Pt_2Si, and NbAs are all topological metals

Topological Semimetal



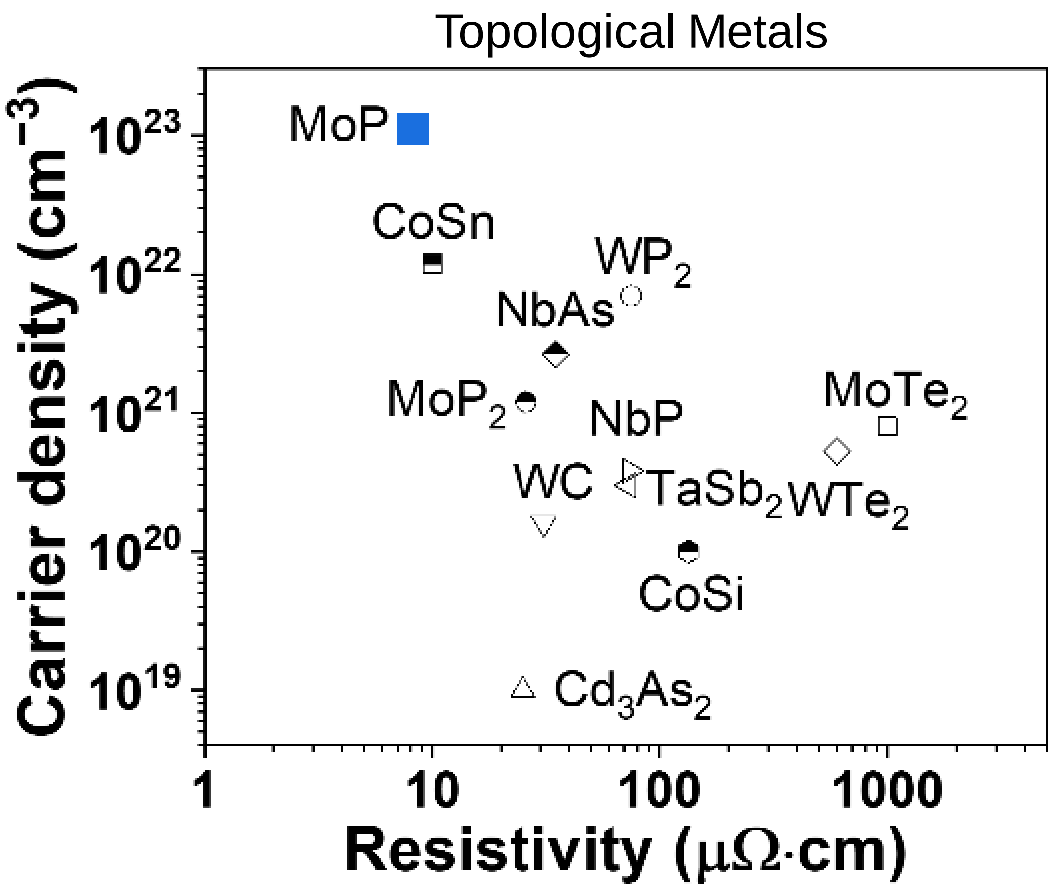
- Topological surface states = superb transport properties
- ~ 25 % of all known materials predicted topological

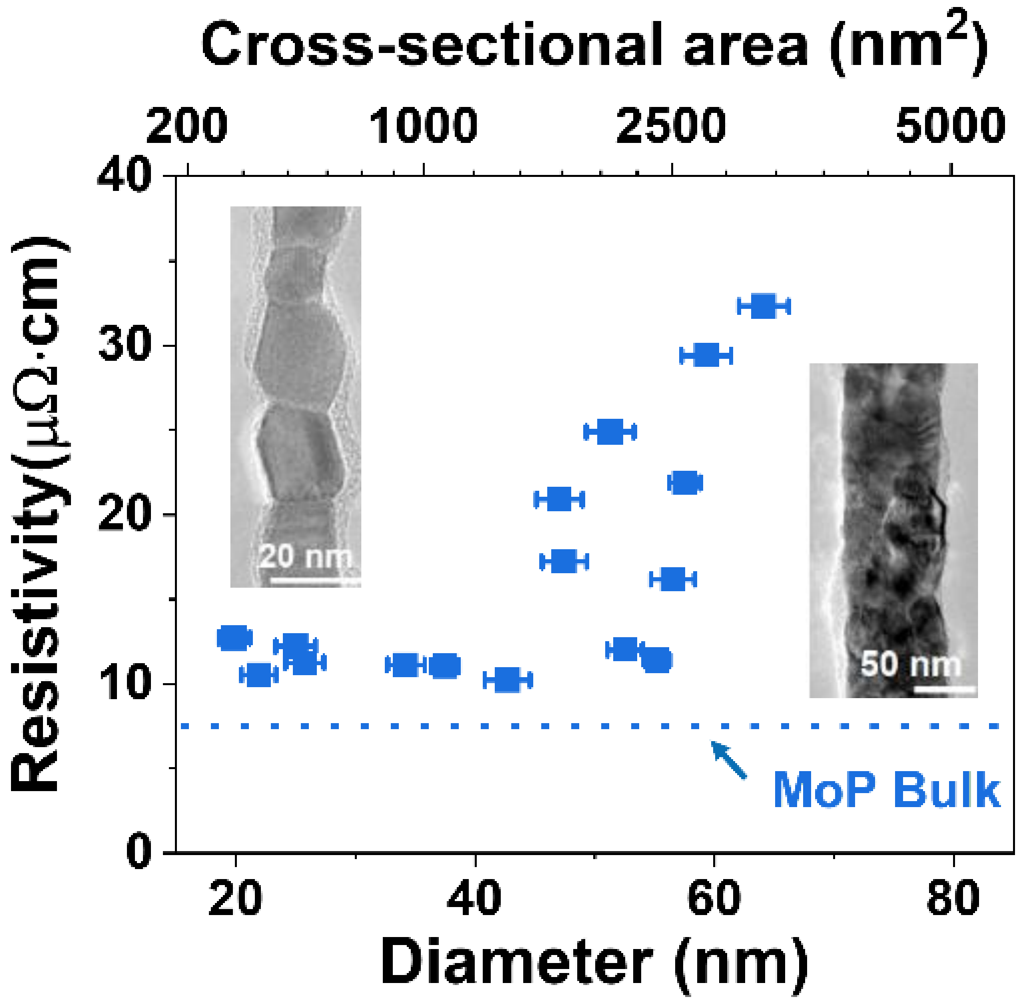
IMPACT

Innovative Materials and Processes for Accelerated Compute Technologies

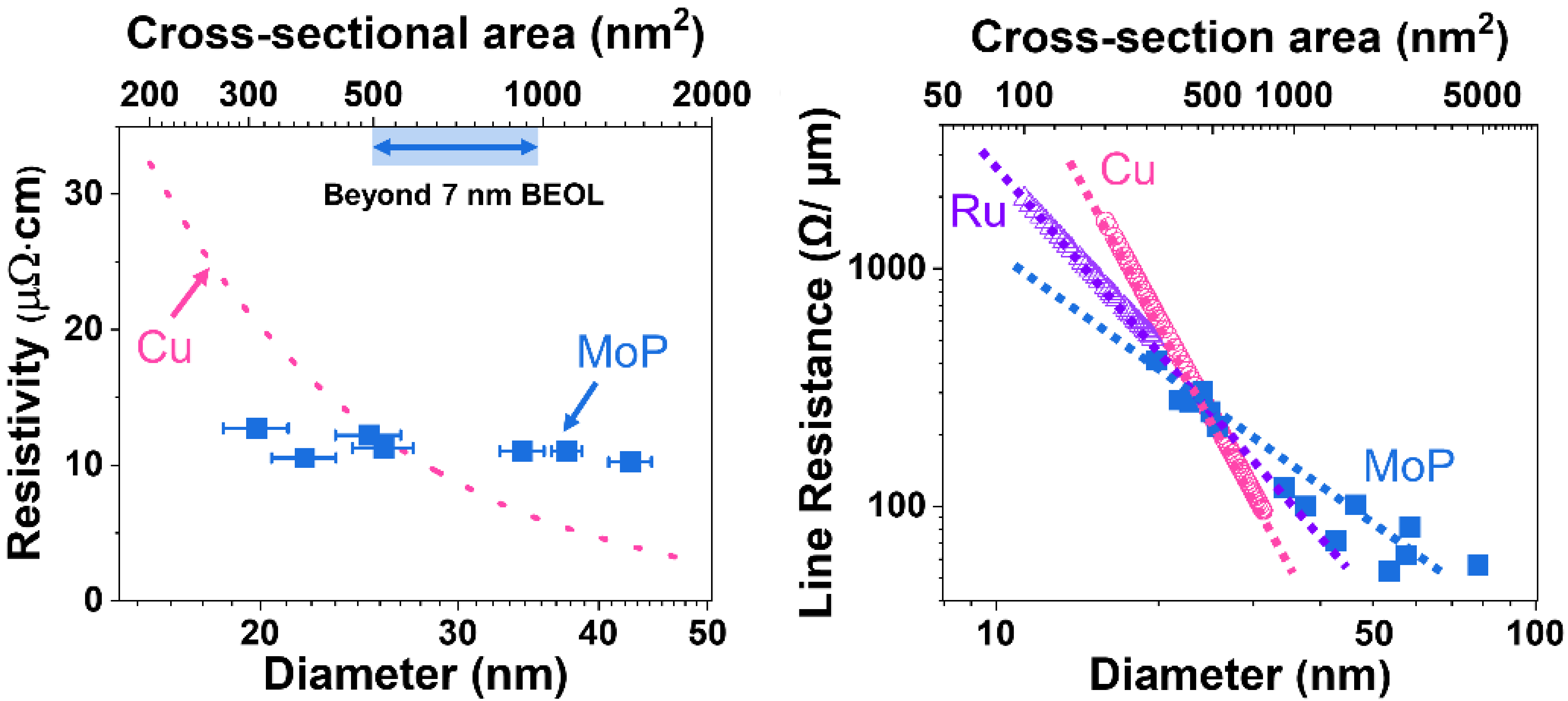
Task 2966.005

"Liner-free, non-oxide-based topological metals"





arXiv:2208.02784 (2022)



Cu and Ru data from IEEE IITC 2018, 172-174

Challenges

- How do we screen promising topological metals in a high throughput manner?
- How do we harness topological surface states at room temperature?
- BEOL-compatible processes for topological materials