Future Semiconductor Materials and Processes

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Challenges facing semiconductor technologies

- We’re moving to ‘ubiquitous computing’ and need significant computing power
- Number of elements used in chips has exploded from ~10 previously to ~60 now
- Fabrication requirements are increasingly complex
  - Need for conformality, uniformity, stability
  - Need to control edge placement error to reach yield
  - Interfaces dominate at nanometer scale devices

Idealized Atomic Layer Deposition (ALD)

- Vapor phase technique for deposition of thin films
- Sequential, self-limiting surface reactions
- Can deposit variety of materials (metals, metal oxides,…)
### Periodic Table of Materials Grown by ALD

![Periodic Table Image](image)

**Atomic number**

**Symbol**

The pure element has been grown

- **Compounds with Te**
- **Compounds with F**
- **Compounds with N**
- **Compounds with O**
- **Compounds with S**
- **Compounds with Se**
- **Compounds with other elements**

**Lanthanoids**

www.AtomicLimits.com, Erwin Kessels et al., Eindhoven University

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www.AtomicLimits.com - DOI: 10.6100/alldatabase
Advantages of ALD

**Thickness control**

W/Al₂O₃


**Film conformality**

Conformal Ge₂Sb₂Te₅ ALD film in trenches


**Composition control**

CdₓZn₁₋ₓS films

Conformality by ALD is exceptional

Cross-sectional HAADF-STEM images and corresponding EDS maps, showing a stack of alternating TiO$_2$ and SiO$_2$ layers and a single layer of Al$_2$O$_3$, all grown by plasma ALD on nanoscale trench structures.

Why Do We Need Selective Deposition?

First “Killer App” is in microelectronics
Integrated circuits have many layers of deposited films

3D rendering by ptychographic X-ray computed tomography (PXCT) with identified elements

Application specific integrated circuit (ASIC) with well-established 110 nm CMOS technology

Wafer Fabrication Process Steps

- Conventional wafer fabrication requires many steps across multiple tools
  - Top-down process

- **Incoming Wafer**
- **Deposition**
- **Lithography**
- **Etch**
- **Strip**
- **Clean**
- **Deposition**

**Steps Explained:**
- **Put down the insulating layers to be patterned**
- **Create the pattern mask**
- **Selectively remove material to create features**
- **Remove the photoresist mask**
- **Remove residues and particles**
- **Deposit conducting materials for the device**
Main Challenge: Edge Placement Error from Alignment in Lithography

- Edge placement error is limiting yield and cost in chips today
- Smaller nodes will have even smaller tolerances
  - Need nanometer and subnanometer precision

Challenge: Cost of Lithography

- Smaller features necessitate EUV
  - EUV scanner >$100 million
- Opportunities for cost-cutting with selective deposition
  - Reduce number of litho. steps

Challenge: Transfer of Pattern

- Often by reactive ion etching
  - Some materials difficult to etch

Bottom-up processing can help alleviate some challenges

Selective Deposition is a Bottom-Up Process

- Direct, additive deposition of materials only where desired
Example Application for Selective Deposition

Fully Aligned Via (BEOL)

**Challenge**

At tight pitches, mis-alignment causes via to metal shorts which result in high resistance and poor time dependent dielectric breakdown (TDDB) lifetime (defects often referred to as a fang or tiger tooth defect).

**Integration Solution: Fully Self Aligned Vias**

Solution: Selective deposition of etch hard mask

1. DD CMP Bottom metal
2. Selective Deposition: DoD
3. Blanket ULK Deposition
4. Via Etch
5. Line Trench Etch
6. DD Metal Fill

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Strategies to Achieve Area Selective ALD

- Inherent selectivity
- Area activation

- Area deactivation
  - Polymers, self-assembled monolayers (SAMs)
  - Small molecule inhibitors

AS-ALD with inhibitors must be DOUBLY SELECTIVE
Area Selective Atomic Layer Deposition (AS-ALD)

A bottom-up fabrication process

Patterned substrate → Inhibitor deposition → ALD → Selective deposition

Types of SAMs

<table>
<thead>
<tr>
<th>Type</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thiols</td>
<td>R-SH</td>
</tr>
<tr>
<td>Silanes</td>
<td>R-SiCl₃</td>
</tr>
<tr>
<td>Alkenes</td>
<td>R-C=C</td>
</tr>
<tr>
<td>Alkanoic acids</td>
<td>R-COOH</td>
</tr>
<tr>
<td>Phosphonic acids</td>
<td>R-PO₃H₃</td>
</tr>
</tbody>
</table>


Motivated by transistor high k gate stack (FEOL)

Initial work on FEOL gate stack funded by SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing (U of A)

Selective ALD via Self Assembled Monolayers

SEM image of representative structure

1-alkenes or 1-alkynes

Pt ALD

alkylsilanes

HfO₂ ALD

Pt elemental mapping

HfO₂ elemental mapping

SAM-Assisted AS-ALD on Metal/Dielectric Patterns

- ODPA SAM blocking process demonstrated on features <50 nm in size
- 15 cycles ZnO ALD
- EDX and TEM confirm no growth on Cu substrate

TEM EDS images of DoD deposition showing high selectivity to deposition on oxide, with SAM blocking dep on metal

Selectivity expression

$$S = \frac{R_{gs} - R_{ns}}{R_{gs} + R_{ns}}$$

$R$ : atomic comp. ratio or coverage
$gs$ = growth surface
$ns$ = non-growth surface

$S > 0.9999$
Area-selective ALD of silicon oxycarbide low-k dielectric

**ALD Process**

- GPC of 1.5 Å/cycle at 40°C
- Dielectric constant of 3.6–3.8

\[
\begin{align*}
\text{HO} & + \text{Cl}_3\text{SiC} & \text{ClSiCl}_3 & \rightarrow \text{ClSiCl}_3 & + \text{HCl} & \quad (1) \\
\text{O} & \text{SiCl}_3 & \text{H}_2 & + \text{H}_2\text{O} & \rightarrow \text{O} & \text{SiCl}_3 & \text{OH} & + \text{HCl} & \quad (2)
\end{align*}
\]

**Area Selectivity**

- Metals:
  - Al: ODPA SAM on surface Al\(_2\text{O}_3\)
  - Cu: DDT SAM

- Dielectric:
  - SiO\(_2\) (growth surface)
Selective DoD growth (SiO$_2$ versus Al or Cu)

Proof of concept for both the positive and negative pattern transfer of the low-k films onto Cu/Al patterns.

Can AS-ALD work for similar substrate materials?

Metal – Dielectric
“easy”

Dielectric – Dielectric
“hard”
Inhibitor Choices for Chemically Similar Materials

- Different kinetics of SAM formation
- Different reactivities of SAM headgroups

Octadecyltrichlorosilane (ODTS)

Octadecylsilane (ODS)

Octadecylphophonic acid (ODPA)
AS-ALD of ZnO on Patterns with Chemically Similar Materials

ODPA as inhibitor on metal oxides

ODPA with further process optimization

25 cycles ZnO ALD blocking test

Selective growth on SiO$_2$ not Al$_2$O$_3$

\[ S = 0.99 \]

Selective growth on SiO$_2$ not TiO$_2$

\[ S = 0.95 \]

Selective growth on SiO$_2$ not Ta$_2$O$_5$

\[ S = 0.95 \]

Selective growth on HfO$_2$ not Al$_2$O$_3$

\[ S = 0.98 \]

\[ S = \frac{\theta_{GS} - \theta_{NS}}{\theta_{GS} + \theta_{NS}} \]

Role of the ALD precursor

Precursor Factors Affecting Growth Characteristics

1) Reactivity
2) Polarity
3) Size
Model System for Precursor Design in Selective ALD: Al₂O₃

ALD Al₂O₃ with different Al precursors

- Al(CH₃)ₓCl₃₋ₓ case: different reactivity but similar monomeric sizes.
- Al(CₚH₂ₚ+₁)₃ case: different monomeric sizes but similar reactivity.

Growth Characteristics

DFT Calculations

Elucidating critical precursor properties for selective CVD (ALD and MOCVD)
Al₂O₃ ALD Selectivity Depends Strongly on Precursor Choice

Selectivity of Al₂O₃ between Growth (Si) and Non-growth Surfaces (ODTS/Si)

- Selectivity trend:
  - $\text{Al(CH}_3)_3 < \text{AlCl}_3 < \text{Al(CH}_3)_2\text{Cl} < \text{Al(C}_2\text{H}_5)_3$

- Why is Al(CH₃)₃ so poor?
  - Its smaller average size may lead to deep penetration into SAMs and difficulty blocking

<table>
<thead>
<tr>
<th>Effective average size ($V_{eff}$, Å³)</th>
<th>AlCl₃</th>
<th>Al(CH₃)₂Cl</th>
<th>Al(CH₃)₂Cl</th>
<th>Al(CH₃)₃</th>
<th>Al(C₂H₅)₃</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>143.7</td>
<td>147.6</td>
<td>151.6</td>
<td>87.2</td>
<td>140.2</td>
</tr>
</tbody>
</table>

Al(C₂H₅)₃ Precursor Provides Good Selective Al₂O₃ Deposition on Patterns

- 50 cycles Al₂O₃ with Al(C₂H₅)₃ on ODTST-treated Pt/SiO₂ patterns

Selectivity of 0.95 is obtained from the Auger Al line scan

Small Molecule Inhibitors (SMIs)

SiO$_2$ and Copper Pattern

Exposure to SMI

Exposure to ALD Process
AS-ALD Cycle with Small Molecule Inhibitor

AS-ALD of Ru and Pt

DMATMS (dimethylamino trimethylsilane)

DMADMS (dimethylamino dimethylsilane)

- Si ALD precursors used as inhibitors for AS-ALD
- They **selectively adsorb** on SiO\(_2\) surface but not on Si and **block ALD** Ru & Pt

Han-Bo-Ram Lee and coworkers, *Chem. Mater.*, 2018, 30 (21), pp 7603–7610
3-step AS-ALD Cycle with Small Molecule Inhibitor

- Process uses 3 alternating pulses in ABC sequence: acetylacetone inhibitor (step A), bis(diethylamino)silane precursor (step B), and O₂ plasma reactant (step C)

- SiO₂ AS-ALD process is selective to GeO₂, SiNₓ, SiO₂, and WO₃ over Al₂O₃, TiO₂ and HfO₂ surfaces

- 15 cycle (1 nm) growth delay observed on Al₂O₃

Mackus et al., ACS Nano 2017, 11, 9303–9311
Organosilane Small Molecule Inhibitors (SMIs)

- Ambient vapor-phase delivery
- Study effects of silane molecular structure

- Reactive headgroups matter
- Tail length does not

Trimethoxypropylsilane (TMPS)
Selective $\text{Al}_2\text{O}_3$ ALD Depends on Al Precursor

- Process temperature: 150 °C

- Using triethylaluminum (TEA) vs. trimethylaluminum (TMA) allows for more selective growth

\[ S = \frac{R_{gs} - R_{ns}}{R_{gs} + R_{ns}} \]

TMPS SMI blocks at least 4 nm ALD on SiO₂, while allowing growth on Cu.

TEA-based ALD performed at 150°C
Complexities of ALD

What we imagine...
Non-Idealities Lurk Everywhere in ALD

Metal ALD on Low Surface-Energy Substrates

Pt ALD on SiO$_2$

- Thick films upon coalescence
- Pinholes
- Rough films
- Polydisperse grain size

Pt Nucleation Enhancement with Small Molecule Surface Activation

Surface treatment prior to ALD incorporates less than a single monolayer of impurities

Small molecules:
- ZnEt₂
- AlMe₃
- AlMe₂Cl

+ O₂ @ 300 °C, Substrate = SiO₂

HVM Requirements for ALD

- Conformality (step coverage)
- Controllable film thickness at angstrom level
- Film continuity / uniformity / pinhole-free
  - Continuity at few nanometer scale film thickness
  - Film roughness
- Compositional control
  - Homogeneity in ternary—or greater—materials
- Reproducibility
- Selectivity (for some applications)
- Process tolerance
  - Temperature, flow, pressure
- Cost and throughput

HVM = high volume manufacturing
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