Future Semiconductor Materials and Processes

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SRC-SIA Webinar on Collaboration Towards Decadal Plan Goals:
Emerging Semiconductor Technologies
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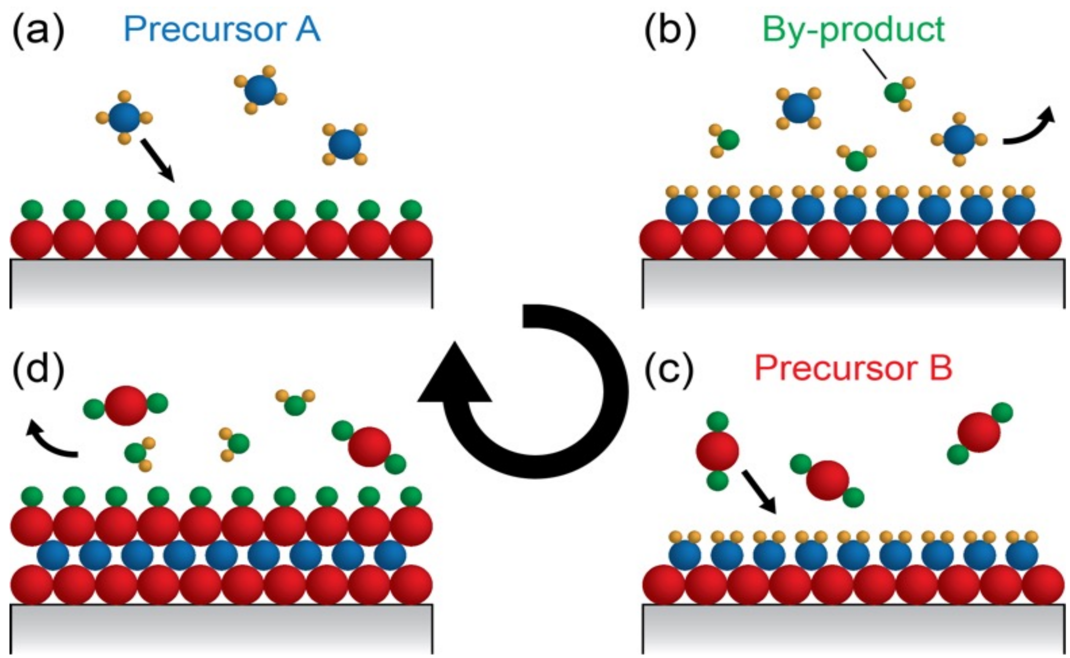
Challenges facing semiconductor technologies

- We're moving to 'ubiquitous computing' and need significant computing power
- Number of elements used in chips has exploded from ~10 previously to ~60 now
- Fabrication requirements are increasingly complex
  - Need for conformality, uniformity, stability
  - Need to control edge placement error to reach yield
  - Interfaces dominate at nanometer scale devices

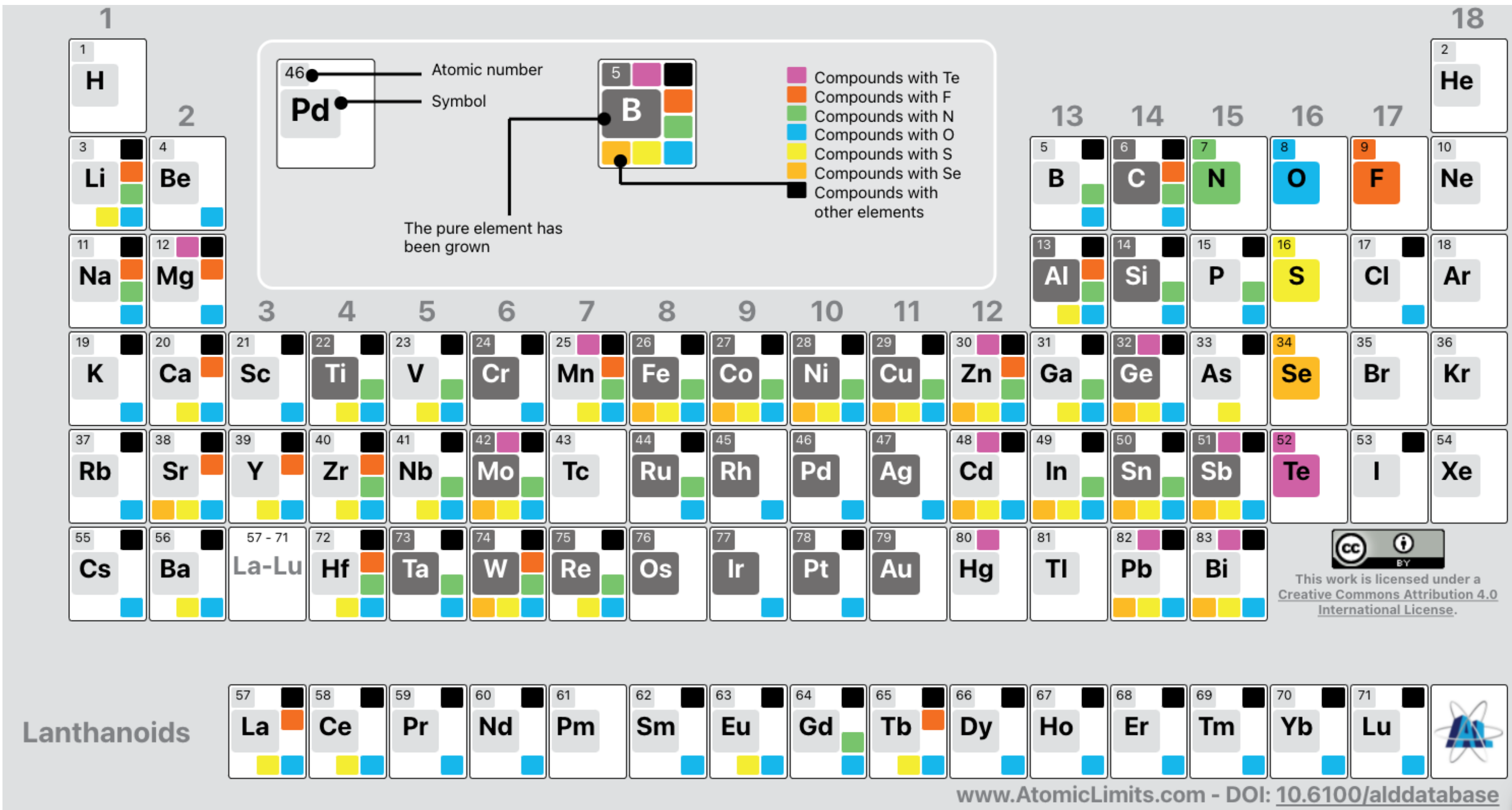
"New process requirements driven by More than Moore and More Moore Device Integration Innovations," P. Leray and S. Steen, ALD/ALE 2022 Conference Presentation

Idealized Atomic Layer Deposition (ALD)

- Vapor phase technique for deposition of thin films
- Sequential, self-limiting surface reactions
- Can deposit variety of materials (metals, metal oxides,…)



Periodic Table of Materials Grown by ALD

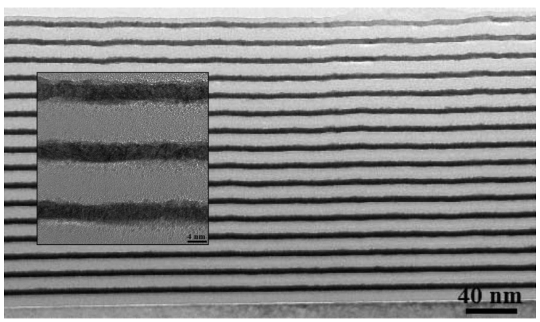


www.AtomicLimits.com, Erwin Kessels et al., Eindhoven University

Advantages of ALD

Thickness control

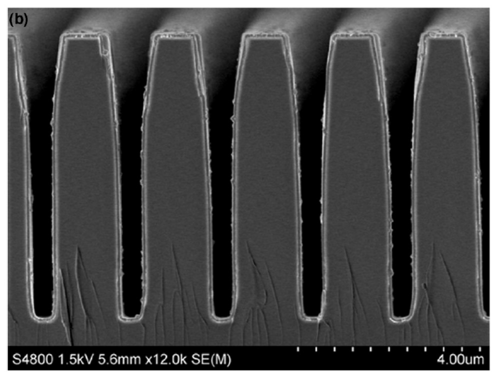
W/Al_2O_3



Fabreguette, F. H.; Wind, R. A.; George, S. M. Appl. Phys. Lett., 2006, 88, 013116.

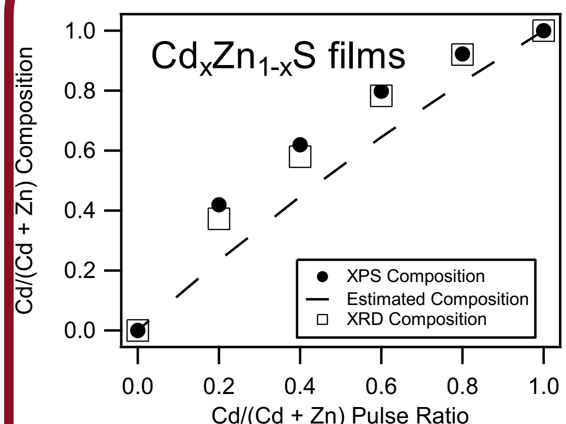
Film conformality

Conformal $Ge_2Sb_2Te_5$ ALD film in trenches



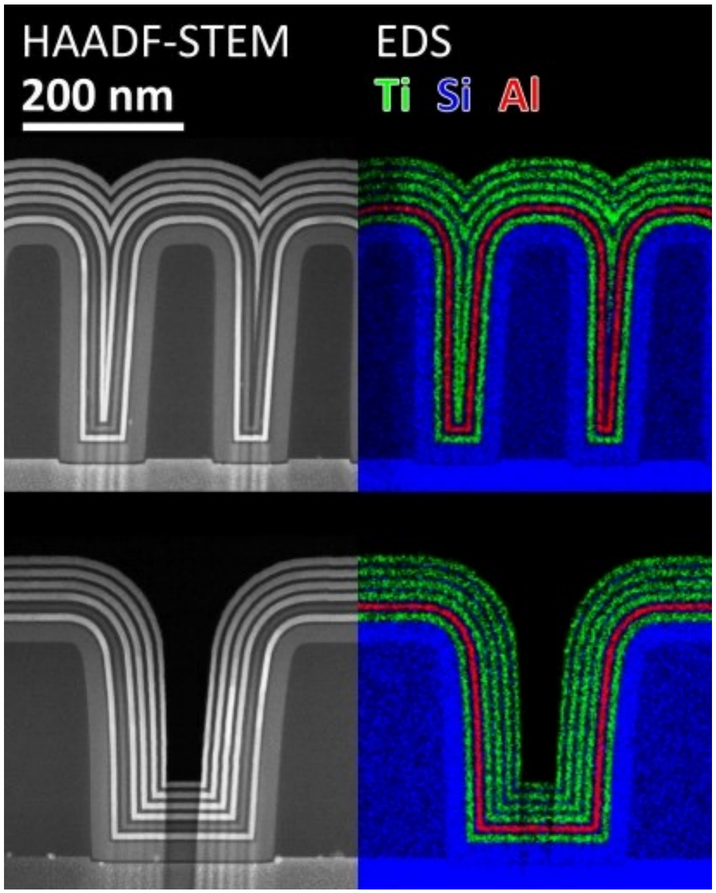
V. Pore, et al. J. Am. Chem. Soc. 131 (10) (2009) 3478–3480

Composition control



Bakke, Tanskanen, Jung, Sinclair and Bent, J. Mater. Chem., 2011, 21, 743–751

Conformality by ALD is exceptional



Cross-sectional HAADF-STEM images and corresponding EDS maps, showing a stack of alternating TiO_2 and SiO_2 layers and a single layer of Al_2O_3, all grown by plasma ALD on nanoscale trench structures.

Courtesy of K. Arts, M.A. Verheijen, W.M.M. Kessels and H.C.M Knoops (CC BY 4.0 license), image library at www.AtomicLimits.com, 2021.

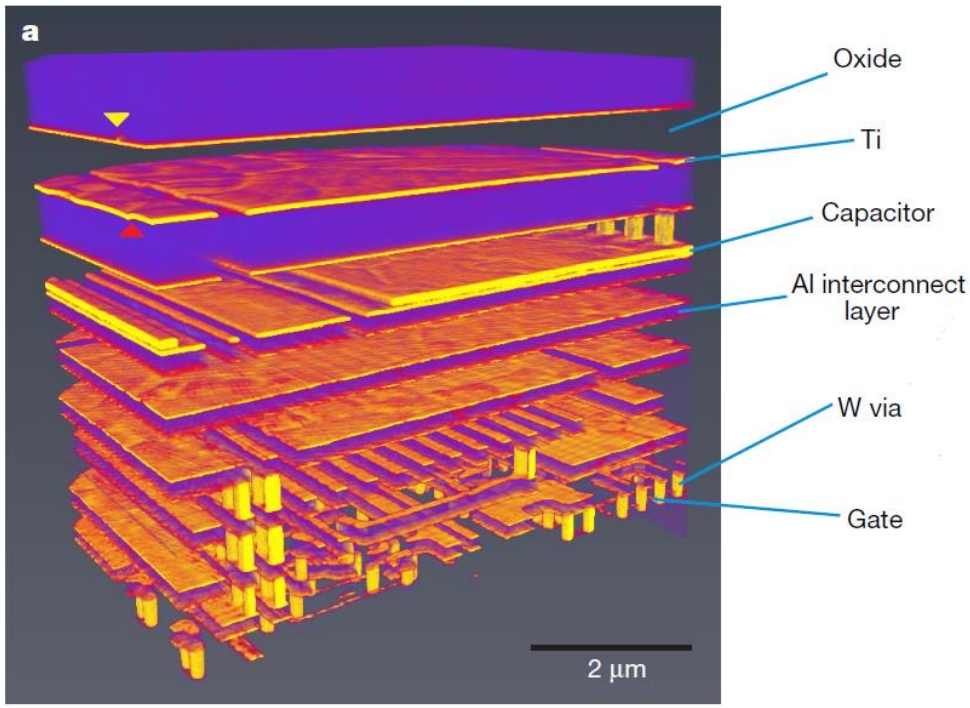
Why Do We Need Selective Deposition?

First "Killer App" is in microelectronics

Integrated circuits have many layers of deposited films

3D rendering by ptychographic X-ray computed tomography (PXCT) with identified elements

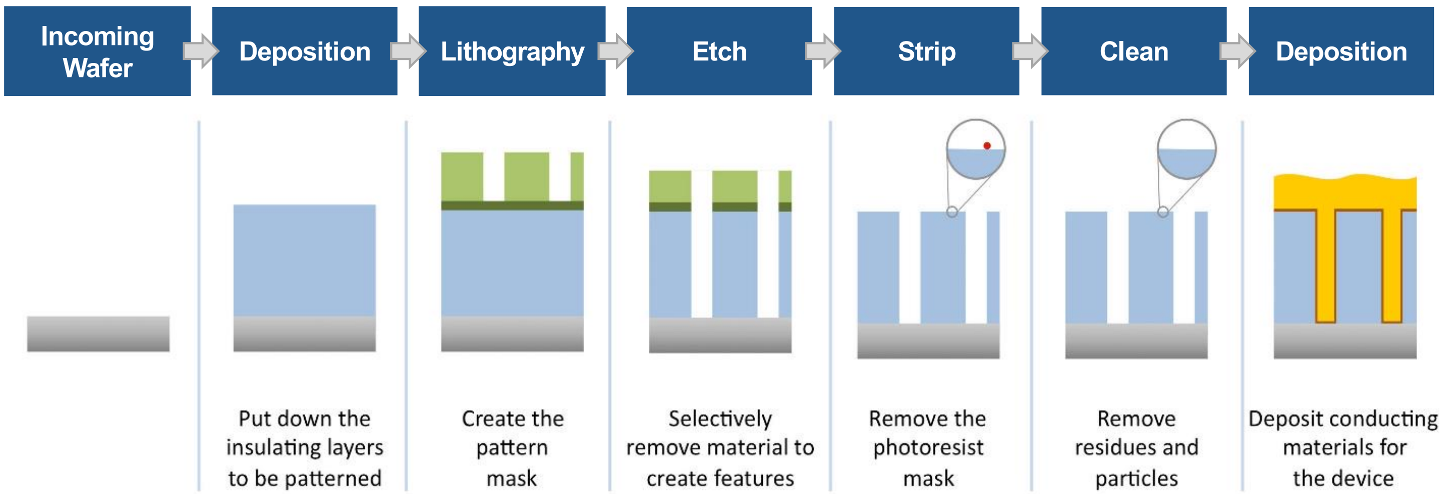
Application specific integrated circuit (ASIC) with well-established 110 nm CMOS technology



Holler, M., Guizar-Sicairos, M., Tsai, E. *et al.* High-resolution non-destructive three-dimensional imaging of integrated circuits. *Nature* **543,** 402–406 (2017)

Wafer Fabrication Process Steps

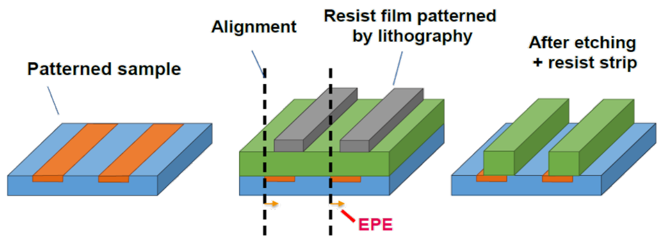
- Conventional wafer fabrication requires many steps across multiple tools
  - Top-down process



Top Down Processing is Causing Challenges to Future Scaling

Main Challenge: Edge Placement Error from Alignment in Lithography

- **Edge placement error is limiting yield and cost in chips today**
- **Smaller nodes will have even smaller tolerances**
  - Need nanometer and subnanometer precision



Mameli et. al., ASD workshop, 2017

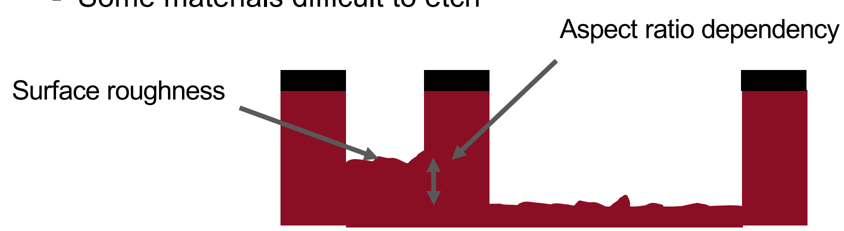
Challenge: Cost of Lithography

- Smaller features necessitate EUV
  - EUV scanner >$100 million
- Opportunities for cost-cutting with selective deposition
  - Reduce number of litho. steps

https://electroiq.com/2018/07/the-devilish-details-of-euv-lithography/

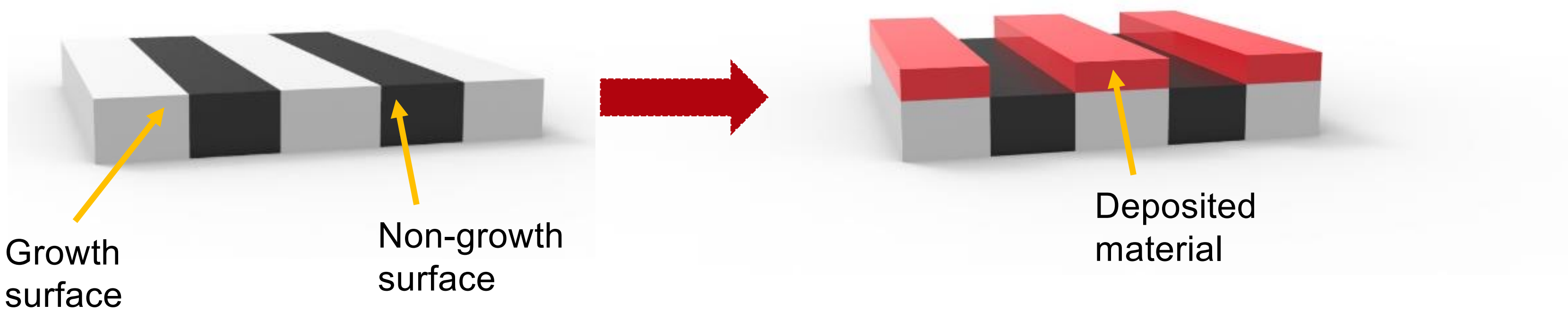
Challenge: Transfer of Pattern

- **Often by reactive ion etching**
  - Some materials difficult to etch



Bottom-up processing can help alleviate some challenges

Selective Deposition is a Bottom-Up Process



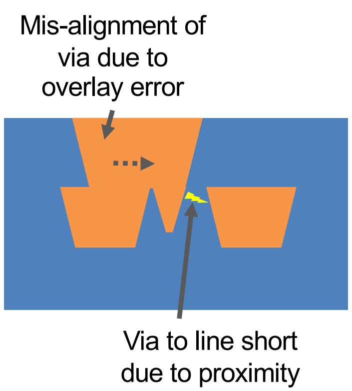
- Direct, additive deposition of materials only where desired

Example Application for Selective Deposition

Fully Aligned Via (BEOL)

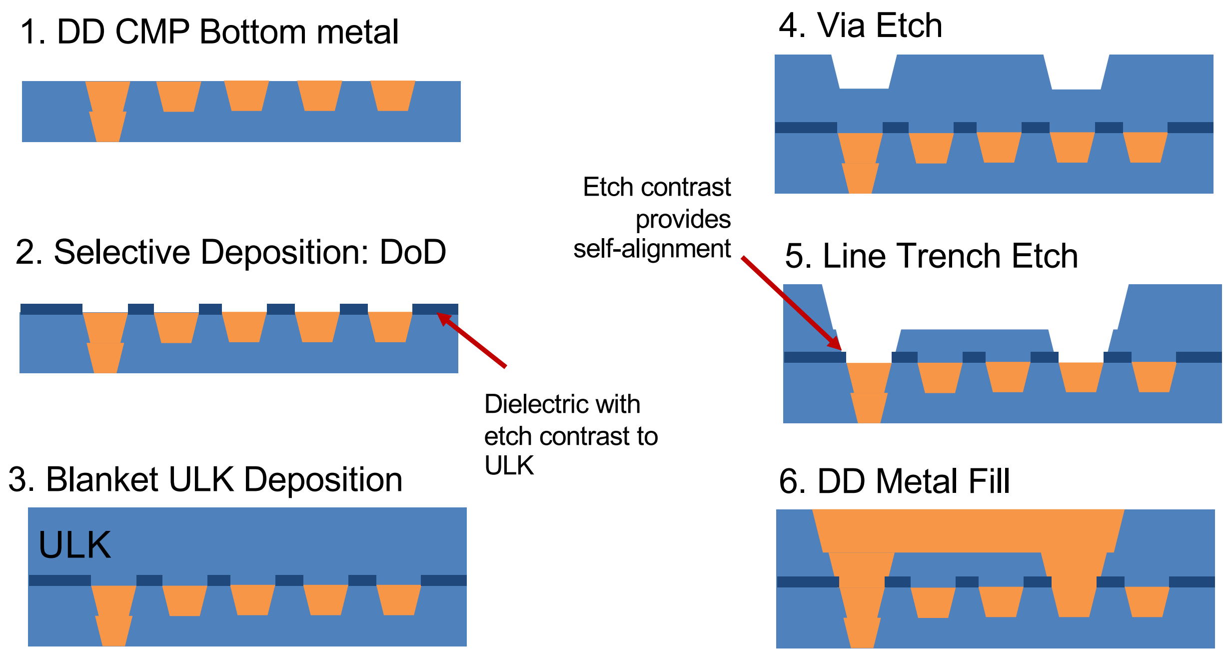
Challenge

At tight pitches, mis-alignment causes via to metal shorts which result in high resistance and poor time dependent dielectric breakdown (TDDB) lifetime (defects often referred to as a fang or tiger tooth defect)



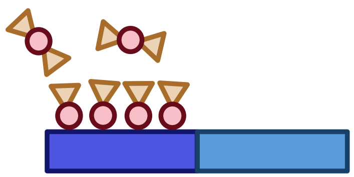
Integration Solution: Fully Self Aligned Vias

Solution: Selective deposition of etch hard mask

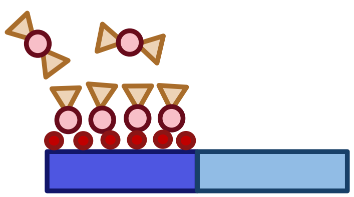


Strategies to Achieve Area Selective ALD

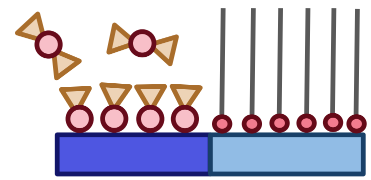
- Inherent selectivity



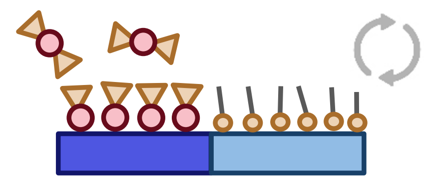
- Area activation



- Area deactivation
  - Polymers, self-assembled monolayers (SAMs)



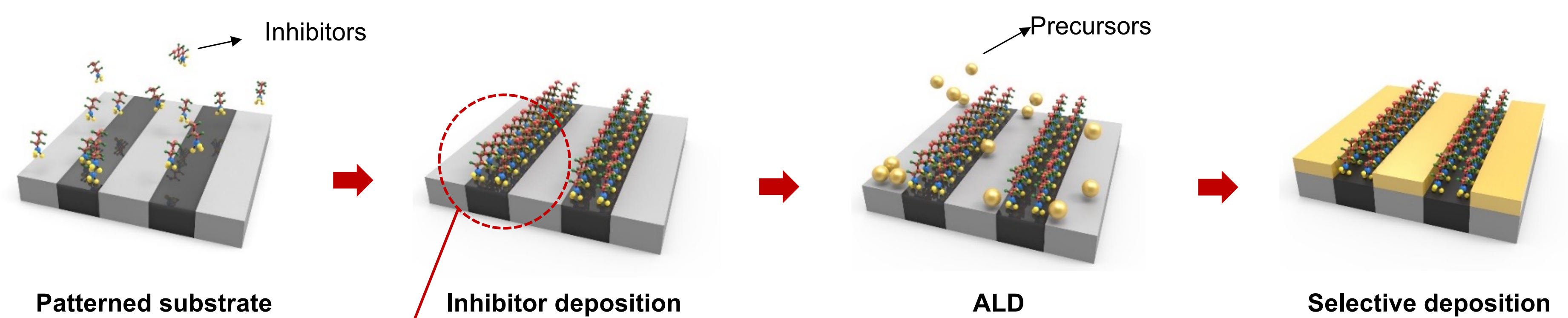
  - Small molecule inhibitors

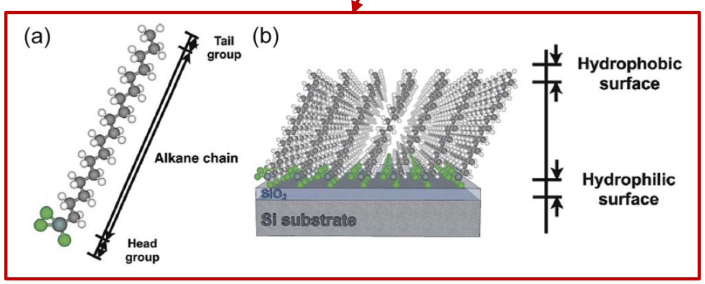


AS-ALD with inhibitors must be DOUBLY SELECTIVE

Area Selective Atomic Layer Deposition (AS-ALD)

A bottom-up fabrication process

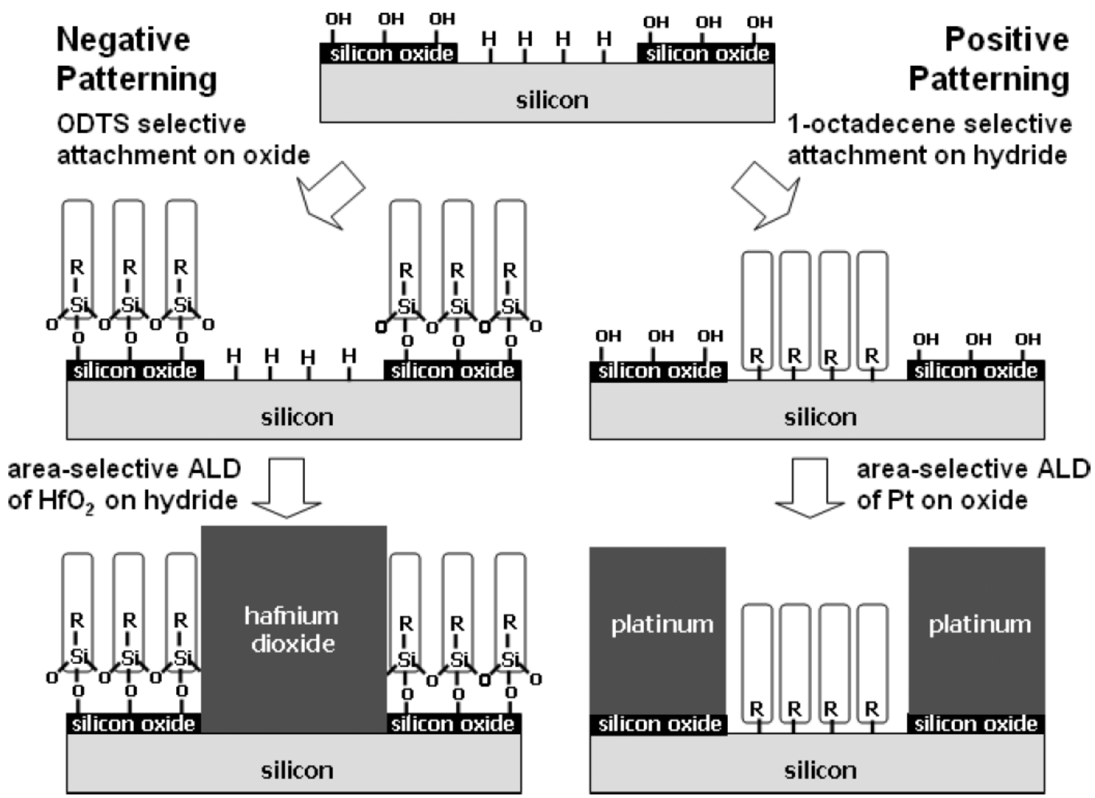




H.-B.-R. Lee and S. F. Bent, in Nanostructures by ALD, Ed. Mato Knez and Nicola Pinna (Wiley-VCH, 2012).

Types of SAMs	
Thiols	R-SH
Silanes	R-$SiCl_3$
Alkenes	R-C=C
Alkanoic acids	R-COOH
Phosphonic acids	R-PO_3H_3

Prototypical Area Selective ALD Process (2006)



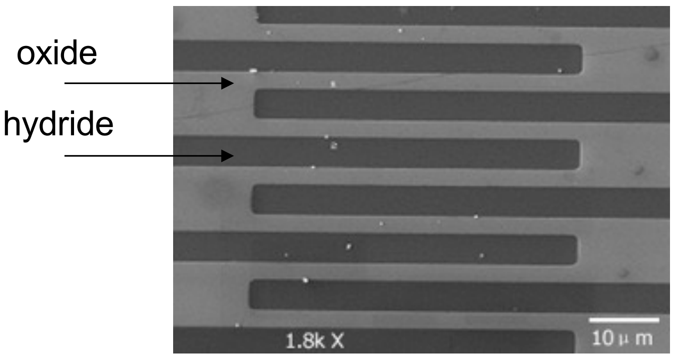
Chen and S. F. Bent, Adv. Mat., 18 (2006) 1086-1090

Motivated by transistor high k gate stack (FEOL)

Initial work on FEOL gate stack funded by SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing (U of A)

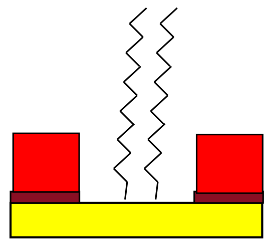
Selective ALD via Self Assembled Monolayers

SEM image of representative structure



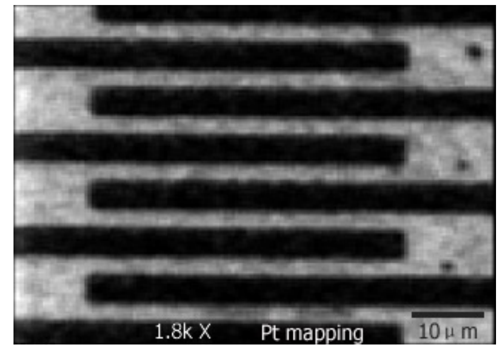
1-alkenes or 1-alkynes

+



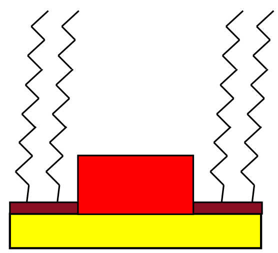
Pt ALD

Pt elemental mapping



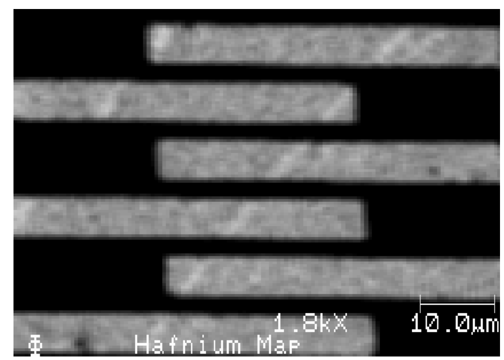
alkylsilanes

+



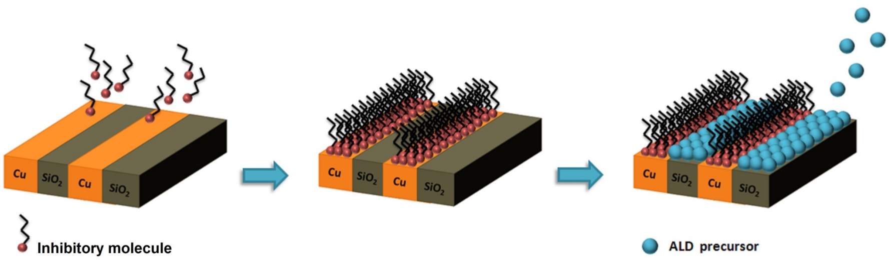
HfO_2 ALD

HfO_2 elemental mapping

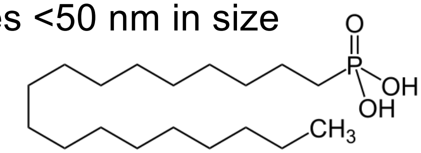


R. Chen and S. F. Bent, Adv. Mat., 18 (2006) 1086-1090

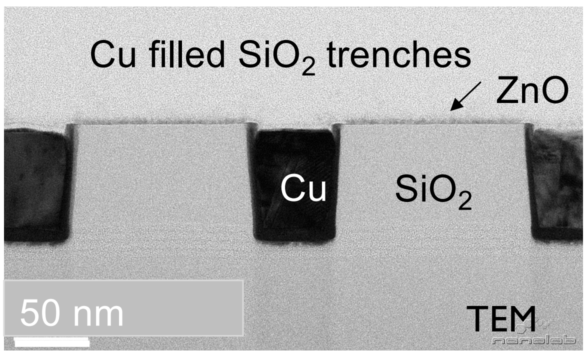
SAM-Assisted AS-ALD on Metal/Dielectric Patterns

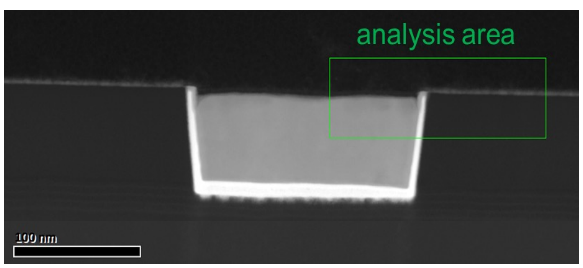


- ODPA SAM blocking process demonstrated on features <50 nm in size

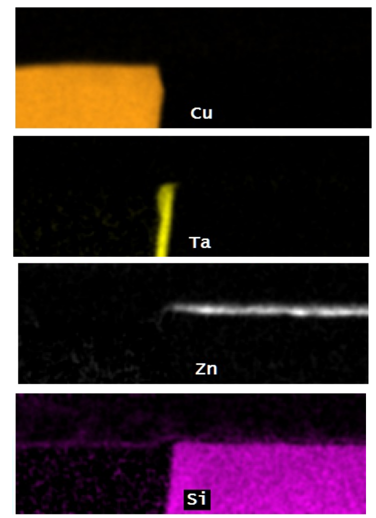


- 15 cycles ZnO ALD
- EDX and TEM confirm no growth on Cu substrate



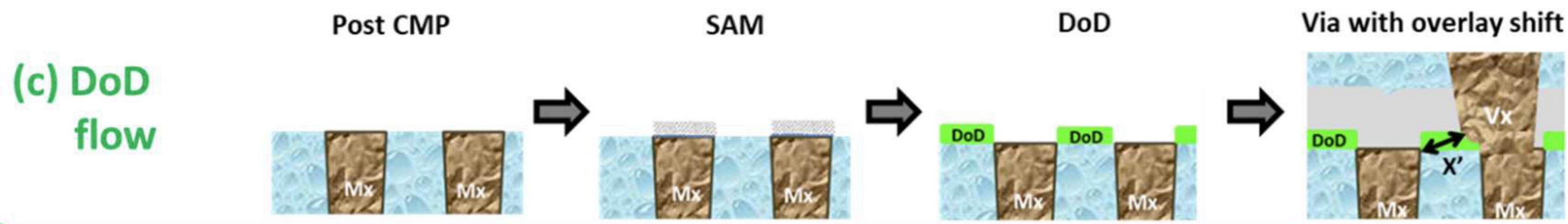


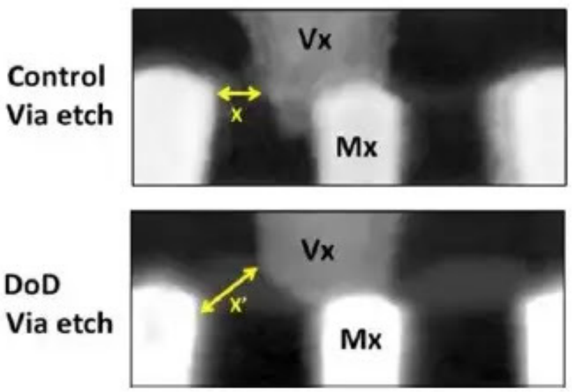
EELS/EDX Elemental Analysis



D. Bobb-Semple, K. L Nardi, N. Draeger, D. M. Hausmann and S. F. Bent, Chem. Mat 31 (2019) 1635-1645.

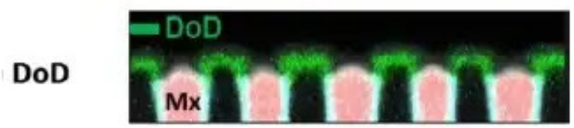
TSMC presentation at Jan 2022 IEDM meeting





TEM images of via-to-adjacent metal, with and without DoD deposition

TEM EDS images of DoD deposition showing high selectivity to deposition on oxide, with SAM blocking dep on metal



Selectivity expression

$$S = \frac{R_{gs} - R_{ns}}{R_{gs} + R_{ns}}$$

R : atomic comp. ratio or coverage
gs = growth surface
ns = non-growth surface

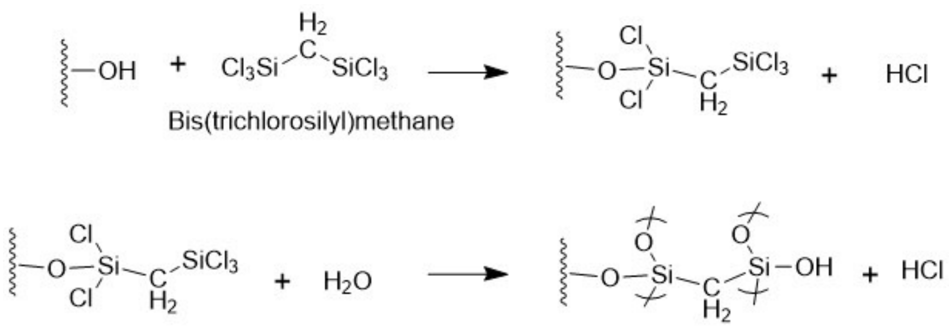
S > 0.9999

"Fully Self-Aligned Via Integration for Interconnect Scaling Beyond 3nm Node," H.P. Chen et al., IEDM21-486-489.

Area-selective ALD of silicon oxycarbide low-k dielectric

ALD Process

- GPC of 1.5 Å/cycle at 40^{o}C
- Dielectric constant of 3.6−3.8



(1)

(2)

Area Selectivity

Metal/SiO_2 pattern

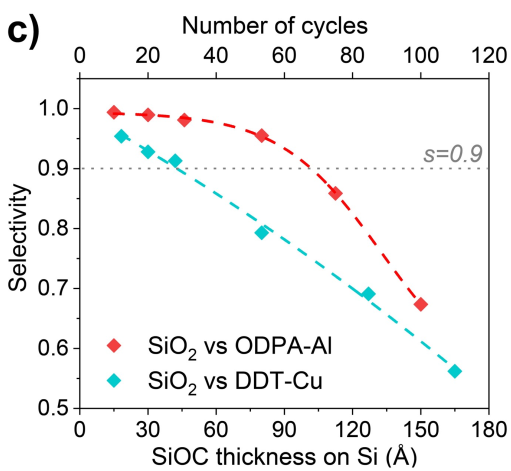
Metals:

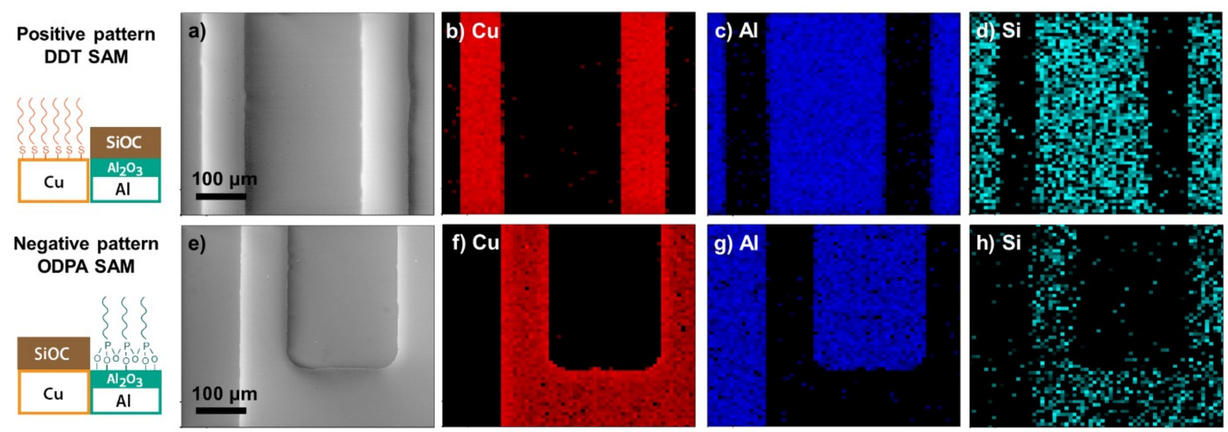
- Al: ODPA SAM on surface Al_2O_3
- Cu: DDT SAM

Dielectric:

- SiO_2 (growth surface)

Selective DOD of silicon oxycarbide low-k dielectric

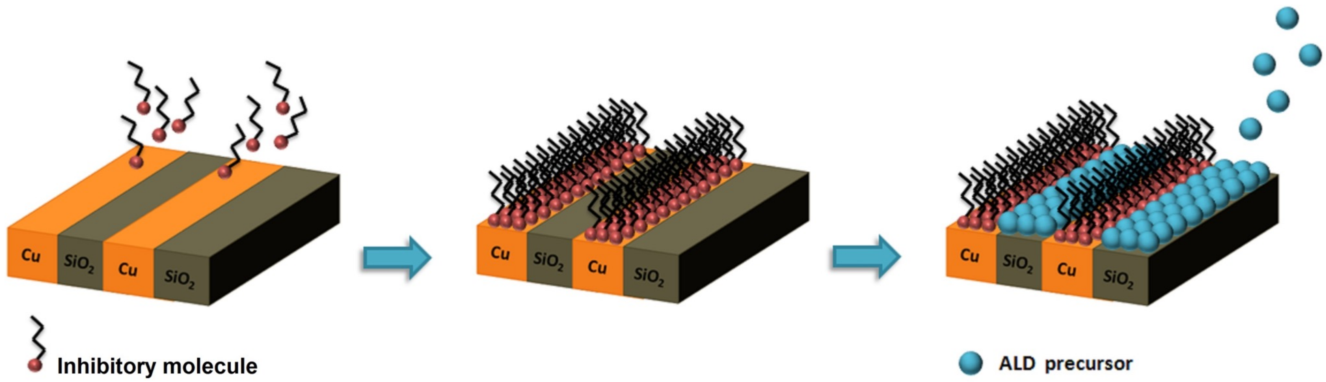




- Selective DoD growth (SiO_2 versus Al or Cu)
- Proof of concept for both the positive and negative pattern transfer of the low-k films onto Cu/Al patterns.

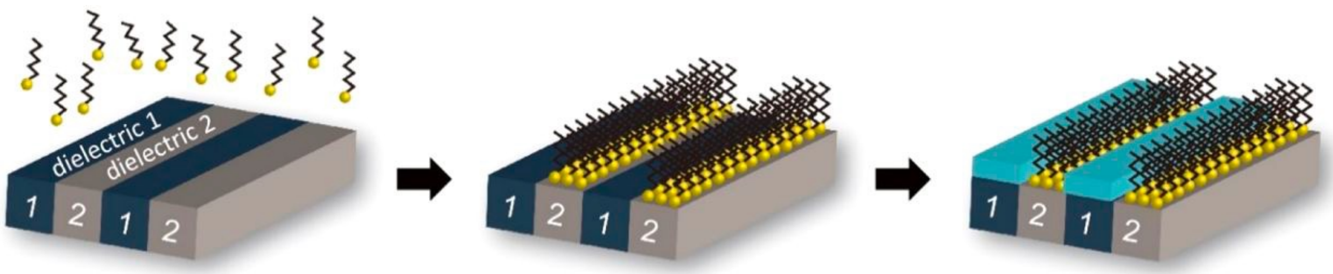
X. Yu, D. Bobb-Semple, I.-K. Oh, T.-L. Liu, R. Closser, W. Trevillyan and S. F. Bent, *Chem. Mat.*, **33** (2021) 902–909

Can AS-ALD work for similar substrate materials?



Metal – Dielectric

"easy"



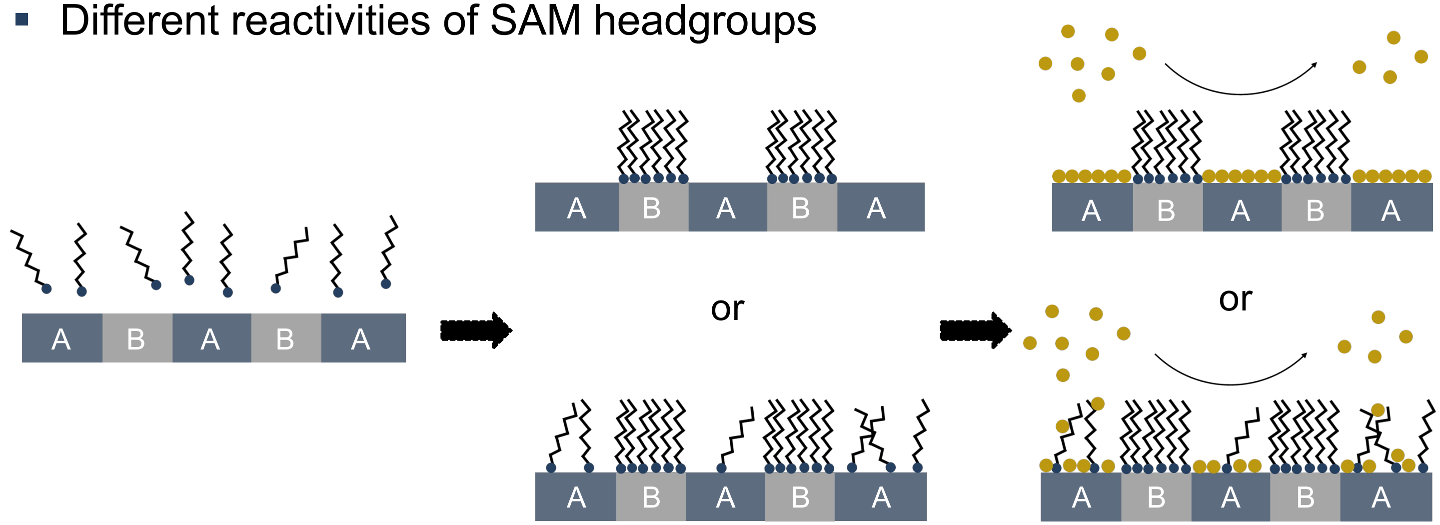
Dielectric – Dielectric

"hard"

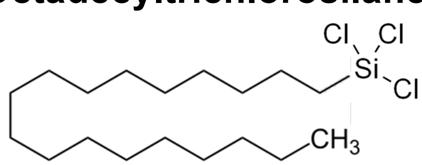
Research under SRC nCORE

Inhibitor Choices for Chemically Similar Materials

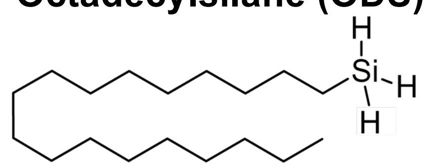
- Different kinetics of SAM formation
- Different reactivities of SAM headgroups



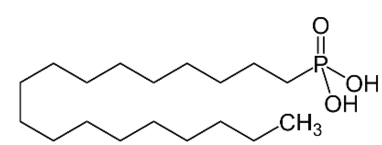
Octadecyltrichlorosilane (ODTS)



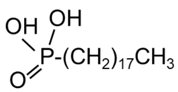
Octadecylsilane (ODS)



Octadecylphophonic acid (ODPA)

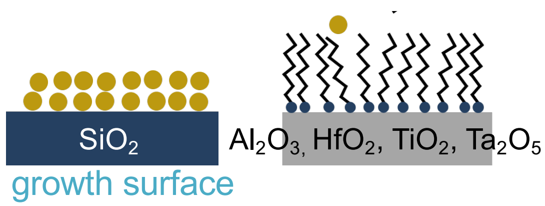


AS-ALD of ZnO on Patterns with Chemically Similar Materials

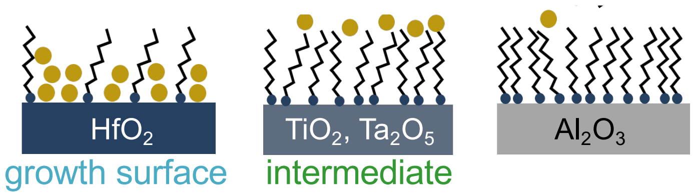


25 cycles ZnO ALD blocking test

ODPA as inhibitor on metal oxides



ODPA with further process optimization



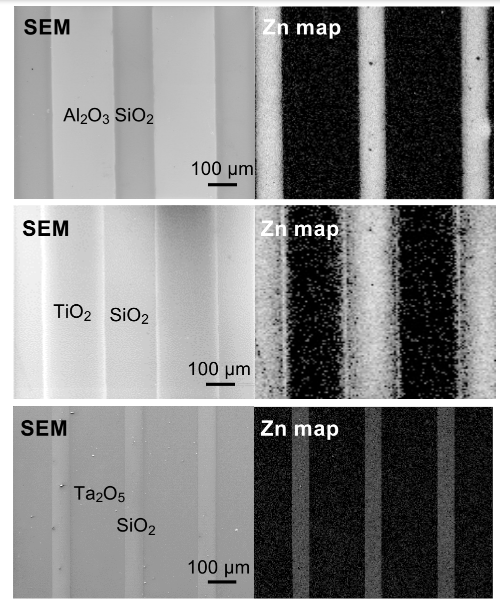
$$S = \frac{\theta_{GS} - \theta_{NS}}{\theta_{GS} + \theta_{NS}}$$

SiO_2/MO_x systems

Selective growth on SiO_2 not Al_2O_3
S = 0.99

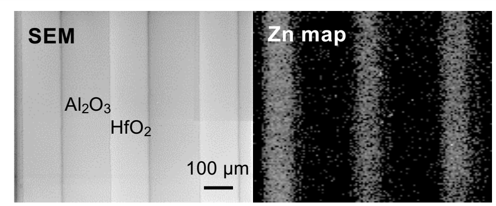
Selective growth on SiO_2 not TiO_2
S = 0.95

Selective growth on SiO_2 not Ta_2O_5
S = 0.95



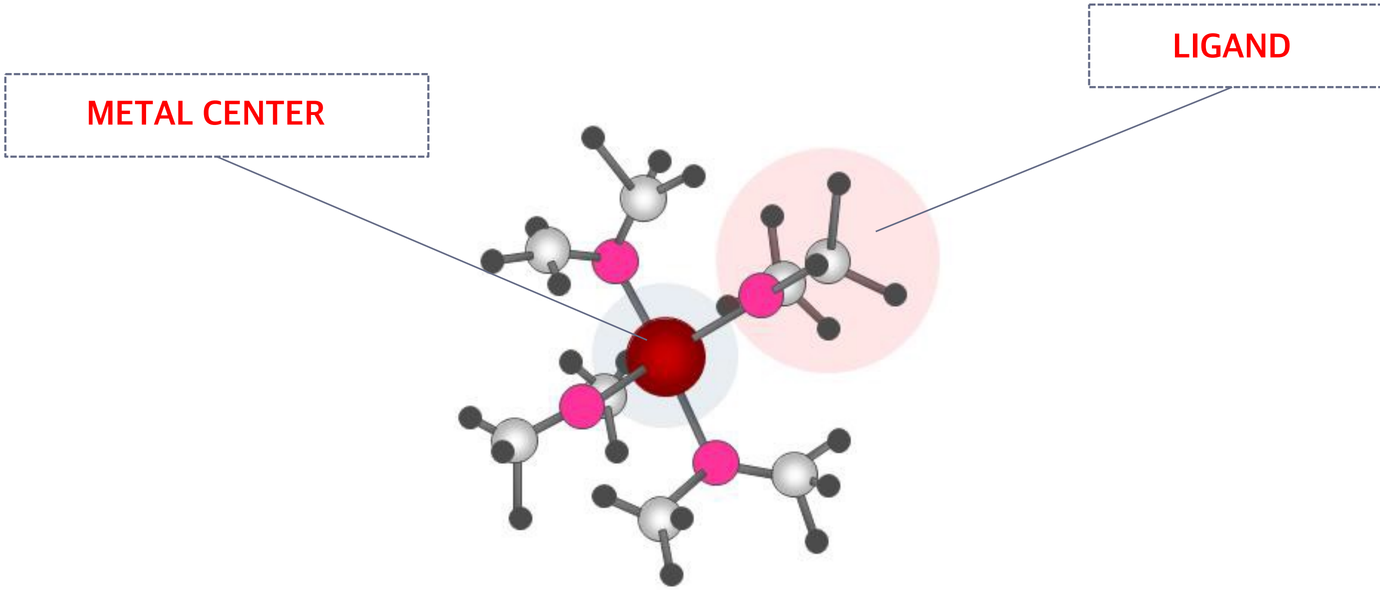
MO_x/MO_y systems

Selective growth on HfO_2 not Al_2O_3
S = 0.98



T.-L. Liu, S. F. Bent. Chem. Mater. 2021, 33, 513−523

Role of the ALD precursor

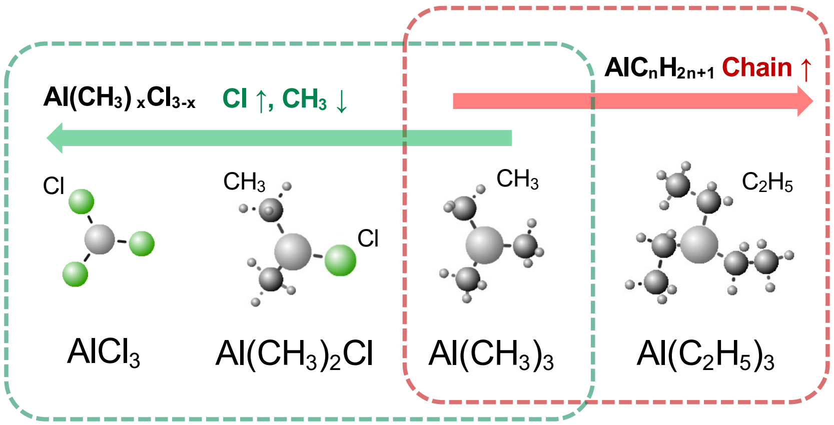


Precursor Factors Affecting Growth Characteristics

1) Reactivity **2) Polarity** **3) Size**

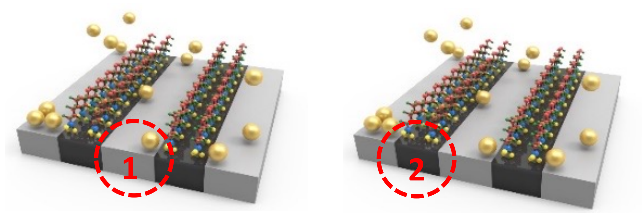
Model System for Precursor Design in Selective ALD: Al_2O_3

ALD Al_2O_3 with different Al precursors



- $Al(CH_3)_xCl_{3-x}$ case: different reactivity but similar monomeric sizes.
- $Al(C_yH_{2y+1})_3$ case: different monomeric sizes but similar reactivity.

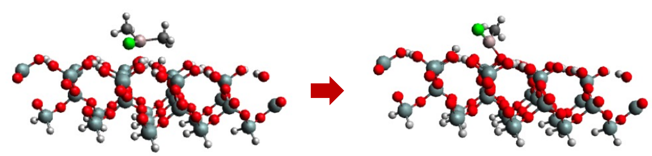
Growth Characteristics



Growth surface

Non-growth surface

DFT Calculations

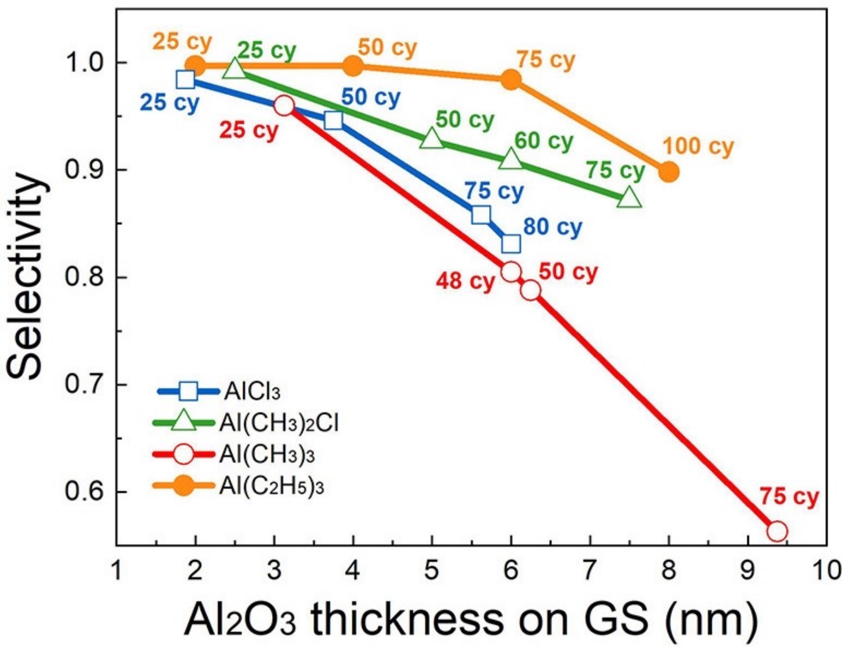


Collaboration with Prof. Tania Sandoval and Prof. Ralf Tonner

Elucidating critical precursor properties for selective CVD (ALD and MOCVD)

Al_2O_3 ALD Selectivity Depends Strongly on Precursor Choice

Selectivity of Al_2O_3 between Growth (Si) and Non-growth Surfaces (ODTS/Si)



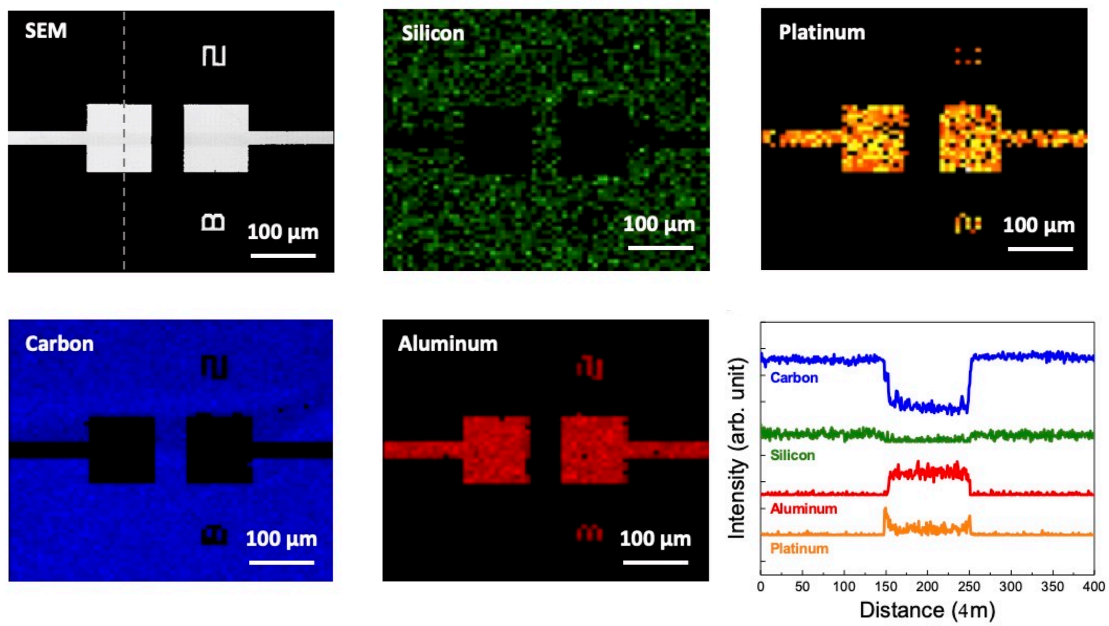
- Selectivity trend:
  - $Al(CH_3)_3 < AlCl_3 < Al(CH_3)_2Cl < Al(C_2H_5)_3$
- Why is $Al(CH_3)_3$ so poor?
  - Its smaller average size may lead to deep penetration into SAMs and difficulty blocking

	$AlCl_3$	$Al(CH_3)_2Cl$	$Al(CH_3)_2Cl$	$Al(CH_3)_3$	$Al(C_2H_5)_3$
Effective average size (V_{eff}; $Å^3$)	143.7	147.6	151.6	87.2	140.2

I.-K. Oh, T. E. Sandoval, T.-L. Liu, N. E. Richey, and S. F. Bent, Chem. Mat., 33 (2021) 3926–3935

$Al(C_2H_5)_3$ Precursor Provides Good Selective Al_2O_3 Deposition on Patterns

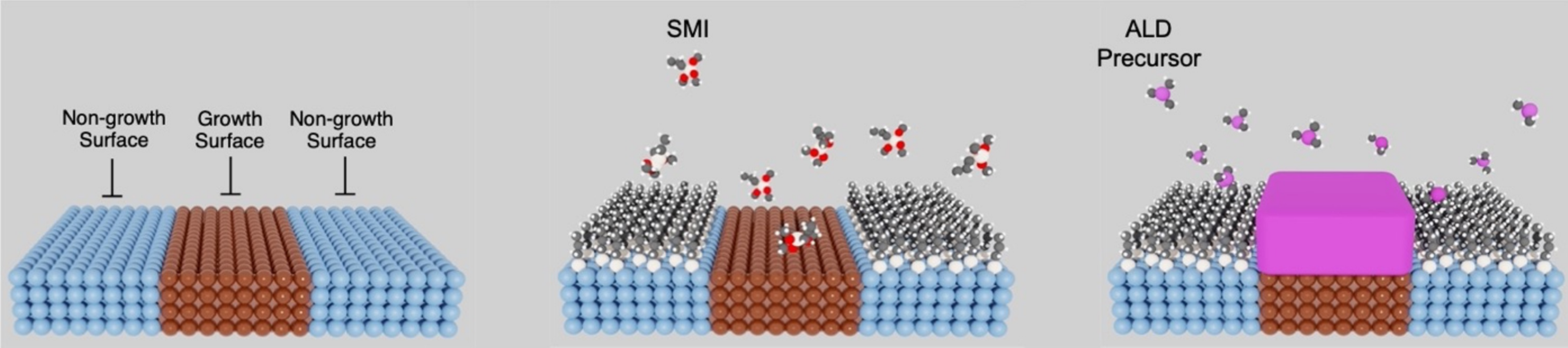
- 50 cycles Al_2O_3 with $Al(C_2H_5)_3$ on ODTS-treated Pt/SiO_2 patterns



- Selectivity of 0.95 is obtained from the Auger Al line scan

I.-K. Oh, T. E. Sandoval, T.-L. Liu, N. E. Richey, and S. F. Bent, Chem. Mat., 33 (2021) 3926–3935

Small Molecule Inhibitors (SMIs)



SiO_2 and Copper Pattern

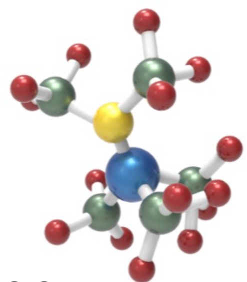
Exposure to SMI

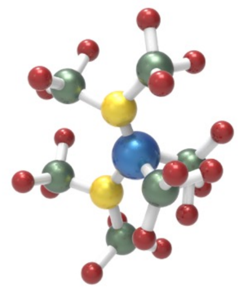
Exposure to ALD Process

AS-ALD Cycle with Small Molecule Inhibitor

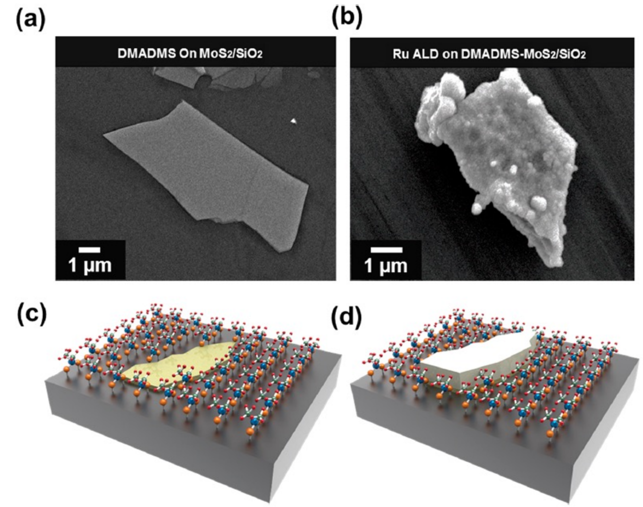
AS-ALD of Ru and Pt

DMATMS
(dimethylamino
trimethylsilane)

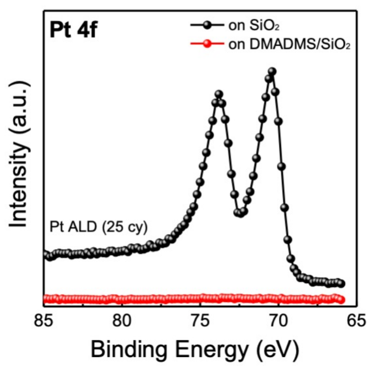


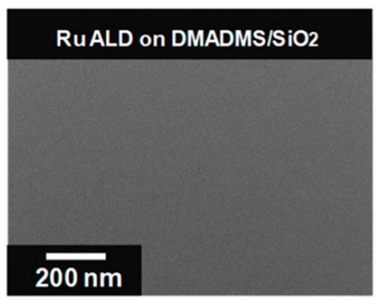


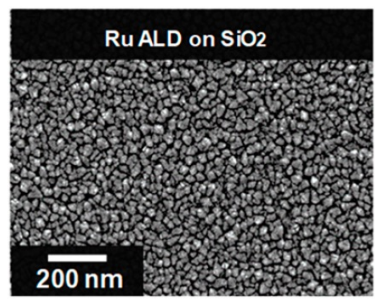
DMADMS
(dimethylamino
dimethylsilane)



Blocking ALD Pt on SiO_2





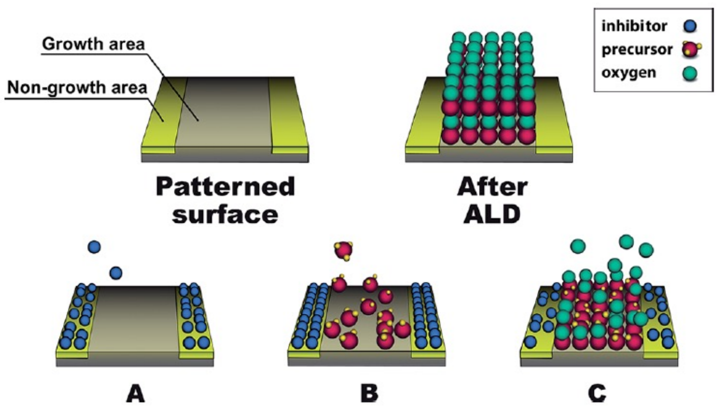


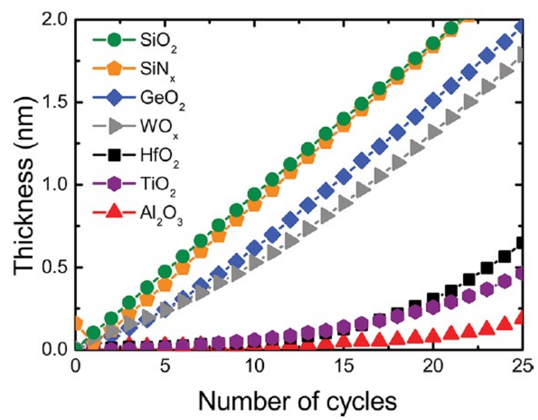
- Si ALD precursors used as inhibitors for AS-ALD
- They **selectively adsorb** on SiO_2 surface but not on Si and **block ALD** Ru & Pt

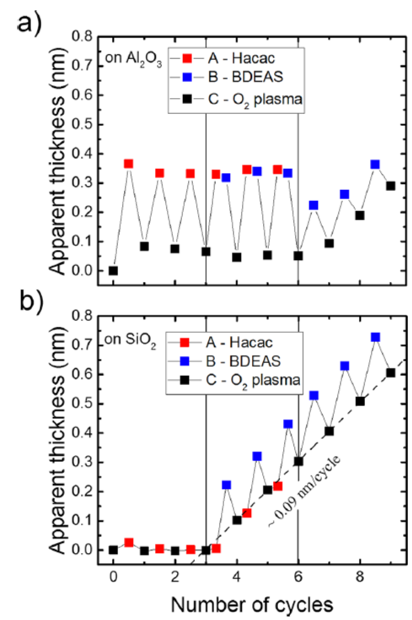
Han-Bo-Ram Lee and coworkers, *Chem. Mater.*, **2018**, *30* (21), pp 7603–7610

3-step AS-ALD Cycle with Small Molecule Inhibitor

- Process uses 3 alternating pulses in ABC sequence: acetylacetone inhibitor (step A), bis(diethylamino)silane precursor (step B), and O_2 plasma reactant (step C)
- SiO_2 AS-ALD process is selective to GeO_2, SiN_x, SiO_2, and WO_3 over Al_2O_3, TiO_2 and HfO_2 surfaces
- 15 cycle (1 nm) growth delay observed on Al_2O_3



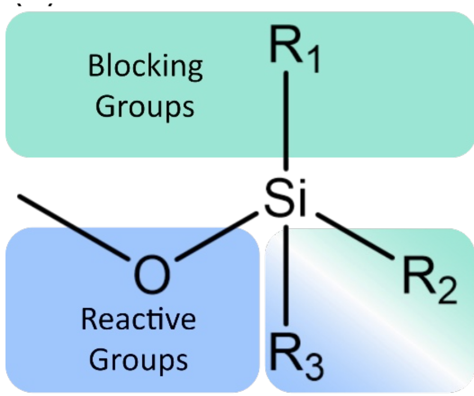




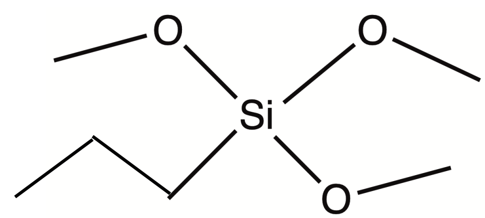
Mackus et al., ACS Nano 2017, 11, 9303−9311

Organosilane Small Molecule Inhibitors (SMIs)

- Ambient vapor-phase delivery
- Study effects of silane molecular structure



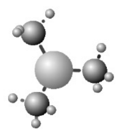
- Reactive headgroups matter
- Tail length does not

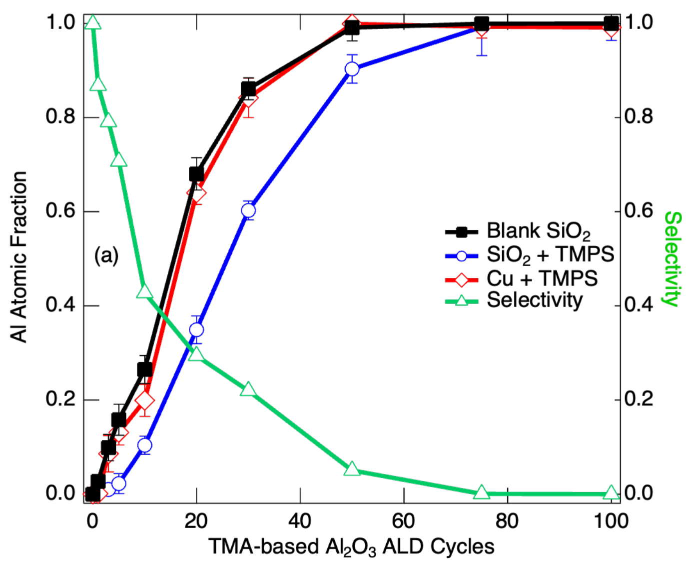


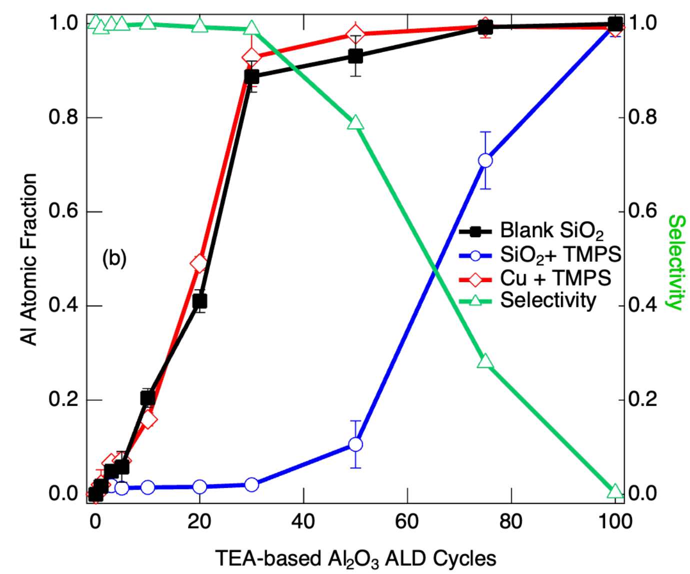
Trimethoxypropylsilane
(TMPS)

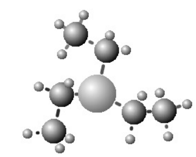
Selective Al_2O_3 ALD Depends on Al Precursor

TMA + Water | **TEA + Water**









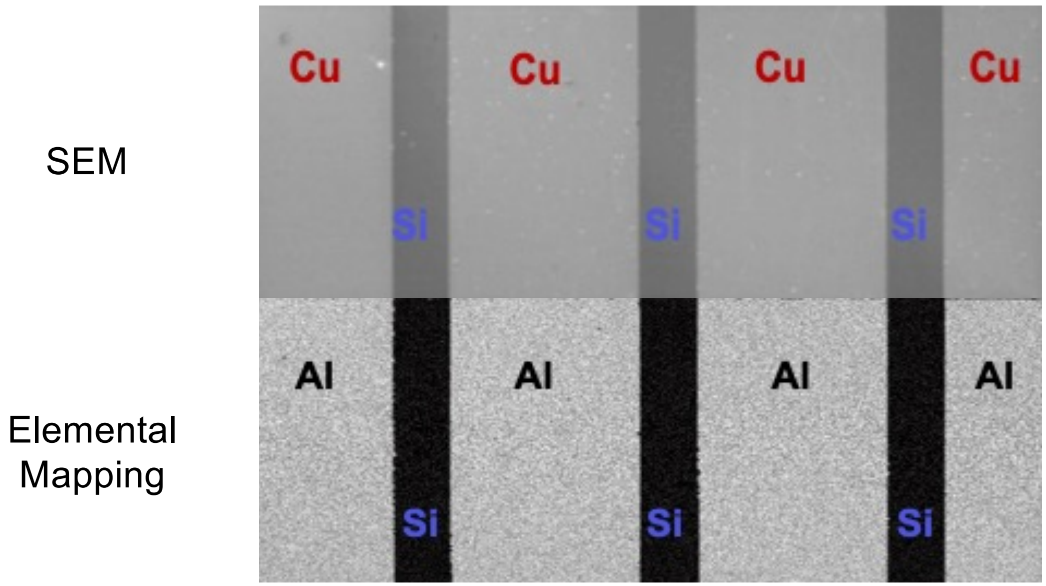
- Process temperature: 150 C

$$S = \frac{R_{gs} - R_{ns}}{R_{gs} + R_{ns}}$$

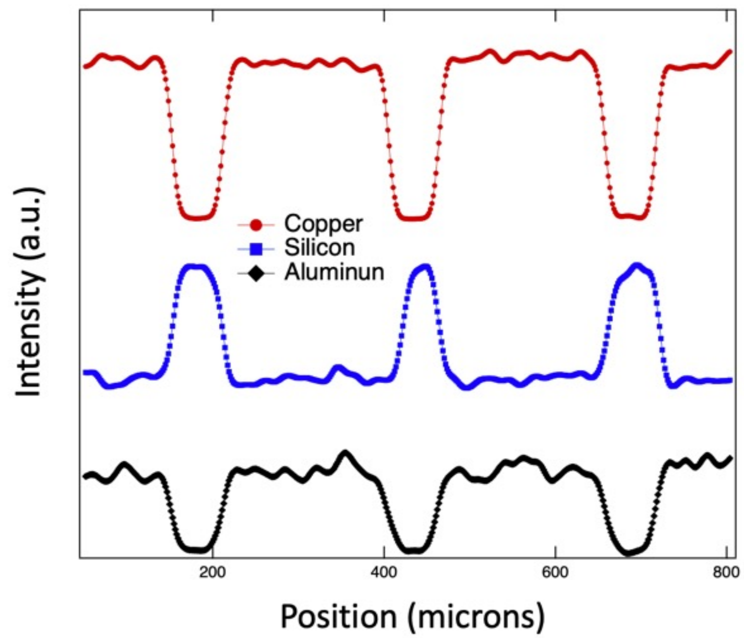
- Using **triethylaluminum (TEA)** vs. trimethylaluminum (TMA) allows for **more selective growth**

J. Yarbrough, F. Pieck, D. Grigjanis, I.-K. Oh, P. Maue, R. Tonner, and S. F. Bent, Chem. Mat, 34 (2022) 4646–4659

Selective ALD on Patterns



Selectivity = 93.7%



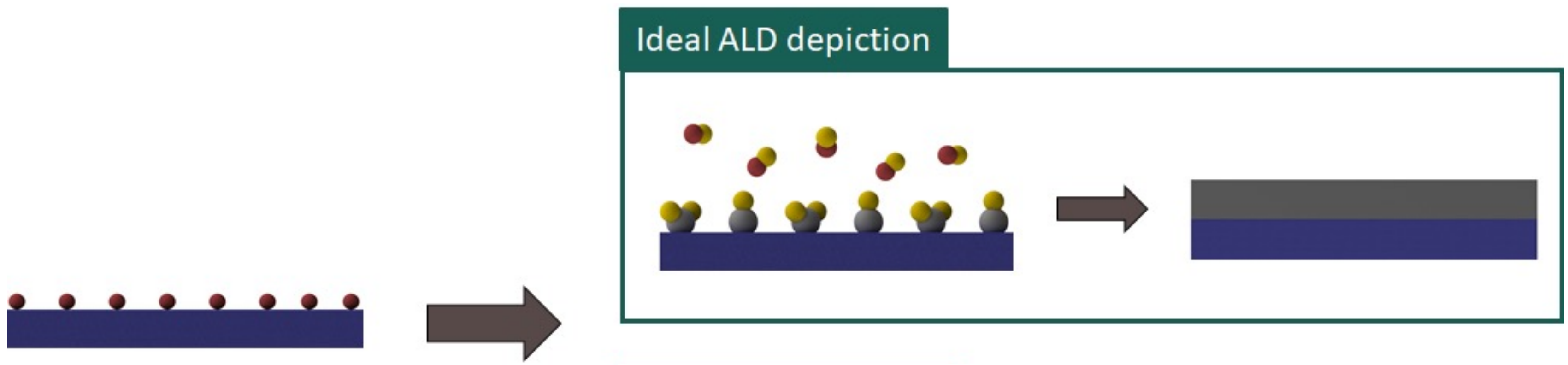
TMPS SMI blocks at least 4 nm ALD on SiO_2, while allowing growth on Cu.

TEA-based ALD performed at 150°C

Complexities of ALD

What we imagine…

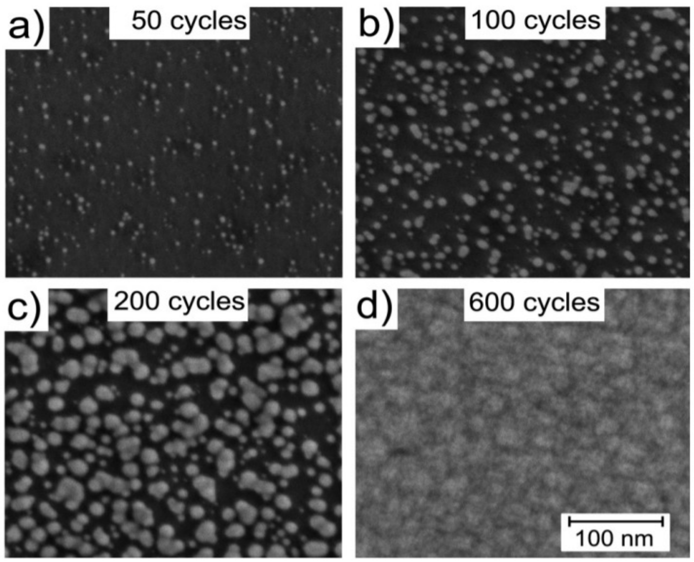
Non-Idealities Lurk Everywhere in ALD



N. E. Richey, C. de Paula and S. F. Bent, J. *Chem. Phys*, **152** (2020) 040902

Metal ALD on Low Surface-Energy Substrates

Pt ALD on SiO_2

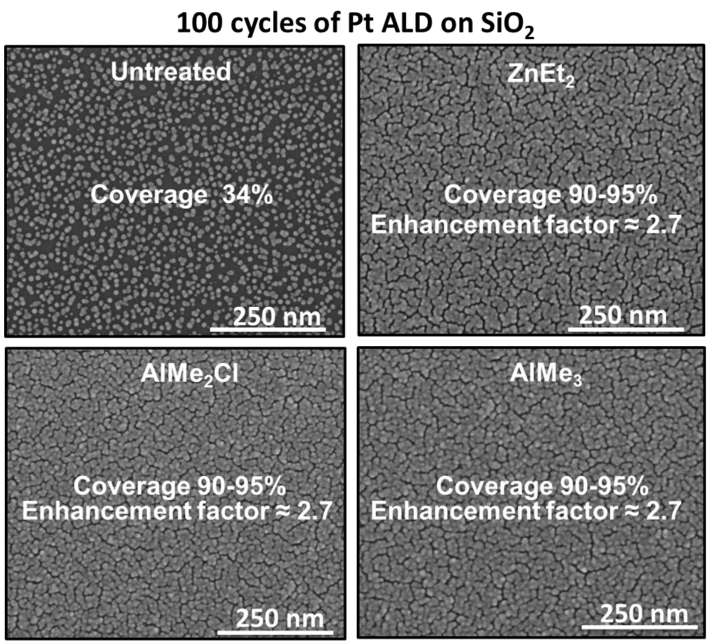


- Thick films upon coalescence
- Pinholes
- Rough films
- Polydisperse grain size

Geyer, S.M., et al. *J. Appl. Phys.* 2014

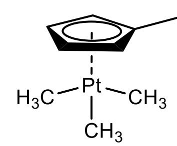
Pt Nucleation Enhancement with Small Molecule Surface Activation

Surface treatment prior to ALD incorporates less than a single monolayer of impurities



Small molecules:

- $ZnEt_2$
- $AlMe_3$
- $AlMe_2Cl$

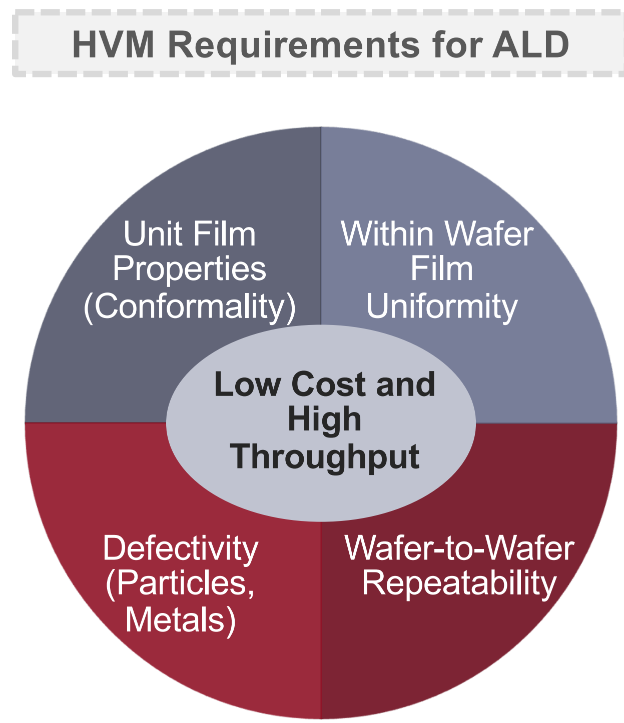


+ O_2 @ 300 °C, Substrate = SiO_2

C. de Paula, L. Zeng, N. E. Richey, and S. F. Bent, Chem. Mat. 32 (2020) 315-325

HVM Requirements for ALD

- Conformality (step coverage)
- Controllable film thickness at angstrom level
- Film continuity / uniformity / pinhole-free
  - Continuity at few nanometer scale film thickness
  - Film roughness
- Compositional control
  - Homogeneity in ternary—or greater—materials
- Reproducibility
- Selectivity (for some applications)
- Process tolerance
  - Temperature, flow, pressure
- Cost and throughput



HVM = high volume manufacturing

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SRC Semiconductor Research Corporation

NEW LIMITS

intel

APPLIED MATERIALS make possible

Merck KGaA, Darmstadt, Germany 350 Research Award

Lam RESEARCH

SAMSUNG

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