

**Comments of the
Semiconductor Industry Association (SIA)
on the Office of Science and Technology Policy (OSTP) “Request for Information; Draft
National Strategy on Microelectronics Research”**

87 FR 56715 (Sep. 15, 2021) [Document No. 2022-19935]

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The Semiconductor Industry Association (SIA) appreciates the opportunity to provide input on the OSTP’s efforts to inform the National Strategy on Microelectronics Research issued by the Subcommittee on Microelectronics Leadership (SML) of the National Science and Technology Council (NSTC).

Responses to Specific Questions from the RFI

- 1. Does the Draft National Strategy capture the key R&D areas that will support future generations of microelectronics? If not, what additional areas of R&D focus are required?*

The Draft Strategy document thoroughly addresses most of the key technologies that should be central to a national microelectronics R&D effort. There are a few areas which seem underdeveloped, and which may need some additional detail. Notably:

- There should be more emphasis on MEMS, analog, RF, and mixed signal devices, as well as the integration of sensors with intelligence and processing.
- R&D for designs should include enhanced device programmability and programmability abstraction.
- The list of processing architectures (OSTC Strategy 1.1.3) should also be expanded to include novel architectures for near-data-processing/processing-in-memory, architectures exploiting heterogeneous integration, hybrid classical/emerging architectures (quantum, neuromorphic), and architectures for new/emerging devices.
- The section concerning heterogeneous integration and chiplet development should discuss the possible creation of an accessible chiplet ecosystem with reusable chiplet design IP and software support that is open and accessible to U.S. institutions and companies.
- The discussion of semiconductor security should include fully encrypted processing (homomorphic), defenses against side channel attacks, and privacy-preserving technologies.

- The discussion of environmental sustainability¹ should clarify that sustainability need not only apply to materials for devices themselves, but also for:
 - Process gases with lower global warming potential.
 - Photolithography chemicals that meet strict functional needs and present an improved environmental profile.
 - New technologies for detection and removal of compounds with extremely low wastewater concentrations, but which nonetheless have a significant environmental impact (e.g. PFAS chemicals).
 - New technologies that satisfy fab requirements while reducing operational demands on energy and water.
- Furthermore, sustainability should be broadened to encompass the full lifetime of semiconductor products beyond only the manufacturing steps (i.e., include lifetime energy consumption and disposal/recycling impacts).
- Innovation for process tools and equipment should be included as well, not only for superior material deposition, layer alignment, and device throughput of existing materials, but also for novel materials that may be challenging to integrate into existing systems.
- The strategy makes reference to “compute-in-memory,” which is one potential application of a convergence between logic and memory chips, including through heterogeneous integration. The more general term, “memory-centric computing,” may be better as it captures the full spectrum of these converging technologies rather the narrower term “compute-in-memory.”

The Draft Strategy document notes many excellent examples of the needs associated with packaging and heterogeneous integration, which are in rough alignment with the needs determined by the industry. However, packaging needs do extend beyond those in support of heterogeneous integration. Examples include technologies and infrastructure for 2.5D and 3D stacking, high-density redistribution, optical packaging and test, fan-out, hybrid bonding, advanced interposers (glass, silicon, high density organic), and fabrication of high-density solder bumps, copper interconnects, and vias.

2. What additional approaches should be considered to develop and expand the microelectronics workforce at all levels, including advanced degrees?

While the discussion within the Draft Strategy is quite comprehensive, some additional areas should be developed further. The document should discuss:

- Expansion of opportunities for students who graduate from high school with technical degrees to be employed in semiconductor manufacturing entry level roles and work on

¹ See SIA comment DOC-2021-0010-0150 to Department of Commerce RFI, “Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry”, pp. 20-23, March 2022 and see SIA Comments to OSTP Identifying Critical Data Gaps and Needs To Inform Federal Strategic Plan for PFAS Research and Development, available at <https://www.semiconductors.org/wp-content/uploads/2022/09/OSTP-research-priorities-8.29.2022.pdf>

post-secondary degrees. This will entail semiconductor manufacturing curriculum in K-12.

- Mechanisms to align community and technical college curricula and training for semiconductor manufacturing to meet some qualifications towards 4-year engineering degrees. Associate of Applied Science (AAS) degrees that prepare technicians for semiconductor fab work do not always transfer to 4-year institutions towards the completion a BA or BS degree. As a result, students must complete an entire 4-year degree from the beginning after completing an AAS.
- Validation of experiential learning experiences for all work-based programs into college credit that will further support underrepresented populations to enter the industry with visible pathways toward a rewarding and long-lasting career.
- Support for additional semiconductor manufacturing courses at community college to ensure students earning degrees are highly qualified as manufacturing automation advances. As we move to greater industry automation and as the complexity of manufacturing increases, coursework will need to evolve to support industry needs.
- Support for learning in community and informal settings should be a priority as well, which will be especially critical for improving access to the semiconductor industry for underrepresented groups.
- The alignment and expansion of federal student aid programs like Pell Grants to support non-traditional pathways and targeted education programs into microelectronics jobs and careers.
- Development of National Standards for semiconductor manufacturing jobs where frameworks define the purpose of an occupation, the job functions that are carried out to fulfill that purpose, the competencies that enable the worker (apprentice) to execute those job functions well, and the performance criteria that define the specific knowledge, skills and personal attributes associated with high performance in the workplace.
- Establishment of a national microelectronics education and training network to upgrade educational laboratory facilities, support curriculum development, and facilitate hiring of faculty into this field.

Furthermore, the Department of Homeland Security should implement existing statutory and regulatory authorities to provide premium processing to newly filed Immigrant Petitions for employment-based second preference advanced degree immigrants seeking a National Interest Waiver to work in microelectronics endeavors.

3. *Are there additional mechanisms that should be considered to ensure rapid transition of R&D to the industry?*

Broadly speaking, the text of the recommendations found in the current Draft Strategy document are quite insightful in noting the possible mechanisms needed for successful implementation of the CHIPS R&D efforts. The strategy correctly cites public-private

partnerships (PPPs) like the Semiconductor Research Corporation (SRC) as good examples of how to bring together multiple parties towards sustained and mutually beneficial technical efforts and notes the value of regional innovations hubs for supporting the workforce and technical needs of a research community. The value of focused use of the Other Transaction Authority (OTA) is also noted as a powerful tool to broaden participation by industry in Federal technology development programs. The Draft Strategy also describes the roles of the National Semiconductor Technology Center (NSTC*) and National Advanced Packaging Manufacturing Program (NAPMP) as supporting the scale-up and prototyping of semiconductor and packaging technologies.

Beyond these priorities, there are some additional considerations that may be helpful:

- The role of IP should be made clear as early as possible. The NIST Special Publication NIST SP 1282 clarifies that individually developed IP should be individually owned, while IP developed jointly should be jointly owned; and (b) the NSTC should retain rights only when IP is developed jointly with facility staff. To maximize industry participation and remove potential chilling effects on innovation, the treatment of joint IP generated from NSTC*-directed research areas should be structured favorably for commercialization by the companies who participated in the relevant research effort, and should be fully clarified. This model is consistent with past federal efforts by agencies like NASA, which agreed to allow companies involved in the Commercial Orbital Transportation Services (COTS) program to retain the IP they generated.² In other circumstances, commercialization of research results can be achieved more widely and promptly by granting non-exclusive licensing rights to the sponsors of the research results. Such companies typically have a need for the technology, have closely monitored its development and are prepared to commercialize it. In any event, the IP rights should be designed for the particular research circumstances at hand by those funding and participating in the research project.
- In evaluating potential IP licensing partners, the Departments and Agencies should ensure consideration of licensees from foreign allies that can attest to the net-benefit of licensure of the technology, and its subsequent commercialization, to the U.S. economy and industrial base. Because the cost of commercializing semiconductor technology is often prohibitively expensive, it is essential that the pool of interested licensees be as broad as possible, while balancing security concerns and vetting of licensees. This approach towards IP licensing will expand the pool of licensees that can credibly and effectively commercialize a technology, accelerate capital contributions to overcome the commercialization valley of death, and encourage a more resilient semiconductor ecosystem.
- It should be clear how the NSTC* and NAPMP will interact with the DoD National Network for Semiconductor R&D. The National Network for Semiconductor R&D is

² American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, November 2021, 18

intended to enable lab-to-fab transition of microelectronics innovations in the U.S. and expand U.S. microelectronics leadership. These tasks may be best accomplished in close partnership with the NSTC* and leveraging the prototyping capabilities that will be created as a part of the broader NSTC* and NAPMP efforts. To avoid duplication of effort and to best allow companies to predict the deployment of infrastructure, the relationship between these efforts should be clarified.

- The NSTC* and NAPMP should be aligned as closely as possible, given the strong overlap between packaging and core semiconductor technology needs and capabilities and given the need for cross-stack co-design (spanning devices, packaging, circuits, tools, architecture, and software).
4. *Do you have any additional suggestions on how the final National Strategy can help ensure the success of the broader CHIPS efforts and ensure continued U.S. leadership in this important area?*
- Industry Engagement – Research goals should be informed by industry participants at each step and should help drive towards the broad technology needs of downstream sectors. Documents like the SRC decadal plan³ help provide long-ranging grand challenges which were developed with thorough industry input, and which describe vastly cross-disciplinary challenges.
 - Clarity of prioritization – A broad list of technology goals is somewhat helpful, but there will be vast differences in the benefits, challenges, and relative costs of pursuing different R&D goals. It may be helpful to convene industry and government stakeholders to help determine, at a high level, the relative prioritization of certain research areas.
 - Road mapping – While the exhaustive list of R&D categories of interest are roughly covered in the existing Draft National Strategy document, and the broad system-level goals are described in other documents (e.g., the SRC decadal plan³ or IEEE Heterogeneous Integration Roadmap⁴), the intermediate steps of technology development are also key questions for the broad microelectronics R&D strategy, though perhaps outside the scope of the draft strategy. Regardless, a strategy for future road mapping activities could be considered.
 - Periodic reassessment – The microelectronics technology sector is fast-moving, and any published set of technology priorities can become outdated relatively quickly. This strategy document should be considered a starting point, and updated R&D strategy documents could be released periodically to account for the often uneven and unexpected rate of progress in different technology areas. The mechanism for updating the R&D priorities should be informed, in part, by the above three categories (industry engagement, clarity of prioritization, road-mapping).

³ See “The Decadal Plan for Semiconductors,” January 2021, <https://www.src.org/about/decadal-plan/>

⁴ <https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html>