American Semiconductor Research

Leadership Through Innovation

November 10, 2022
2022 CHIPS & SCIENCE ACT
Signed summer 2022 in historic win for the industry

$39 billion manufacturing incentive program
25% manufacturing investment tax credit (estimated at $24.3 billion over duration of credit)
$13 billion in R&D and workforce investment
CHIPS R&D IMPLEMENTATION

Goal: Promote collaborative R&D ecosystem

Key investment areas for NSTC and NAPMP

- Support transition pathways for innovative technologies
- Upgrade research infrastructure for early-stage ecosystem
- Establish and expand access for mid-stage development and prototyping infrastructure
- Convene industry, academia, and government for collaborative innovation partnerships
- Promote dynamic workforce programs to increase and hone domestic workforce
## CHIPS AND SCIENCE - FUNDING ALLOCATION

$13B overall

### Authorized programs in CHIPS Act

<table>
<thead>
<tr>
<th>Dept.</th>
<th>Program</th>
<th>Statutory objectives</th>
</tr>
</thead>
<tbody>
<tr>
<td>White House Office</td>
<td>Sub-committee on microelectronics leadership</td>
<td>Create national strategy on microelectronics research</td>
</tr>
<tr>
<td>Commerce</td>
<td>Industrial Advisory Committee</td>
<td>Assess effectiveness of national strategy</td>
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<tr>
<td></td>
<td>Semiconductor incentives</td>
<td>Construct, expand, or modernize fabs located in US</td>
</tr>
<tr>
<td></td>
<td>National Semiconductor Technology Center (NSTC)</td>
<td>Strengthen security of supply chain and economic competitiveness, public-private partnership</td>
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<tr>
<td>Commerce (NIST)</td>
<td>National Advanced Packaging Mfg. Program</td>
<td>Strengthen domestic advanced test, assembly, packaging capabilities</td>
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<td></td>
<td>Manufacturing USA institute</td>
<td>Develop and cultivate semi. manufacturing capabilities in the US</td>
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<tr>
<td></td>
<td>Microelectronics research</td>
<td>Accelerate R&amp;D for metrology of next-generation microelectronics</td>
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<tr>
<td>Defense</td>
<td>National Network for Microelectronics Develop.</td>
<td>Enable lab-to-fab transition of microelectronics innovations</td>
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<tr>
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<td>Defense Microelectronics</td>
<td>Incentivize consortia for measurably secure microelectronics</td>
</tr>
<tr>
<td>Treasury/State</td>
<td>Multilateral Semiconductor Security Fund</td>
<td>Develop and promote secure semi. supply chains with allies</td>
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</tbody>
</table>

- **$11B** for discussed programs
- **$2B** for other programs

Dedications status:
- **Dedicated funding**
- **No Dedicated funding**
# Semiconductor Research - Stages of Development

Innovations traverse 5 phases before volume production

<table>
<thead>
<tr>
<th>Portfolio</th>
<th>Phases of innovation leading to volume production</th>
<th>Public support example (non-exhaustive)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Many, small bets</td>
<td><strong>Basic research</strong></td>
<td>- National labs (e.g., Sandia, Lincoln Laboratory, etc.)</td>
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<tr>
<td>$</td>
<td><strong>Applied research</strong></td>
<td>- Nanofabrication facilities network</td>
</tr>
<tr>
<td>Rising investment needs, financial risks by orders of magnitude</td>
<td><strong>Pathfinding and prototyping (development)</strong></td>
<td>- DoD Manufacturing Technology (ManTech)</td>
</tr>
<tr>
<td>Few, large bets</td>
<td><strong>Piloting (development)</strong></td>
<td>- Incentives (e.g., tax credits)</td>
</tr>
<tr>
<td>1-2 innovations in production</td>
<td><strong>Scaling to volume production (development)</strong></td>
<td>- Various security and defense programs (e.g., In-Q-Tel)</td>
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<tr>
<td></td>
<td></td>
<td>- Incentives (e.g., tax credits)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Various security and defense programs (e.g., Title III DPA)</td>
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</table>

1. Precompetitive, often fundamental research designed to expand knowledge; findings typically shared widely.
2. Often post-competitive and proprietary research that can occur in companies or academia and builds on basic research.
3. Viability assessment and creation of a small number of working semiconductors that meet desired criteria.
4. Manufacturing of finished semiconductors in scale amounts on actual fabrication processes.
5. Scaling up production of pilot manufacturing processes to commercially useful volumes.
RESEARCH LANDSCAPE: NSTC/NAPMP & Valley of Death

Funder
- NSF
- DOE Office of Science
- ARPA-E
- SRC
- DOE EERE
- SBIR/STTR
- NASA
- DOD Branch Labs
- Manufacturing USA Institutes
- DOD FFRDCs & UARCs
- Albany Nanotech Complex

Performer
- DOE National Labs
- University & NNCI
- NIST Laboratories
- IMEC*
- Industry Labs & Fabs

NSSTC/NAPMP
- DARPA/IARPA
- AFOSR/ARO
- ONR
- DOD ManTech
- DIUx
- Title III DPA
- In-Q-Tel

Basic research
Applied R&D
Prototyping
Piloting
Scaling to production

- Broadly Serving Activity Range
- DOD/IC Serving Core Focus
- Not US-based, but accessible to US researchers

Private labs conducting publicly funded R&D
PARTNERSHIP FROM RESEARCH THROUGH PRODUCTION

Collaboration across ecosystems for full-stack approach

To be successful, the NSTC and NAPMP should have **wide industry representation** to:

- Build a diversified **technology and infrastructure portfolio** for research and development
- Facilitate **collaborative development** more effectively
- Maintain a **wide network of industry partners**, including their suppliers and needs of both

Note: Graphic designed to illustrate need for NSTC to collaborate widely and is not exhaustive
Thank You
semiconductors.org