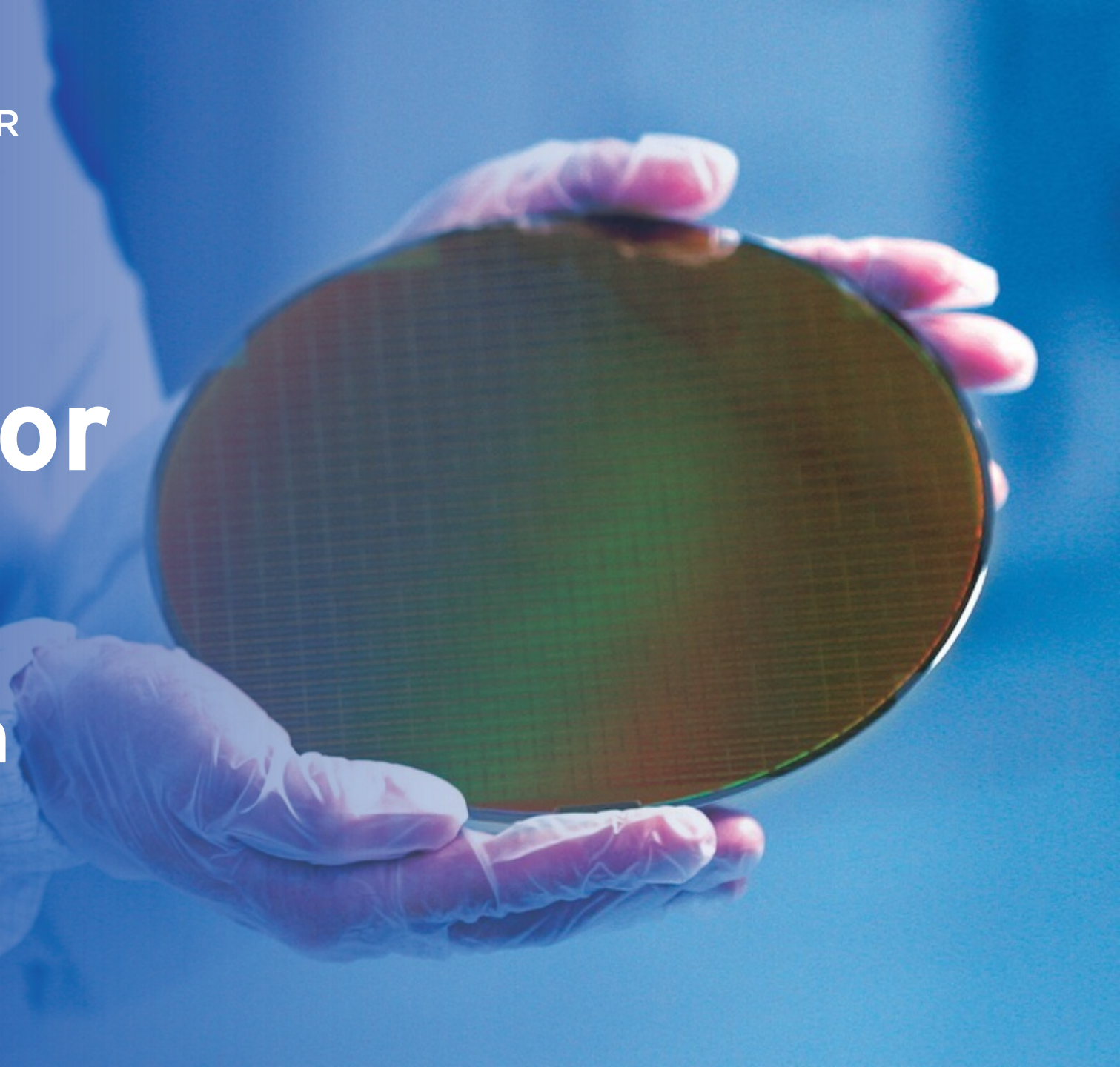
SEMICONDUCTOR INDUSTRY ASSOCIATION

American Semiconductor Research

Leadership Through Innovation

November 10, 2022



2022 CHIPS & SCIENCE ACT

Signed summer 2022 in historic win for the industry

$39 billion manufacturing incentive program

25% manufacturing investment tax credit (estimated at $24.3 billion over duration of credit)

$13 billion in R&D and workforce investment

CHIPS R&D IMPLEMENTATION

Goal: Promote collaborative R&D ecosystem

Key investment areas for NSTC and NAPMP

- Support transition pathways for innovative technologies
- Upgrade research infrastructure for early-stage ecosystem
- Establish and expand access for mid-stage development and prototyping infrastructure
- Convene industry, academia, and government for collaborative innovation partnerships
- Promote dynamic workforce programs to increase and hone domestic workforce

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CHIPS AND SCIENCE – FUNDING ALLOCATION

$13B ov

Authorized programs in CHIPS Act

Dept.	Program	Statutory objectives	
White House Office	Sub-committee on microelectronics leadership	Create national strategy on microelectronics research	
Commerce	Industrial Advisory Committee	Assess effectiveness of national strategy	
Commerce (NIST)	Semiconductor incentives	Construct, expand, or modernize fabs located in US	$11B
	National Semiconductor Technology Center (NSTC)	Strengthen security of supply chain and economic competitiveness; public-private partnership	
	National Advanced Packaging Mfg. Program	Strengthen domestic advanced test, assembly, packaging capabilities	
	Manufacturing USA institute	Develop and cultivate semi. manufacturing capabilities in the US	
	Microelectronics research	Accelerate R&D for metrology of next-generation microelectronics	
Defense	National Network for Microelectronics Develop.	Enable lab-to-fab transition of microelectronics innovations	$2B
	Defense Microelectronics	Incentivize consortia for measurably secure microelectronics	
Treasury/State	Multilateral Semiconductor Security Fund	Develop and promote secure semi. supply chains with allies	

Discussed in this report

Dedicated funding

No Dedicated funding

SEMICONDUCTOR RESEARCH – STAGES OF DEVELOPMENT

Innova

Innovations traverse 5 phases before volume production

Portfolio

Many, small bets

Rising investment needs, financial risks by orders of magnitude

Few, large bets

1-2 innovations in production

Phases of innovation leading to volume production

1	**Basic research**	Precompetitive, often fundamental **research designed to expand knowledge**; findings typically shared widely
2	**Applied research**	Often post-competitive and **proprietary research** that can occur in companies or academia and builds on basic research
3	**Pathfinding and prototyping** (development)	Viability assessment and creation of a **small number of working semiconductors** that meet desired criteria
4	**Piloting** (development)	Manufacturing of finished semiconductors in **scale amounts on actual fabrication processes**
5	**Scaling to volume production** (development)	**Scaling up production** of pilot manufacturing processes to commercially useful volumes

More collaborative — More proprietary

Public support example

(non-exhaustive)

- National labs (e.g., Sandia, Lincoln Laboratory, etc.)
- Nanofabrication facilities network
- DoD Manufacturing Technology (ManTech)
- Incentives (e.g., tax credits)
- Various security and defense programs (e.g., In-Q-Tel)
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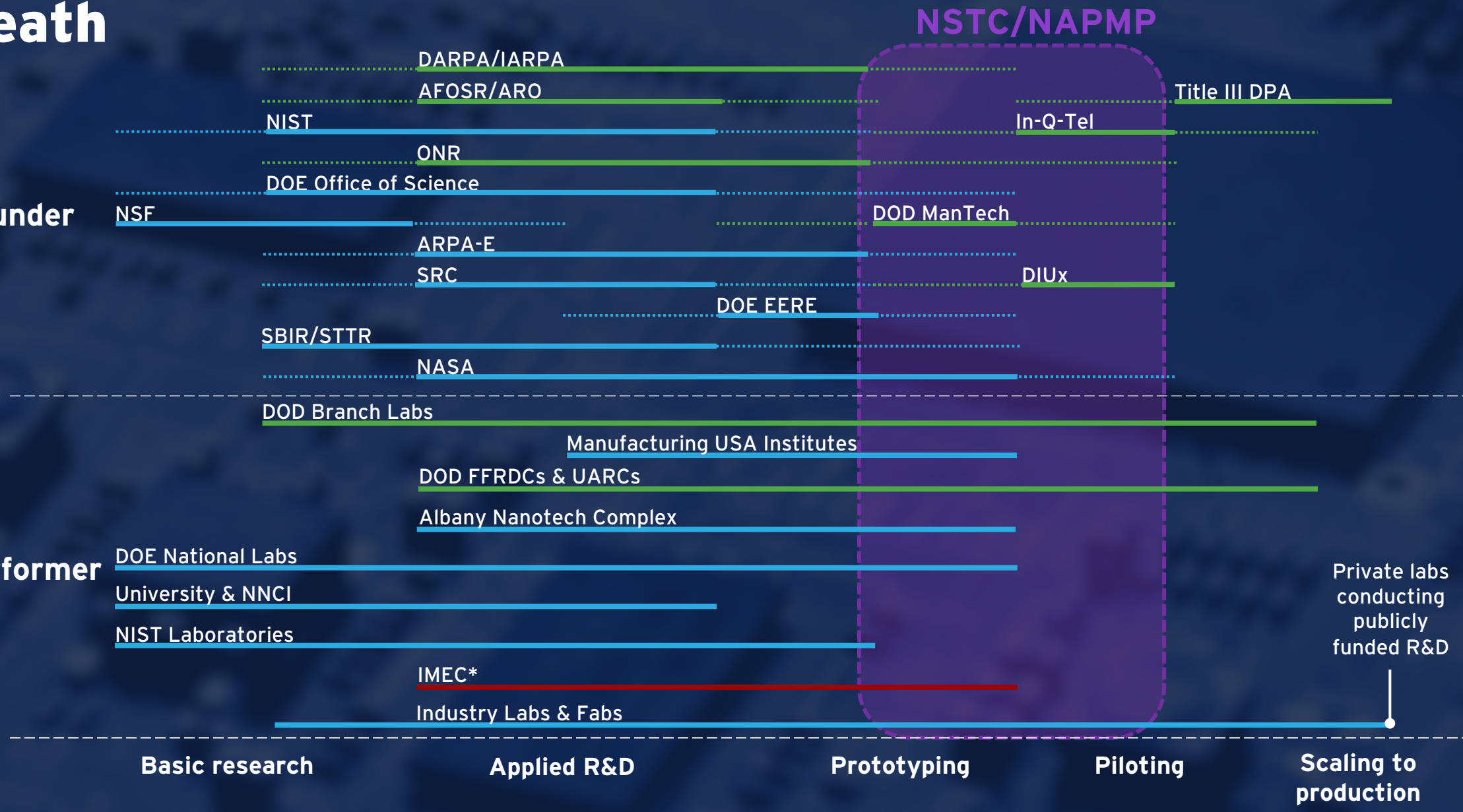
RESEARCH LANDSCAPE: NSTC/NAPMP & Valley of Death



PARTNERSHIP FROM RESEARCH THROUGH PRODUCTION

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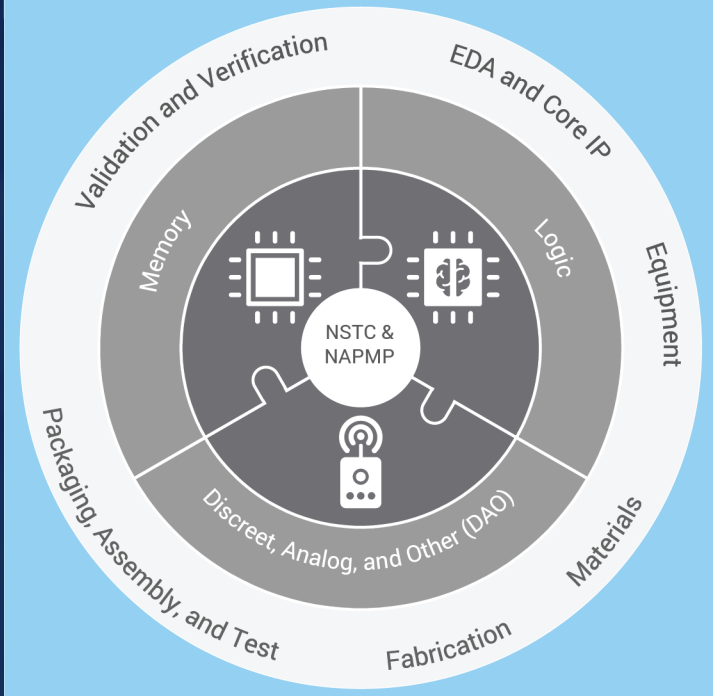
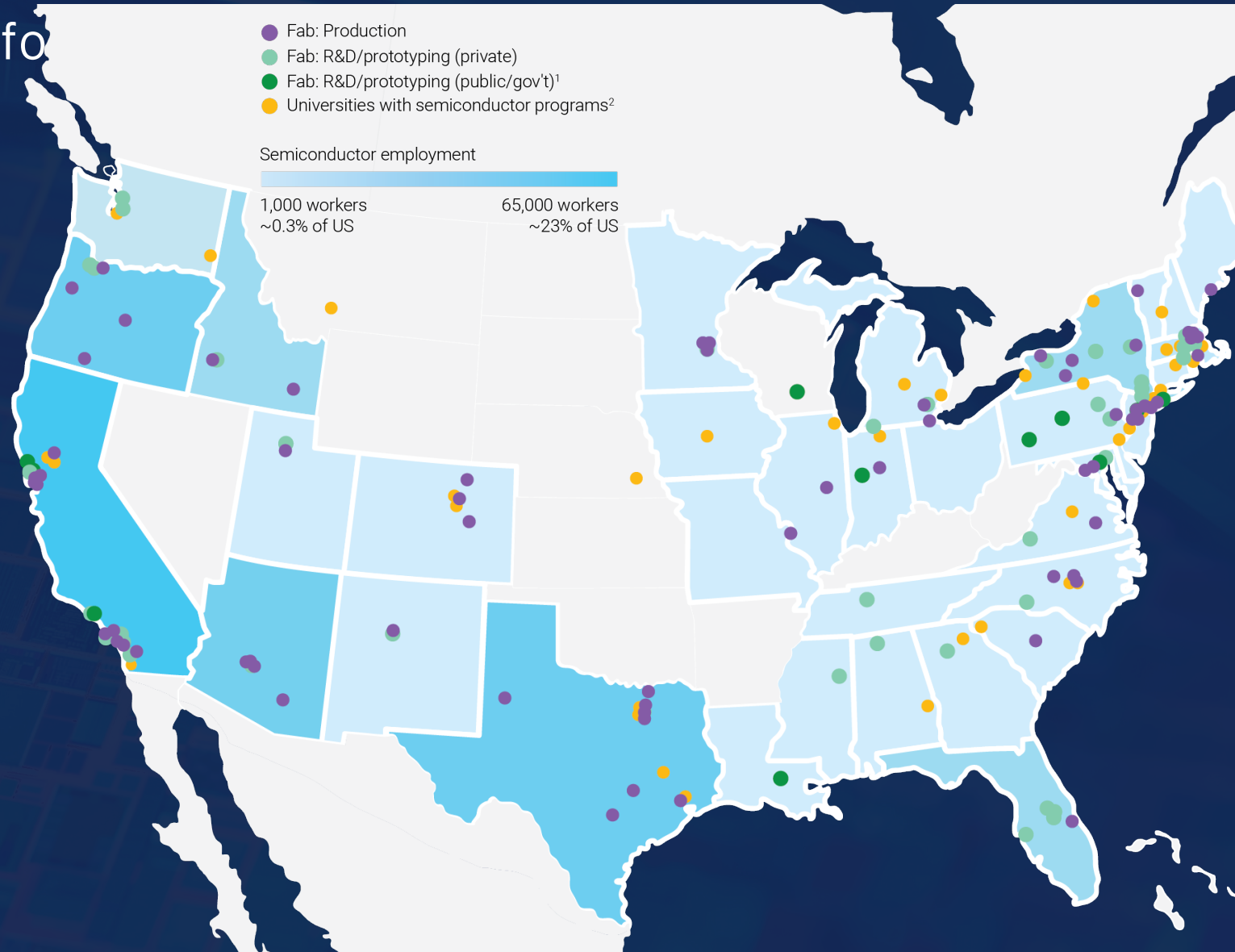


To be successful, the NSTC and NAPMP should have **wide industry representation** to:

- Build a diversified **technology and infrastructure portfolio** for research and development
- Facilitate **collaborative development** more effectively
- Maintain a wide **network of industry partners**, including their suppliers and needs of both

Note: Graphic designed to illustrate need for NSTC to collaborate widely and is not exhaustive



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Thank You

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