Chips Act R&D Efforts- Key Priorities & Innovation Opportunities
An IBM Perspective

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Key Priorities for Chips R&D

- **Democratize** access to advanced semiconductor technologies & spur design innovation
- **Accelerate** Open Chiplet Ecosystem for next generation of system architectures
- **Reduce** cost of chip design by EDA modernization

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The AI imperative

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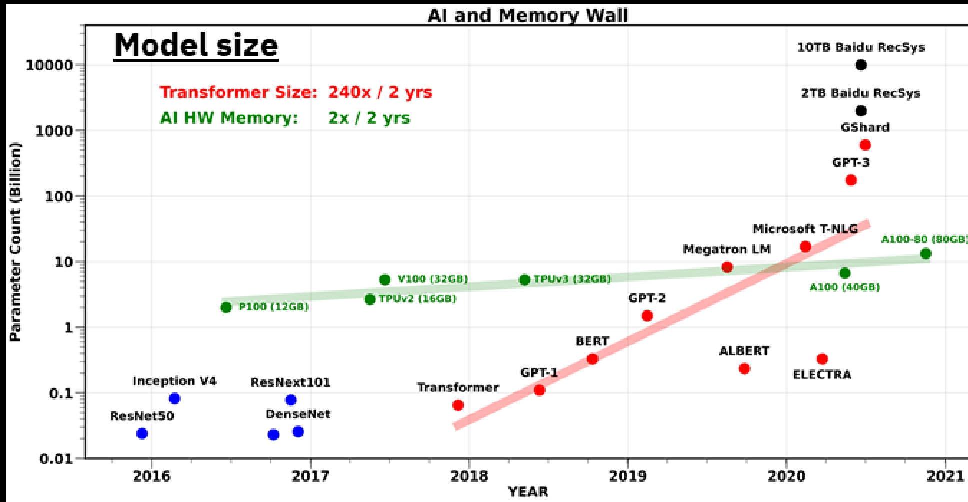
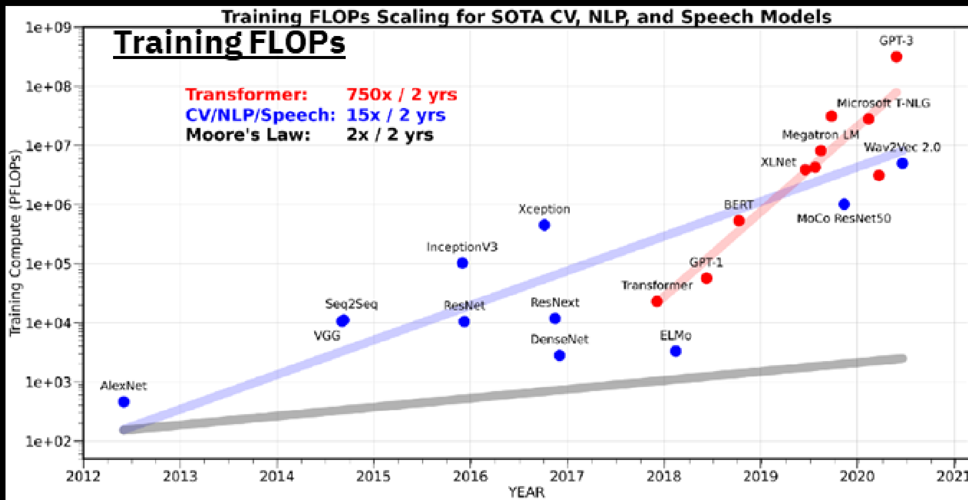
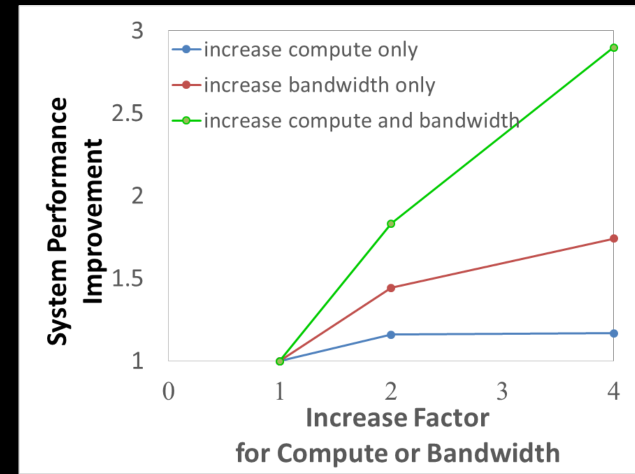




https://medium.com/riselab/ai-and-memory-wall-2cb4265cb0b8/ 8



A. Kumar, IEDM 2018

- Reduced-precision to increase compute efficiency
- Overcome von-Neumann bottleneck with:
  - Near-memory compute (*mitigate*)
  - In-memory compute (*eliminate*)
  - Increased memory bandwidth with Advanced Packaging or Heterogeneous Integration

Unsustainable without innovations across-the-stack, including in:
Materials, Devices, Algorithms, Accelerators & Software.

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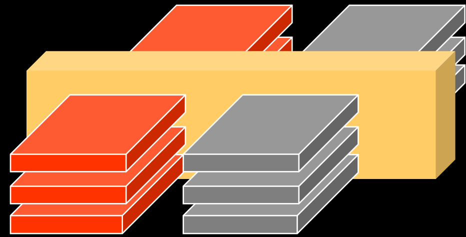
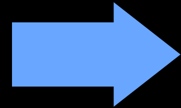
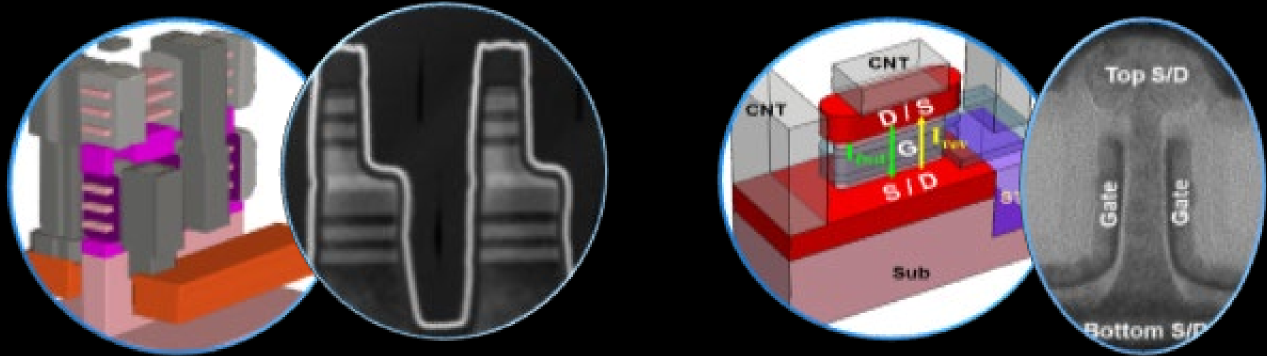
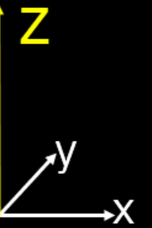
Semiconductor Innovations for Sustained US Leadership





Nanosheet





Stacked Transistor ,Vertical Transport Transistor

- Device architectures for vertical stacking
- Enable backend scaling beyond Cu- Novel materials, process and integration
- High-NA EUV lithography

Novel dielectric materials, Novel & subtractive conductors beyond Cu, High- NA EUV

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Democratize Access to Advanced Semiconductor & HI Technology

Nanosheet- Democratize Access to Adv. Logic

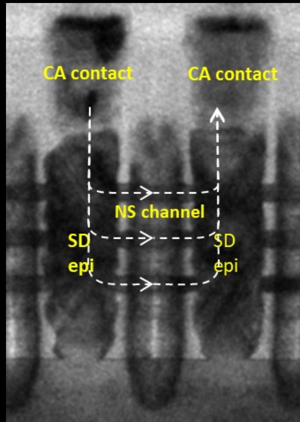
- Demonstrate IP and functional circuit blocks with Nanosheet technology
- Nanosheet technology PDK
- MPW run using the Nanosheet Technology

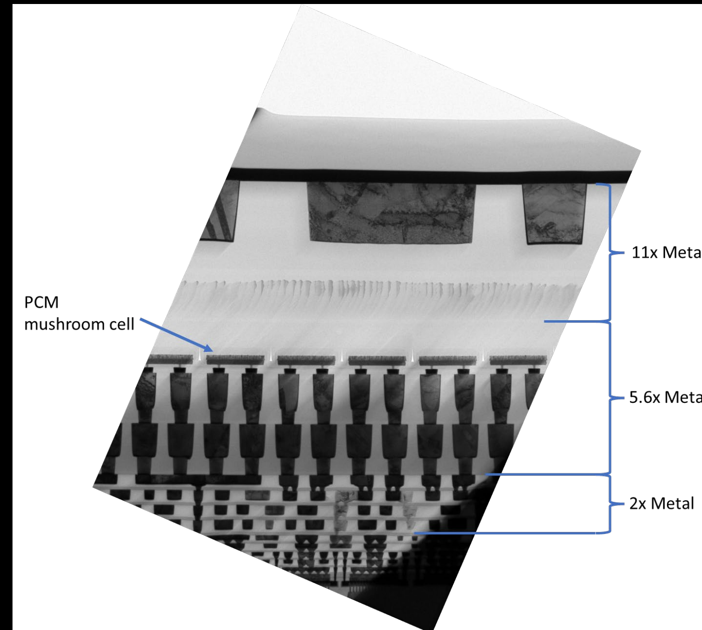
Embedded NVM in leading edge CMOS For In-Memory & Near Memory Compute

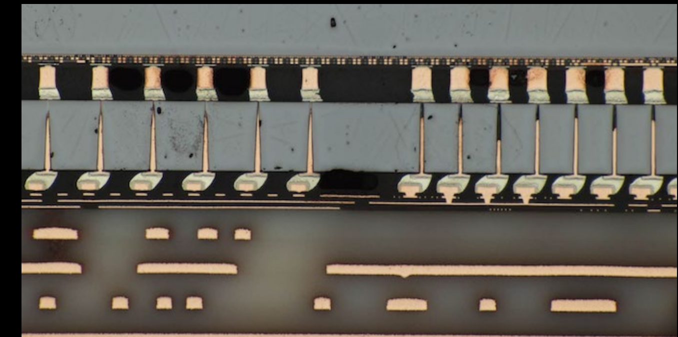
- Demonstrate In-mem/near mem compute with embedded NVM
- MPW runs with enhanced PDK & relevant I/O IP

Next Generation HI Technologies- For 3D Chiplet and increased BW for System performance

- RDL for multilevel high density chiplet interconnect
- 3-D Integration for high bandwidth applications with scalable interconnect density







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Open Chiplet Ecosystem for future System Architectures

Accelerate system design-level innovation with ***NSTC & NAPMP.***

Open Chiplet Ecosystem- Breaking Down Barriers

- **Democratize access to chiplet-based architecture for innovation from die stacking to full system level**
  - Open standards of die-die communication
  - Availability of affordable chiplet prototypes
  - EDA tool enhancement for package-level design
  - Workload-based chiplet platform
- **Enables SMB to work with large companies**
  - *Open standards would facilitate participation*
- **Open access to all** including start-ups, small companies, and academia

Emerging open standard candidates for communication protocol across the stack:

- Bunch of Wires (BoW)
- Universal Chiplet Interconnect Express (UCIe)
- Open Memory Interface (OMI)
- Compute Express Link (CXL)

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EDA Modernization: Platform for Designers to Scale Their Workloads on the Cloud

1. Transitioning EDA design flows to Cloud *

- Capability to optimize infrastructure to specific workloads
- Automated provision of **useable** cloud resources
- Opportunity for tailoring algorithms to leverage microservices in the cloud for increased parallelism

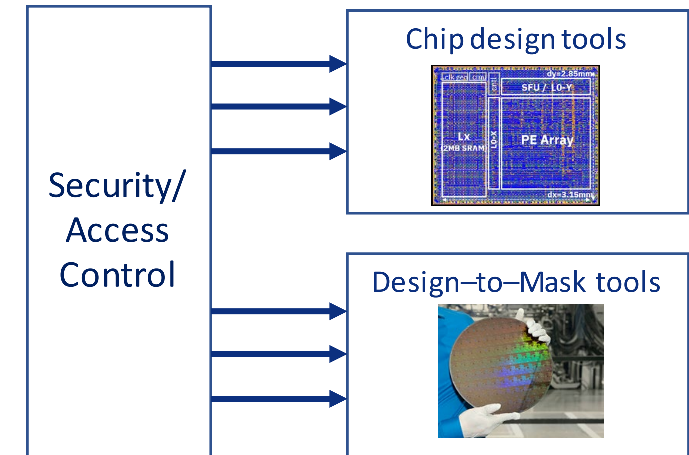
2. AI/ML-driven Design Flow Orchestration

- Scalable workload executions
- AI/ML-driven design capabilities

3. Design Productivity Improvement

- Improvements in TAT and Quality of Results (QoR)

SYNOPSYS SIEMENS CADENCE

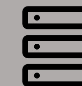


Cloud native orchestration

Kubernetes Service

EDA-optimized hybrid cloud infrastructure

On Prem



Industry Cloud

Other cloud providers

* D.N. Dunn, G. Singh, Y. Cui, et al., "Hybrid Cloud Bursting Electronic Design Analysis Optical Proximity Correction (OPC) Flows to Public Cloud Managed Kubernetes Services", Kubecon HPC+Batch Day, Oct 2022

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