SEMICONDUCTOR INDUSTRY ASSOCIATION

Comments of the
Semiconductor Industry Association (SIA)
On the
National Institute of Standards and Technology Request for Information
On
Manufacturing USA Semiconductor Institutes

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The Semiconductor Industry Association (SIA) appreciates the opportunity to comment on the Request for Information (RFI) by the National Institute of Standards and Technology (NIST).

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Responses to Specific Questions from the RFI

Institute Scope

1. *The Manufacturing USA semiconductor institute program is one component of an $11 billion R&D effort that includes the National Advanced Packaging Manufacturing Program, the National Semiconductor Technology Research Center and the NIST laboratories. The entire R&D program is intended to be interconnected and comprehensive, with no gaps and minimal redundancy, to position the United States for technology and workforce leadership in the semiconductor and microelectronics sector for the long-term prosperity of the nation. Additionally, the Manufacturing USA authorizing statute specifies that new institutes must not substantially duplicate the technology focus of any other Manufacturing USA institute. From your perspective, what role do you envision for new Manufacturing USA semiconductor institutes that will best complement the other R&D investments and remain consistent with the programmatic purposes of Manufacturing USA? Since the Secretary of Commerce may award financial assistance to any existing Manufacturing USA institutes for work relating to semiconductor manufacturing, what role do you envision for existing, federally-sponsored Manufacturing USA institutes with respect to semiconductor manufacturing?*

There are key, high-level considersations that must be accounted for in advance of the establishment of new Manufacturing USA Institutes.

1. A new Institute targeting semiconductor technologies must fully account for the scope and goals of the National Semicondctor Technology Center (NSTC), National Advanced Packaging Manufacturing Program (NAPMP), and DoD Microelectronics Commons, and avoid any substantial overlap in responsibilities
2. A new Institute must account for the existing landscape of Institutes
    a. It is important to enhance existing Institutes where possible in addition to standing up new Institutes for two reasons: 1) these Institutes already have active membership and are further along their trajectory to self-sustainability than a new Institute would be and 2) these Institutes have already convened regional

innovation centers of gravity and it is imperative not to disrupt successful ecosystems by cannibalizing components of their mission

b. Some Institutes, such as AIM Photonics, NextFlex, Power America, or Advanced Functional Fabrics of America already pursue specialty technologies that are core or tangential to semiconductor R&D (though new funding opportunities may want to include more mainstream semiconductor technology development) – these should be enhanced with CHIPS funding where appropriate and integrated into the broader CHIPS act semiconductor ecosystem with advisement and direction from the CHIPS Industrial Advisory Committee
c. Some Institutes, such as Advanced Robotics for Manufacturing or The Cybersecurity Manufacturing Innovation Institute, pursue technologies that could enhance semiconductor manufacturing with additional funding to add a semiconductor specialization area – these should be considered for CHIPS funding if such added specialization is found cost effective

3. Membership and participation will be critical for long-term sustainability and the establishment of excessive overlapping organizations (Institutes, NSTC centers, etc.) put a strain on industry resources and personnel

2. *The technological breadth of innovation in semiconductors and microelectronics is likely larger than can be served by any single Manufacturing USA institute. Therefore, each Manufacturing USA semiconductor institute should have an appropriate scope to ensure that each institute is impactful and does not duplicate efforts of other programs. Historically, institutes in the current network of existing Manufacturing USA institutes have generally been funded for an initial 5 years at $150 million to $600 million, including federal funding and cost-sharing (co-investment) from non-federal partners. What would be the ideal scope and corresponding financial investment from federal and non-federal partners, for a Manufacturing USA semiconductor institute to achieve the needed impact on competitiveness?*

It is difficult to provide a meaningful answer to this question without first understanding the goals and scope of the other components of the CHIPS act R&D ecosystem (NSTC, NAPMP, Commons) and then without understanding how the Manufacturing USA Institutes will cut across those other efforts or serve to fill in the technology gaps not served by those broader efforts. That said, not all semiconductor R&D efforts will have similar costs associated with their activities and not all technology areas have the same level of infrastructure maturity within the United States. For example, it would make sense to focus on technology areas that are complementary and not duplicative of NSTC and NAPMP efforts, such as semiconductor fabrication or packaging facility design and operations or product testing. Such an Institute would merit a larger investment, such as $600M over 5 years. Note that even packaging is not necessarily a less costly area for research, since the tools and equipment required for the most advanced of advanced packaging technology are similar to tools and equipment for wafer fabrication. Meanwhile, an Institute with a more focused scope in an area of greater infrastructural and technical maturity, such as design virtualization and visualization, could still provide an impact with a smaller investment.

3. *Potential technology areas of focus that could be addressed by the Manufacturing USA semiconductor institutes to complement the National Advanced Packaging*

Manufacturing Program and the National Semiconductor Technology Research Center in Question 1 are listed below. What are your thoughts on the appropriateness of each for the scope of work for a Manufacturing USA semiconductor institute? What other topics should be included in the scope of an institute?

- *Chip-package architectures and co-design of integrated circuits and advanced packaging. May include artificial intelligence, security, test methodologies, etc.*
- *Technologies to increase the microelectronics manufacturing productivity of American workers, lower costs and offset the drastic shortfall of skilled workers.*
- *Assembly and Test metrologies to develop new analytical equipment and analysis capabilities based upon standards.*
- *Coding and system software with novel computing paradigms and architectures, including chiplet compatibility with earlier generations.*
- *Integration of security into packaging, interposers and/or substrates.*
- *High Density Interposers and substrates, incorporating new materials and designs.*
- *Chiplet-enabled trusted packaging facilities that obviate the need for trusted foundries.*
- *New materials, such as glass for substrates, or compound semiconductors.*
- *Environmental Sustainability for semiconductor manufacturing.*
- *Analog and Gigahertz Technology materials and metrology, enabling beyond 5G, the Industrial Internet of Things and Industry 4.0.*
- *Performance and Process Modeling and Metrology*

All topics proposed above are appropriate for the scope of work for a Manufacturing USA semiconductor institute as long as they all are addressed in a synergetic/integrated way. It is also important to include some additional potential topics: digital processing, MEMS, fab virtualization and digital twins, integration of AI capabilities into manufacturing processes, photonic technology integration. Once again, it is imperative that the new Manufacturing USA semiconductor institute integrates both microelectronic and advanced packaging topics (again, without overlap of the NAPMP), rather than focusing on one or several stand-alone technical areas. Benchmarking advances in both areas would be valuable to drive and deliver the overall needs of the systems as called out by the 2030 Decadal Plan for Semiconductors .

4. *What criteria should be used to select technology focus areas in delineating the scope for a Manufacturing USA institute focused on semiconductor manufacturing?*

The Manufacturing USA institutes should serve as early TRL feeders for the NSTC and NAPMP for technology areas of interest, or should support cross cutting technologies that may enhance the efforts of multiple NSTC nodes while not clearly falling into one area. Ultimately, any technologies matured through the Institutes and (eventually) the NSTC will require further development and scale-up from the semiconductor industry. As such, it is critical to secure technological buy-in from semiconductor companies at an early stage. Some criteria to consider are:

- Based on the consensus of US semiconductor industry and related roadmaps
- Hardware-centric
- Emphasize advanced packaging as an enabler of the next microelectronic revolution (whole operating as a complement to the NAPMP)
- Must synergistically include both advanced packaging and microelectronics components

- Strong emphasis on semiconductor workforce development

5. *What technology focus areas that meet the criteria suggested in Question 4 above would you be willing to co-invest in?*

No comment provided

Institute Structure and Governance

6. *Existing Manufacturing USA institutes were launched and operate in alignment with the design principles published in 2012 as the National Network for Manufacturing Innovation: A Preliminary Design (https://www.manufacturingusa.com/ reports/ national-network-manufacturing-innovation-preliminary-design). Are there any unique considerations for the semiconductor and microelectronics sector that may require modifications to the conventional design for any Manufacturing USA semiconductor institutes under consideration?*

No comment provided

7. *Semiconductor R&D and manufacturing cover substantial technical breadth. What business models or best practices should be employed by a Manufacturing USA semiconductor institute to support U.S. leadership and effectively manage emerging technologies to support commercialization? What advantages or disadvantages would there be to one "super-sized" Manufacturing USA semiconductor institute that would cover the technology sector broadly? Since Congress authorized the NIST Director to establish up to three institutes, what advantages or disadvantages would there be for multiple Manufacturing USA semiconductor institutes each with a smaller scope focused on a specific technology area? How would one Manufacturing USA semiconductor institute or multiple institutes structure relationships with other significant partners to spur collaborative work?*

Multiple specialized Manufacturing USA institutes could make powerful partners for the NSTC in workforce training, the development of new capabilities, and as a supplier of ideas and technology into industry, the NSTC, and the NAPMP. As addressed in question 2, the value of a "super-sized" institute would depend on the technology area in question and it would be critical to identify how a "super-size" Manufacturing USA Institute might be different from the NSTC.

The risk of multiple institutes is that the creation of too many new Institutes, in addition to those that already exist and the new NSTC effort, could necessitate significant overlaps in membership. This could risk "membership fatigue", where firms are either reluctant to join so many efforts at once without a clear value-add, or where firms initially join but down-select after some number of years, putting Institute sustainability at risk.

As discussed in question 2, the size of a new Institute should follow from its technology focus and the degree to which existing infrastructure for that technology area at the given level of maturity is present within the U.S. or would need to be substantially established. Furthermore, as discussed in question 1, NIST should look to existing Institutes where possible for enhancement via CHIPS funding rather than standing up the maximum allowed number of new Institutes.

8. *What membership and participation structure for a Manufacturing USA semiconductor institute would be most effective for ensuring participation by industry, academia, and other critical stakeholders, particularly with respect to financial and intellectual property obligations, access, and licensing? Based on your knowledge of current Manufacturing USA institute practices, are the needs of potential semiconductor institutes different than for other institutes?*

There are many unique facets of the semiconductor industry that could, in turn, demand unique considerations from an Institute compared to those Institutes that serve other sectors. Enormous capital equipment costs, expensive and continually evolving digital tools, a highly sophisticated global supply chain with many specialized participants, and the degree of existing R&D support from industry are all important factors not necessarily present in many advanced industries.[1] There are many focus areas for a potential Institute that would need to take into account all or most of these aforementioned topics.

The high level of industry funding for R&D means that there is already a mature ecosystem for technology development within the industry that should be supplemented and not supplanted with CHIPS funding for Manufacturing USA Institutes. As such, government should not solely fund specific R&D programs but rather should use seed funding that creates and builds an Institute that can operate with industry co-funding, as required by statute. Only if industry is a co-funding source at the right level will the Institute be aligned with and serve industry needs. Looking at other institutes, 50% of revenue for effective existing collaborations comes from government.[2]

With regard to governance and IP issues, a few key points:

- IP rights, governance, revenue models, and operations should be structured similarly to other institutes.
- IP rights have to be balanced to allow industry members to profit from them while also recognizing the value creation by academia.
    - IP models' balance must include different options, perhaps some IP will be made publicly available while other IP will offer a high competitive advantage for sponsoring member(s) and therefore should provide some terms of exclusivity or protection.
- The organization structure should be informed by and implement known best practices and learnings from other Institutes
- Must be industry-led with strong academic partners, alongside government oversight, and be highly inclusive of the broad semiconductor ecosystem
- Because of the high degree of breackthorugh technology innovation required for success in the industry, academics play a more critical role in the industry as compared to other industries. Because of this, CHIPS related Manufacturing USA Institutes will require inter-academic collaboration.

[1] See "Strengthening the Global Semiconductor Supply Chain in an Uncertain Era", BCG & SIA, April 2021; https://www.semiconductors.org/wp-content/uploads/2021/05/BCG-x-SIA-Strengthening-the-Global-Semiconductor-Value-Chain-April-2021_1.pdf

[2] See "Manufacturing USA: Advanced Manufacturing Institutes and Network (R46703)," October 2022, https://crsreports.congress.gov/product/details?prodcode=R46703

- Manufacturing continues to add more advanced materials into the manufacturing process, including materials that can be reproduced but are not always well understood scientifically. Additionally, new materials need to be assessed for environmental health and safety which needs to be part of the research process.

Strategies for Driving Co-Investment and Engagement

9. *The authorizing statute for Manufacturing USA requires at least an equal non-federal co-investment in Manufacturing USA institutes to match the federal investment. From your perspective, what are the most significant considerations to garner support for the required co-investment for a Manufacturing USA semiconductor institute? What is the anticipated impact of the new Investment Tax Credit (ITC) for industry established in the CHIPS Act on the level of investment in the new Manufacturing USA semiconductor institute(s), in facilities, including for manufacturing equipment and construction? How might a Manufacturing USA semiconductor institute be set up to best leverage the Investment Tax Credit?*

Commerce can best encourage co-investment for a Manufacturing USA semiconductor institute by allowing participating companies to have flexibility in the type of support to be provided, including the use of in-kind contributions. Companies seeking to support the institute are more likely to support the effort by being able to provide different types of support at their discretion, including in-kind contributions of people or equipment, in addition to cash contributions. The new Advanced Manufacturing Investment Credit enacted as part of the CHIPS and Science Act of 2022 ("CHIPS Act") is a vital complement to the semiconductor grant program also enacted as part of the CHIPS Act. These critical federal incentives indirectly support additional funds for important semiconductor research and innovation that aligns well with the mission of the Institute.

With regard to the applicability of the Advanced Manufacturing Investment Credit included as part of the CHIPS and Science Act, implementing regulations may clarify or determine whether the ITC could assist in attracting contributions to the institute. The credit is applicable to a "qualified investment" in an "advanced manufacturing facility." IRC § 48D(b)(1). A qualified investment is defined as certain "qualified property" that includes tangible property either constructed by the taxpayer or "acquired by the taxpayer if the original use of such property commences with the taxpayer" and is "integral to the operation of the advanced manufacturing facility." § 48D(b)(2). An advanced manufacturing facility means a facility "for which the primary purpose is the manufacturing of semiconductors or semiconductor manufacturing equipment." § 48D(b)(3).

The interpretation of each of these terms will likely impact whether the credit will help drive contributions to the Manufacturing USA semiconductor institute. In addition, the institute itself must have the "manufacturing of semiconductors or semiconductor manufacturing equipment" as its "primary purpose." This could include research activities, but in any case the manufacturing of semiconductors or equipment must be the primary purpose. Ultimately, implementing regulations from the Treasury Department will significantly shape whether the tax credit is relevant for Manufacturing USA Institutes.

10. *For the required non-federal co-investment for a Manufacturing USA semiconductor institute, with respect to the different types of co-investment (e.g., cash, equipment donations, facilities access, etc.), are there factors unique to the semiconductor industry*

that would impact how the co-investment could be structured to best support the institute?

It would depend significantly on the nature of the Institute itself and which technology areas are the intended focus of any given institute. The enormous capital equipment costs associated with certain manufacturing processes (e.g. advanced node logic, advanced packaging, and memory) do not necessarily apply for some other Manufacturing USA semiconductor Institutes. For those examples of Institutes that would support more cross-cutting efforts like general semiconductor manufacturing automation, access to fabrication facilities may be the best form of co-investment. A further point of consideration is that there is separation in the industry between foundries that manufacture and design houses that do not own equipment. The Institute will be able to bring resources from design together with facilities from foundries to push technological advances that would otherwise not be possible. As part of co-investment contributions, foundries will be able to provide access to cutting edge fabs, advanced packaging, and manufacturing facilities. Design firms could contribute both software and mindshare to work with those at facilities to collaborate and develop ideas not possible in their individual silos. It may also be advantageous for an institute for partner with materials and equipment suppliers for access to process development labs to provide specialized process steps or access to emerging materials at smaller scales as a co-investment strategy

11. *What arrangements for co-investment proportions and types could help a Manufacturing USA semiconductor institute sustain operations in the absence of continued federal support?*

Co-investment from the semiconductor industry is already happening, at scale. Many top companies in the industry are contributing millions of R&D dollars to research and development programs at universities, including those programs currently run by SRC. This is made possible by the alignment of the Institute's mission and the needs of the industry. If the Institute is formed and not aligned with industry needs, it will not be sustainable.

Co-investment from universities is also already occurring in the ecosystem. Continued investment by government and industry will send the message to universities that their contributions in both ideas and co-investment are valued. This will help ensure continued support for the Institute by top academic researchers.

12. *A Manufacturing USA semiconductor institute should support domestic competitiveness. How should relationships with foreign entities be structured or constrained to support domestic manufacturing priorities while maximizing the opportunities to leverage international expertise and resources? In what circumstances should the Manufacturing USA Semiconductor institutes and NIST as the federal sponsor, consider membership requests from foreign-owned businesses?*

Over the past several decades, the semiconductor industry has changed the way we work, play, and connect while enabling trillions of dollars in economic prosperity and transforming national security. During these decades, however, the industry fractured into specialized supply chain blocks. While each of these specialized blocks has different economic and risk characteristics, together they deliver a system that has enabled massive industrial growth and yields a global supply chain that is highly optimized to convert silicon ingots into integrated circuits that meet and drive consumers' needs.

Although this regional growth enabled global economic growth, it has resulted in a growing economic dependence on other regions, and therefore risk, as well as national security risks. Mitigating supply chain risk does not require the U.S. to become a leader in all aspects of the supply chain blocks (functional technologies, design, and applications) through the entire innovation pipeline from research to manufacturing for all products markets. Instead, the U.S. should aim to become a top global leader in innovation for all blocks of the supply chain needed for 2030 and beyond, and then strategically select which manufacturing blocks to lead directly and which to collaborate on with international partners.

While partnership and collaboration with foreign-owned business is essential in semiconductor R&D, the U.S. taxpayer-funded Manufacturing USA Institutes should primarily focus on U.S. owned companies, in alignment with the goals of the CHIPS Act to reinvigorate U.S. R&D leadership. Other highly effective research organizations, including SRC, work well with international companies and facilitate cooperation; the Manufacturing USA Institutes, however, have a unique charter that should prioritize U.S.-based companies.

13. *How should a new Manufacturing USA semiconductor institute engage other existing Manufacturing USA institutes (https://www.manufacturingusa.com/ institutes), including those awarded funds for work related to semiconductor manufacturing, and other manufacturing related programs and networks such as the Manufacturing Extension Partnership (https://www.nist.gov/ mep) and the U.S. Department of Energy's Next Generation Power Electronics National Manufacturing Innovation Institute ("Power America")?*

There are several ways for a new Institute to engage other existing Manufacturing USA Institutes. All are funded with taxpayer dollars, and all should be looking to further the US agenda.

A great starting place would be for the Institute to share both operational and intellectual property models. Sharing best practices with other Institutes could be key to successfully operating the Institute before and after government funding. Leveraging knowledge among Institutes is a very low cost/high benefit activity.

Institutes should also share facilities resources where applicable. The semiconductor industry has advanced manufacturing capabilities that could be made available to other Institutes. We also recommend that some of the new dollars that go to existing manufacturing institutes be dedicated to collaboration with the MAPT MMUSAI.

Joint projects can and should be worked on. This new Institute would have common interests with Power America, AIM Photonics, and possibly other existing Institutes. By pooling funds from different Institutes, additional leverage can be obtained to make research dollars go further on both sides. Also, different viewpoints and ideas can be created by bringing together Institutes which may have some similar interests but look at those interests from different viewpoints and motivators.

14. *How should a Manufacturing USA semiconductor institute interact with State and local economic development entities?*

The Institute(s) should leverage existing regional semiconductor manufacturing ecosystems that have been driven by strong state and local economic development support. For example, the southwest, northwest, and central regions of the US have excellent resources and talent that could contribute to the mission of new Manufacturing USA Institutes through a working relationship with State and local economic entities. These states have very strong research universities, national labs, and research professionals which could contribute to both the industry and the Institutes. State and local economic entities could assist in furthering workforce development, infrastructure, land use, and economic strategies aligned with the goals of the CHIPS Act. Several states have recently initiated efforts which could be complementary with and helpful to the success of Manufacturing USA Institutes including efforts in Arizona, Indiana, New York, Ohio, Oregon, and Texas. .

15. *How should a Manufacturing USA semiconductor institute coordinate with and inform standards development bodies on the need to modify existing or develop new standards as a result of this initiative?*

Although part of the value of government/industry partnerships is the possibility to convene a critical mass of technology stakeholders to help develop open standards for integration, these standards should be led by industry needs in most cases, with government serving primarily as a convening authority. It makes sense to include voices from mission agencies (DOD, NASA, DOE, etc.) for those standards that are especially relevant to their mission and funding. For these areas especially, direction may be determined by both industry and government needs. This is the value of a Manufacturing USA Institute with inroads to U.S. mission agencies. In all cases, Institutes should partner with organizations like IEEE and the Joint Electron Device Engineering Council for the development of standards.

Education and Workforce Development

16. *How could a Manufacturing USA semiconductor institute best support advanced manufacturing workforce development and/or awareness at all educational levels (e.g., for K-12 through post-graduate students)?*

17. *How could a Manufacturing USA semiconductor institute best engage and leverage the diversity of educational and vocational training organizations (e.g., universities, community colleges, trade schools, etc.)?*
18. *How could a Manufacturing USA semiconductor institute best ensure that advanced manufacturing workforce development activities address the industry's priorities?*

19. *How could a Manufacturing USA semiconductor institute best leverage and complement existing education and workforce development programs?*

20. *What measures could assess Manufacturing USA semiconductor institute performance and impact on education and workforce development?*

21. *How might a Manufacturing USA semiconductor institute integrate research and development activities and education to best prepare the current and future workforce?*

22. *How could a Manufacturing USA semiconductor institute help build a steady pipeline of skilled workers? What knowledge, skills and abilities will future workers need, and are there workers with those skills currently employed in other sectors?*

23. *How could a Manufacturing USA semiconductor institute broaden the talent base (i.e., embrace diversity, equity, inclusion, and accessibility; reach women and minority communities, engage non-traditional workers, engage separating service members, veterans, and families) to modernize the workforce?*

24. *What type of education and workforce development activities should a Manufacturing USA semiconductor institute support (e.g., curricula, online education, hybrid, entrepreneurship opportunities, credentialing, regional development, train the trainers, internships/apprenticeship, learning labs, etc.) and why?*

Consolidated workforce response:

The ability for the Institutes to help address U.S. workforce training needs is especially critical. A recent White House agency announcement fact sheet describes a variety of beneficial actions the executive branch plans to take to address the increasing U.S. STEM demands. Within this broad set of activities,[3] the Institutes could promote a range of programs to expand the supply of the U.S. semiconductor R&D workforce:

- **Invest in U.S. STEM education**. The Institutes could support curriculum development and standardization at the high school, undergraduate, and graduate levels to expand the pipeline of workers with prerequisite STEM skills.[4] For example, prerequisite math classes should start in middle school so students can complete the more rigorous math classes in high school in order to enroll and complete a STEM postsecondary/higher education degree. Additionally, building the awareness of what microelectronics enables and importance to daily lives can motivate or excite students to learn more and move into this area. Starting at the middle-school level is not too early. These students "see" the apps on their phones but they may be unaware of the exciting underlying microelectronics technology which power their devices.
- **Attract STEM graduates to the industry**. The Institutes could educate students about career opportunities in the semiconductor industry through apprenticeships, internships, "earn while you learn", and mentorship programs.[4] By offering a path for graduate students and postdocs to also commercialize their own startups and IP, the Institutes could offer further incentive for U.S. students to remain in the industry and foreign students to remain in the U.S.[5]
- **Promote flexible work authorization**. The Institutes could promote flexible work authorization or extended education programs – like optional practical training periods - that enable foreign nationals to work in the US if they graduate from U.S. universities with skills critical to industry.[4]

[3] https://www.whitehouse.gov/briefing-room/statements-releases/2022/01/21/fact-sheet-biden-harris-administration-actions-to-attract-stem-talent-and-strengthen-our-economy-and-competitiveness/
[4] See SIA Research Report; "American Semiconductor Research: Leadership Through Innovation", October 2022
[5] See "ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA", FEBRUARY 2022, 13

Several programs have been successful in attracting new workers into the semiconductor workforce. As one example, the Department of Defense's Scalable Asymmetric Lifecycle Engagement (SCALE) program is a public-private-academic partnership that supports university engineering departments and matches participating students with private sector employers. This program has seen early success in building a STEM workforce in each of its five technical verticals at both the undergraduate and graduate levels. Another example is Maricopa Community College's Associate in Applied Science (AAS) in Electronics Technology program, which offers a model for how more local educational programs could be shaped.[6]
SIA recommends that Manufacturing USA Institutes make it an essential and urgent priority opportunity to partner with local community colleges, high schools, and minority serving institutions to train and develop talent to cater to skills required in semiconductor manufacturing. Veteran engagement and skill bridge programs provide excellent opporutinites to develop and expand the talent pool and help veterans transition into civilian workforce.

One SIA member offers online resources for students, educators, researchers, and entrepreneurs in developing their skills in the semiconductor industry. It helps train and certify students on intelligent system design technologies, learning computational software skills for transitions into industry, and these are complemented by scholarship and internship opportunities that directly support the pipeline of new and diverse STEM talent.[7]

Additionally, one major U.S. semiconductor firm runs a $4.5 million multi-year program with 6 historically black colleges and universities (HBCUs) to increase the pipeline of African Americans in engineering fields. This program has increased black enrollment in these fields by as much as 55 percent in some partner universities. The same firm also runs a $5 million partnership with a local public school district to encourage underrepresented youth to pursue further education in STEM fields. Over four years, underrepresented minority students enrolled in computer science classes in the district increased by 17 times, and girls enrolled in computer science increased by 33 times.

Lastly, FIRST Robotics is a hands-on learning program that prepares K-12 students for jobs in engineering and other STEM fields. It organizes students into teams that design, program, and build robots, and these teams compete on local and national levels.[8]

These types of long-term investments have a proven track record and a scalable model of such programs across the U.S. should be considered to attract more underrepresented minorities to the semiconductor sector.

Other examples of successful program templates can be found internationally, which the Manufacturing USA Institutes could borrow from. The Taiwan Semiconductor Research Institute (TSRI) is the product of the consolidation of two national labs in Taiwan, and it serves as a powerful model for what services a workforce collaboration between government and industry ought to offer. The TSRI offers a comprehensive range of training programs, comprising a series of courses ranging from device fabrication to circuit systems, and TSRI partners with universities that offer courses on fundamental theories to complement the practical lessons offered by the institute. Beyond education, TSRI facilitates critical hands-on opportunities by

[6] https://www.maricopa.edu/degrees-certificates/science-technology-engineering-mathematics/electronics-technology-3220-aas
[7] https://www.cadence.com/en_US/home/company/cadence-academic-network.html
[8] https://www.firstinspires.org/robotics/frc

providing advanced process equipment and a complete measurement and design environment that students and trainees can use. Because the training courses include both introductory and applied/laboratory lessons, learners are able to complete their own chip designs, which teaches them the critical tacit skills needed to add value in the industry at the highest levels.[9]

These are all examples of efforts that have been undertaken in some form or another to address the workforce gap. The greatest impact for the Manufacturing USA Institutes can be realized by partnering with and expanding these efforts where appropriate, or looking to these past efforts for inspiration when considering new initiatives. NIST should consider the regions that are expected to experience the greatest growing demand for semiconductor talent based on the planned locations of new capacity.

Metrics and Success

25. *What metrics could be used to best evaluate the performance of a Manufacturing USA semiconductor institute in accelerating innovation, and any associated impacts on economic competitiveness and national security? Are there sector-specific metrics for an institute in the semiconductor technology space?*

26. *What type of metrics could be used to best evaluate the performance and impact of a Manufacturing USA semiconductor institute on education and workforce development in support of U.S. competitiveness?*

27. *What type of metrics could be used to best evaluate the performance and impact of a Manufacturing USA semiconductor institute in establishing and expanding the U.S. semiconductor manufacturing ecosystem?*

28. *What constitutes a successful first year for a Manufacturing USA semiconductor institute? What forms of support, and from which partners, are needed to ensure a successful first year?*

Consolidated Metrics and Success Response:

Evaluating metrics and impacts is very challenging without first identifying those specific areas that new Manufacturing USA Institutes should target, which is in turn difficult without a determination of the broad CHIPS Act R&D structure (NSTC, NAPMP). That said, the most comprehensive way to determine metrics for success is to identify technology and Institute roadmaps based on expert stakeholder input from industry, academia, and government. In some cases, enormous effort has already been dedicated to establishing technology roadmaps, such as IEEE heterogeneous integration roadmap.[10] In other cases, an Institute may need to convene stakeholder workshops and roundtables to identify appropriate roadmaps and evaluation criteria. For workforce, it may be valuable to use NAEP scores for domestic metrics and TIMMS for global competitiveness metrucs. Domestically, each state has their own set of

[9] https://www.tsri.org.tw/en/training.html

[10] https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html

tests for evaluating performance so NAEP would be a better benchmark for longitudinal measurement on the impact on education.