SEMICONDUCTOR INDUSTRY ASSOCIATION

Comments of the
Semiconductor Industry Association (SIA)
To the
Internal Revenue Service
On the
Advanced Manufacturing Investment Credit, Notice of Proposed Rulemaking
REG-120653-22
88 Fed. Reg. 17451 (March 23, 2023)

May 22, 2023

The Semiconductor Industry Association (SIA)[1] appreciates the opportunity to provide comments on the Internal Revenue Service (IRS) and Treasury Department (Treasury) notice of proposed rulemaking[2] ("Proposed Regulations") related to the Advanced Manufacturing Investment Credit enacted in the CHIPS and Science Act of 2022 ("CHIPS Act" or "the Act")[3] and set forth in section 48D of the Internal Revenue Code.[4]

The complex, technologically advanced process of designing and manufacturing semiconductors and semiconductor manufacturing equipment requires high levels of investment in people, facilities, and equipment due to the complexity of the technology and the rigorous and exacting standards needed for construction, equipment, and infrastructure. In light of the critical role of semiconductors to the U.S. economy and national security, Congress enacted the CHIPS Act to provide robust incentives for the expansion of the semiconductor ecosystem in the United States in order to make the U.S. competitive with other countries. These incentives consisted of two separate but complementary programs: (1) a program of direct manufacturing incentives under the authority of the Department of Commerce and (2) an "advanced manufacturing investment credit" codified under section 48D.

SIA commends the Treasury Department in adopting a holistic approach to section 48D in the Proposed Regulations so as to provide taxpayers with a credit for a wide range of investments necessary to manufacture semiconductors and semiconductor manufacturing equipment. We provide the following comments on the proposed rules and, as necessary, recommend clarifications to provide taxpayers with certainty in determining their eligibility to claim the credit. SIA also includes in Appendix A a "Brief Overview of Semiconductor Manufacturing and Equipment Manufacturing" to provide Treasury with additional information in support of our comments.

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[1] The Semiconductor Industry Association (SIA) is the voice of the semiconductor industry, one of America's top export industries and a key driver of America's economic strength, national security, and global competitiveness. SIA represents 99% of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. chip firms. Through this coalition, SIA seeks to strengthen leadership of semiconductor manufacturing, design, and research by working with Congress, the Administration, and key industry stakeholders around the world to encourage policies that fuel innovation, propel business, and drive international competition. Learn more at www.semiconductors.org.
[2] Advanced Manufacturing Investment Credit, Internal Revenue Service, Treasury, 88 Fed. Reg. 17451 (proposed March 23, 2023) (to be codified at 26 CFR 1)
[3] Pub. L. No.117-167 (2022).
[4] All "section" or "§" references are to the Internal Revenue Code of 1986, as amended, and the regulations promulgated thereunder.

SEMICONDUCTOR INDUSTRY ASSOCIATION

I. Definitions. (§ 1.48D-2)

A. "Semiconductor"

In response to Treasury's request that taxpayers provide comments regarding the proposed definition of "semiconductor," SIA respectfully requests the term be modified so as to include mono or polycrystalline solid substances—such as polysilicon, ingot/boules, wafers, and similar materials—with electronic properties manufactured specifically for the purpose of semiconductor manufacturing (§ 1.48D-2(k)). Generally, Treasury should provide a more expansive definition of "semiconductor" to include a substance, system, or device because the production of semiconductors necessarily requires the production of semiconductor grade polysilicon, semiconductor silicon wafers, compound semiconductors, such as silicon carbide and gallium nitride, or other types of boules, the singulation of the boules into individual wafers, the polishing of the wafers, and frequently the deposition of epi layers on the wafer. These highly complex manufacturing processes are integral to the semiconductor manufacturing process and comprise the first step in manufacturing a semiconductor device. Put another way, polysilicon and similar materials are the "semiconductor" material in the semiconductor chip. The crystal structure of the boule or wafer forms the base of the finished wafer, which is manipulated through successive depositions, implants, etching, and other steps to create the chip.

The inclusion of polysilicon, boules, wafers and similar materials with electronic properties manufactured specifically for the purpose of semiconductor manufacturing would be consistent with existing Treasury guidance pertaining to the tax credit for the manufacture of solar panels. Specifically, with respect to the section 48C clean energy manufacturing tax credit, Treasury guidance confirms that certified projects involving the production of such materials as polysilicon, ingots, and wafers were determined to be eligible for the credit.[5] Notably, the solar panel manufacturing process is comparable to the production process for semiconductors, which supports the conclusion that the above-referenced materials similarly be included in the definition of "semiconductor," and therefore qualify for the section 48D credit.

In addition, while the proposed definition of "semiconductor" is broad and appears to encompass systems for quantum computing, such systems are not expressly referenced in the Proposed Regulations. SIA urges Treasury to consider revising the definition to clarify this point by adding "quantum electronics" to the illustrative list of devices and systems.

B. "Semiconductor Manufacturing" and "Semiconductor Manufacturing Processes," including "Packaging"

Treasury should revise the definition of "semiconductor manufacturing" and "semiconductor manufacturing processes" (§ 1.48D-2(l)) to include all stages of "packaging" (i.e., "back-end" manufacturing), consistent with the definition in the proposed regulations of the Department of

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[5] § 48C(c)(1)(A)(i)(I). The White House Fact Sheet announcing awardees of the clean energy manufacturing tax credit under section 48C includes a list of certified applications and certified projects by the Internal Revenue Service, which includes projects for polysilicon, ingots, wafers, etc. *See, e.g.*, Hemlock Semiconductor Corp., SolarWorld Industries America, Inc., Sumco Phoenix and Wacker Polysilicon North America LLC. See https://obamawhitehouse.archives.gov/the-press-office/fact-sheet-23-billion-new-clean-energy-manufacturing-tax-credits and https://obamawhitehouse.archives.gov/sites/default/files/100108-48c-selection-final-with_projects.xls.

Commerce ("Proposed Commerce Regulations"), which is incorporated by reference in the Proposed Regulations (§ 1.48D-2(l)(1)).[6] In particular, Treasury should clarify that the definition of semiconductor "packaging" also includes the process of "assembly" and "test" of semiconductors (§ 1.48D-2(l)(2)(i)).

Once hundreds of chips are fabricated on a wafer, the next step is to separate the individual chips, test them, and assemble them in a "package" to prepare it for mounting onto a circuit board and incorporation into a finished assembly or product. The assembly, test, and packaging (ATP) stage is commonly known within the industry as "back-end" manufacturing. Each of these steps are integral parts of the manufacturing process as manufacturers must assemble, test, and package an individual device to ensure the product meets customer specifications. We respectfully request that Treasury expand the examples listed in the Proposed Regulations (§ 1.48D–3(f)) to confirm the inclusion of back-end manufacturing equipment (i.e., that related to assembly, testing, and packaging) to ensure consistency and transparency of what is considered "semiconductor manufacturing" and the types of property eligible under section 48D.

Additionally, "semiconductor manufacturing" should include in its definition compound semiconductor formation processes such as crystal growth, wafer singulation, and epitaxy and the production and purification of polysilicon and silicon carbide, as well as monosilicon ingots, boules, and wafers manufactured from semiconductive substances (such as polysilicon and silicon carbide). This addition aligns with SIA's proposed definition of "semiconductor" to include mono or polycrystalline solid substances with electronic properties manufactured specifically for the purpose of semiconductor manufacturing.

C. "Semiconductor Manufacturing Equipment"

The Proposed Regulations generally adopt a broad definition of "semiconductor manufacturing equipment" (§ 1.48D-2(m)) and list a number of examples of such equipment (§1.48D-2(m)(1) through (7)). SIA supports this definition and requests it be further clarified. The list of examples in the definition should be framed as a non-exclusive one. Accordingly, the sentence immediately preceding § 1.48D-2(m)(1) should be modified to read as follows: "Specific examples of semiconductor manufacturing equipment and subsystems that enable semiconductor manufacturing equipment include*, but are not limited to* . . . ." SIA requests that Treasury expand the list to provide taxpayers with more certainty in claiming the credit. A proposed list of qualified property to be included can be found in Appendix A.

Furthermore, the list of property in § 1.48D-2(m) appears to reference only finished equipment and does not address the term "subsystems." Subsystems included in semiconductor equipment manufacturing, such as lenses and photomasks, are both necessary and primarily applicable to the production of semiconductor chips. These subsystems are customized, with months-long production timelines, and of the highest durability in that these lenses and photomasks must be able to withstand billions of laser pulses. These lenses are directly responsible for the lasers used in photolithography, metrology, and inspection. The lenses and

[6] Preventing the Improper Use of CHIPS Act Funding, CHIPS Program Office, National Institute of Standards and Technology, Department of Commerce, 88 Fed. Reg. 17439 (Proposed Reg. March 23, 2023) (to be codified at 15 CFR 231) at § 231.118.

mirrors are produced from glass boules, are shaped, polished, and coated to customer specifications, and are housed in mechanical assemblies in order to locate and align the beams directed through them. These manufacturing processes are generally not automated and instead require highly skilled workers to produce them through meticulous precision and testing. Depending on the final piece of manufacturing equipment, these sub-assemblies are built into larger subsystems that are integrated into a larger "box" (i.e., the finished piece of equipment) along with other subsystems. Perhaps most importantly, such subsystems are produced only for use in semiconductor manufacturing equipment made specifically to manufacture semiconductor chips.

Accordingly, we recommend that Treasury include in its definition of subsystem 1) specialty glass lenses (e.g., high-purity fused silica or ultra-low expansion glass) and photomasks used by photolithography machines to etch chip designs, 2) lenses and mirrors, like those made of calcium fluoride or high-purity fused silica, that enable the laser light source for wafer flatness inspection equipment (i.e., "laser optics"), 3) lens assemblies for wafer defect inspection following wafer printing (i.e., "precision optics"), and 4) light sources or other major components of photolithography systems.

D. Partnership Basis Allocations and "Applicable Taxpayer" in the Partnership Context

In North America, semiconductor companies may enter into partnerships with third parties (e.g., financial institutions) to engage in large scale semiconductor manufacturing projects and help optimize their investments in new chip manufacturing. Often, these arrangements are structured as partnerships under which only one partner is intended to take advantage of the section 48D credit (i.e., claim 100 percent of the credit), notwithstanding the fact that the partnership itself is funded by the contributing partners in some other ratio (e.g., 50%/50%). The Proposed Regulations specify that for purposes of the apportionment of basis between partners, rules under Treas. Reg. § 1.46-3(f) will apply. Those rules generally require that partners' shares of the partnership's basis in qualified property will be determined in accordance with the ratio in which the partners divide the general profits of a partnership.[7] Thus, in the instance of a 50/50 joint venture, the partners would each share 50 percent of the basis in the partnership's qualified property, consistent with the partners' 50/50 split of the partnership's income. Of course, this would frustrate the intent of the partners in the partnership that only one partner claim the full section 48D credit, as the basis allocation would limit the extent to which the credit could be claimed to 50 percent.

To allow unrelated parties entering into joint ventures to structure the section 48D credit benefit as they wish, SIA proposes that § 1.46-3(f) be modified to permit the allocation of the partnership's basis in qualified property to partner(s) independent of the ratio in which the partnership's general profits are allocated amongst the partners. In no circumstances would the partnership's basis in qualified property be allocated to a partner who would not otherwise be entitled to claim the credit if it were to undertake the same activities it undertook within the joint venture on its own. Further, SIA recommends that the partner(s) to whom the basis is allocated – and who therefore actually claim the section 48D credit – be treated as the applicable

[7] Treas. Reg. § 1.46-3(f)(2)(i).

taxpayer for purposes of the recapture rules proposed under § 1.50a-2 (rather than the partnership), because activities undertaken outside the context of the joint venture by an unrelated partner should not operate to trigger recapture of the section 48D credit claimed by another partner who is party to the joint venture.

II. Qualified property. (§ 1.48D-3)

A. Calculating basis in a dual-use facility

The statute specifies that qualified property "includes any building or its structural components which otherwise satisfy the requirements" of the Act and excludes "a building or portion of a building used for offices, administrative services, or other functions unrelated to manufacturing."[8] This provision underscores Congress's intent to broadly define qualified property to include any building or its structural components needed for semiconductor fabrication or equipment manufacturing, with the limited exception of accompanying offices.

In excluding portions of a building used for offices, Treasury should distinguish true back-office type functions unrelated to manufacturing (e.g., payroll, accounting, etc.) from office space supporting the operations of the manufacturing facility (e.g., direct supervision, management, support services, and procurement). Accordingly, Treasury should deem the basis attributable to reasonably identifiable portions of a building, including office space, as well as research and storage facilities mentioned in § 1.48D-3(f)(2), that are integral to manufacturing semiconductors or semiconductor manufacturing equipment to be treated as qualified property and therefore eligible for the credit. Office space properly characterized as qualified property might include (but is not limited to), for example, offices housing functions such as:

- Facilities teams to maintain the clean room systems integral to semiconductor manufacturing;
- Environmental Health and Safety ("EHS") teams to ensure the safety of both the people and the environment during the manufacturing process;
- IT infrastructure/data processing directly related to the manufacturing process, such as systems in support of automated processes, equipment and process monitoring, and operational systems; and
- Facilities for workforce training centers directly related to manufacturing semiconductors or semiconductor manufacturing equipment.

Further, the Proposed Regulations treat offices devoted solely to administrative functions as outside the scope of the credit. In the case of a dual-use facility, SIA respectfully requests additional guidance on how to apportion basis between portions of the facility that are and are not considered "qualified property" (§ 1.48D-3(c)(2)). For any portion of a building and its structural components that is excluded from the term "tangible depreciable property" pursuant to § 1.48D-3(c)(2), Treasury should allow taxpayers to utilize any reasonable method to apportion the basis and offer examples of methods that are considered reasonable to determine the apportionment of the basis attributable to the excluded property.

[8] § 48D(b)(2)(B)(ii).

For example, one method Treasury should consider is the apportionment of the basis in buildings and structural components based upon square footage at the time of placement into service. Another method Treasury should consider is an actual allocation of costs of building and structural components among the portion utilized for manufacturing actives and the portion utilized for other functions unrelated to manufacturing. Treasury could also provide a safe harbor similar to that included in the UNICAP regulations addressing dual function storage.[9] In that context, the regulations establish a de minimis 90-10 rule providing that if 90 percent or more of the costs of a facility are attributable to the on-site storage function, the entire storage facility is deemed to be an on-site storage facility. Similarly, if 90 percent or more of the costs of an advanced manufacturing facility were determined to be integral to the manufacture of semiconductors or semiconductor manufacturing equipment, the entire building would be qualified property for purposes of section 48D.

Finally, while the Proposed Regulations do exclude property related to administrative functions from the qualified property definition, they do allow for property related to cybersecurity operations to be eligible for the credit. We support Treasury's treatment of cybersecurity operations, due to the highly sensitive nature of semiconductor manufacturing.

B. Request for a transition rule for calculating basis after date of enactment

Section 107(f) of the Act provides that, in general, the advanced manufacturing investment credit "shall apply to property placed in service after December 31, 2022." The language goes on to state that the credit shall apply to "any property the construction of which begins prior to January 1, 2023, only to the extent of the basis thereof attributable to the construction, reconstruction, or erection after the date of enactment of this Act." Taxpayers will benefit from some flexibility on this point because of difficulties associated with tracking and allocating costs around a date occurring in the middle of a month—that is, the date of enactment on August 9, 2022.

SIA therefore requests that the final regulations provide a transition rule where taxpayers may use any reasonable method to allocate costs to periods after August 9, 2022. Existing Treasury regulations frequently allow taxpayers to use "any reasonable method" to make determinations for which a taxpayer may not have the ability or data. Relevant examples relating to the investment tax credit include those for rehabilitation expenditures under 1.48-11(b)(5)(i), where any reasonable method may be used to allocate property that services different portions of a building between the qualified rehabilitated portions of a building, or 1.48-12(c)(1), where a taxpayer may use any reasonable method to allocate qualified rehabilitation expenditures between an original building and an enlargement.

[9] *See* Treas. Reg. § 263A-3(c)(5)(iii)(C).

C. "Original use" (§ 1.48D-3(e))

Semiconductor manufacturing and packaging facilities routinely fabricate and package chips using second-hand, refurbished equipment. Accordingly, SIA requests that Treasury revise the Proposed Regulations' definition of "original use" such that it includes acquired property that is reconditioned or rebuilt by another taxpayer, without a requirement that the acquiring taxpayer subject such property to further reconditioning or rebuilding before it may claim the section 48D credit. Such a result is appropriate where the property (e.g., lithography systems) has a long useful life. One manufacturer of semiconductor equipment estimates that 96% of its machines ever produced currently remain in service, and that manufacturer has been producing the equipment for nearly 40 years.[10] Due to the quality and continued value of the equipment, coupled with the high cost of acquiring such systems, using reconditioned or rebuilt equipment is a common practice in the industry, and such property should be covered under 48D.

D. Clarify certain circumstances surrounding leased property (§ 1.48D-3(e))

Leasing is a form of financing that is critical to the semiconductor manufacturing industry given the high capital expenditure requirements, and it is unclear how the Proposed Regulations would apply to the taxpayer's use of leased property that the taxpayer reconditions or rebuilds. Former section 48(d) provided rules with respect to leased property and taxpayers currently rely on section 50(d)(5) and Treas. Reg. § 1.48-4 to make lease elections for eligible investment tax credit property. Consistent with the statutory authority under section 50(d)(5),[11] Treasury should provide that Treas. Reg. § 1.48-4 also applies for purposes of section 48D and should specify the requirements for a lessor to elect to treat the lessee of leased property as the owner of such property for purposes of section 48D.

In the absence of specific rules in line with the section 48 guidance outlined above, Treasury should at least consider clarifying that a taxpayer's lease of an advanced manufacturing facility that the taxpayer subsequently reconditions, rebuilds, or purchases constitutes "original use" of the property for purposes of section 48D. As a part of this additional guidance, SIA proposes including illustrative examples, including those addressing the issue of which taxpayer – the lessee, the lessor, or the lessee who purchases the previously leased facility and subsequently reconditions and/or rebuilds it – is eligible to claim the credit under these circumstances.

E. Further clarification of qualified property integral to the operation of a manufacturing facility (§ 1.48D-3(f))

Section 48D(b)(2)(iv) provides that qualified property must be "integral to the operation of the advanced manufacturing facility." SIA generally supports Treasury's proposed coverage of the types of investments in qualified property that are integral to the operation of an advanced

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[10] Tarasov, K. (2022, March 23). ASML is the only company making the $200 million machines needed to print every advanced microchip. Here's an inside look. CNBC. https://www.cnbc.com/2022/03/23/inside-asml-the-company-advanced-chipmakers-use-for-euv-lithography.html

[11] Providing that, for purposes of subchapter A, part IV, subpart E of the code (which includes section 48D), rules similar to those under section 48 (as in effect prior to the enactment of the Revenue Reconciliation Act of 1990) regarding the treatment of leased property shall apply.

manufacturing facility.[12] As a general matter, the Proposed Regulations properly encompass the full range of investments in buildings, infrastructure, and equipment for the equipping, construction, expansion, or modernization of a semiconductor fabrication facility ("fab") or a facility producing semiconductor manufacturing equipment. SIA believes the Proposed Regulations are construed broadly to include site preparation, construction of the manufacturing facility, equipment, automation, test tools, accompanying infrastructure—like piping and storage systems, purification, pollution, lighting, and temperature control systems—and similar property integral to the operation of an advanced manufacturing facility.

In the Proposed Regulations, Treasury provides what appears to be a non-exhaustive list of qualified property considered to be eligible for the section 48D credit. To increase taxpayer certainty in claiming the credit, Treasury should clarify that the list is illustrative and does not encompass the full universe of property that may be deemed to be integral to the operation of the facility. Accordingly, the sentence immediately preceding § 1.48D-3(f)(1) should be modified to read as follows: "Specific examples of property which normally would be integral to the operation of the advanced manufacturing facility of an eligible taxpayer *include, but are not limited to . . . .*"

SIA respectfully requests that Treasury also expand the non-exhaustive list of qualified property included in the final regulations to include the types of property listed in Appendix A (note, however, that such list does not constitute an exhaustive list of all property that could be considered qualified property under section 48D). For example, we request qualified property include emulation tools and photomasks/reticles. These additional examples, like others in the Appendix A, are "tangible depreciable property that is integral to the operation of an advanced manufacturing facility," are used "in connection" with manufacturing, and are "essential to the completeness of the manufacturing operation." We note that the Proposed Regulations already include "reticle handlers," "mask manufacturing equipment," and "inspection and metrology equipment" among the examples of qualified property, but these terms do not encompass emulation tools or photomasks/reticles. We note below the special functions of each of the above-enumerated types of property in an effort to distinguish them from the property already included in the Proposed Regulations and illustrate how they rise to the level of qualified property properly deemed eligible for the section 48D credit.

- Emulation hardware is a type of electronic hardware used for testing and debugging digital systems or electronic designs. It allows engineers to verify and validate the functionality of a design before the actual hardware is produced. One of the key benefits of using emulation hardware is that it allows engineers to identify and fix problems that may be inherent to the design, which can help to reduce the overall development time and cost.

- During the lithography process, the patterned mask is placed over the substrate, and a beam of light is directed through it to transfer the pattern onto the substrate. The light

[12] Property is integral to the operation of manufacturing semiconductors or semiconductor manufacturing equipment if such property is used directly in the manufacturing operation, is essential to the completeness of the manufacturing operation, and is not transformed in any material way as a result of the manufacturing operation" *Prop. Treas. Reg.* § 1.48D-3(f).

passing through the transparent areas of the mask will expose the photoresist on the substrate, creating a pattern that can then be etched into the substrate. The process is fundamental to the creation of the circuitry that provides for the functionality and performance of an individual chip.

Each of these items are integral to the manufacturing process, and explicitly including these inputs to the manufacturing process as qualified property is wholly consistent with congressional intent of incentivizing domestic investments in semiconductor manufacturing.

Additionally, SIA requests that Treasury clarify that the definition of "transformed" in the Proposed Regulation (§ 1.48D-3(f)) does not include the normal degradation of components of semiconductor manufacturing equipment.

F. Clarify the eligibility of certain research or storage facilities

SIA supports the Proposed Regulations' inclusion of research facilities, such as those used in pre-pilot production or prototyping, in the definition of qualified property insofar as they are deemed "integral to the operation of the advanced manufacturing facility under section 48D(b)(2)(A)(iv)."[13] Many companies have production facilities—fabs, ATP facilities, semiconductor manufacturing equipment facilities, and design—and research and development (R&D) operations, which may or may not share buildings, infrastructure, and equipment, to ensure new design and/or product technology is developed and transitioned into a prototype or pilot manufacturing setting. This part of the process is to ensure a particular technology can be scaled for commercial production. Due to the rapidly advancing technologies used in the semiconductor industry, R&D facilities are critical to certain manufacturers to optimize the time to market for new technologies and are an integral component to semiconductor manufacturing regardless of whether they are co-located with a manufacturing facility.

However, the Proposed Regulations further note that research facilities do not qualify if they do not manufacture any type of semiconductor or semiconductor manufacturing equipment.[14] This restriction goes beyond the statutory language, which only excludes buildings, or portions thereof, that are "unrelated" to manufacturing. SIA recommends that Treasury should treat these types of facilities as advanced manufacturing facilities, notwithstanding potential co-location within a single structure.

As currently drafted, the Proposed Regulations exclude certain research facilities which are integral to the operation of semiconductor manufacturing, used "in connection" with manufacturing, and are essential to "the completeness of the manufacturing operation." We believe the Proposed Regulations exclude certain research facilities that should otherwise qualify for the credit and request the last sentence of § 1.48D-3(f)(2) be changed to read "a research facility that is not used in connection with the manufacture of any type of semiconductors, as provided in § 1.48D-2(k), or semiconductor manufacturing equipment, as provided in § 1.48D-2(m), does not qualify."

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[13] *See Prop. Treas. Reg.* § 1.48D-3(f)(2).
[14] *Id.*

In regard to storage facilities, the Proposed Regulations list examples to include "mineral, chemical, and gas storage tanks, including high pressure cylinders or specially designed tanks and drums,"[15] but do not explicitly include semiconductor equipment parts storage used in regular maintenance. Such storage for equipment replacement, repair, and cleaning, and other storage used to maintain advanced manufacturing facilities should be included so as to fully encompass the scope of storage facilities integral to the operation of semiconductor manufacturing and semiconductor equipment manufacturing.

III. Advanced manufacturing facility of an eligible taxpayer. (§ 1.48D-4)

A. Strike, or define, the term "finished" as applied to "semiconductor" and "semiconductor manufacturing equipment"

There are several references throughout the Proposed Regulations to the term "finished semiconductor" and "finished semiconductor manufacturing equipment" *(see, e.g.*, Prop. Treas. Reg. § 1.48D-3(f), -4(b) and -4(c)), but the term is not defined. SIA recommends Treasury strike the word "finished" as applied to "semiconductor" and "semiconductor manufacturing equipment" in the Proposed Regulations everywhere it appears so as to avoid inadvertently disqualifying otherwise qualifying expenditures, property, or facilities. Without such adjustment, the term may exclude output from a broad range of semiconductor fabrication and semiconductor manufacturing equipment facilities.

For example, assume a semiconductor fab produces a patterned wafer consisting of hundreds of individual semiconductor devices, which comprises a significant portion of the overall value of the entire manufacturing process. Arguably, the patterned wafer is not a "finished semiconductor." The fabricated wafer remains an interim product that awaits additional processing before it is ready to be incorporated into a larger component (e.g., a circuit board) or a final product (e.g., a cell phone, a laptop, etc.). In another common scenario, consider a complex piece of semiconductor manufacturing equipment. The equipment may be shipped from a semiconductor manufacturing equipment facility to another semiconductor manufacturing equipment facility for additional assembly to take place at a semiconductor fab prior to the equipment being fully operational. In this example, a lithography tool may be shipped with the primary light source and top module intact and then undergo additional assembly or upgrades at another manufacturing facility. Chipmakers do not purchase these distinct components produced by the semiconductor manufacturing equipment facility; they purchase the complete lithography system that is later assembled.

It is evident that both Congress and Treasury intended for the fabrication of semiconductor wafers and production of semiconductor manufacturing equipment to be eligible for the section 48D credit, but the reference to "finished" semiconductors and manufacturing equipment injects uncertainty as to what property qualifies for the section 48D credit. Accordingly, SIA recommends that the term "finished" as applied to "semiconductor" and "semiconductor manufacturing equipment" be stricken from the final regulations.

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[15] *Prop. Treas. Reg.* § 1.48D-3(f)(2).

As an alternative and at minimum, Treasury should expand § 1.48D-2 to include a definition of the term "finished" to better reflect the states of a semiconductor or the various types of semiconductor manufacturing equipment when such property leaves a manufacturing facility. It is critical that this new term is clarified to include various forms of output from semiconductor manufacturing facilities (i.e., semiconductor wafers that have been produced as output from the fabrication process) and semiconductor equipment manufacturing facilities. Treasury should also explicitly state that "back-end" and "front-end" functions do not need to occur within the same facility. In other words, "finished semiconductor" should be defined to include both wafers from a front-end fabrication facility as well as modules and components from a back-end assembly, test, and packaging facility.

B. "Primary purpose" threshold test

In the Proposed Regulations, Treasury states that the "primary purpose" of a facility will be determined on a facts and circumstances basis, whereby taxpayers must demonstrate that a facility is designed to make semiconductors or "products consisting of specialized equipment that can only be used for semiconductor manufacturing." Treasury lists two examples, both of which use a 75 percent threshold to illustrate circumstances where a facility may satisfy the test (§ 1.48D-4(c)). We request that Treasury consider implementing a safe harbor under which the facility's primary purpose will be considered to be the manufacture of semiconductors or semiconductor manufacturing equipment if more than 50 percent of its functions are devoted to such activities. This change would help to accommodate dual-use facilities that may manufacture other types of equipment not exclusive to the semiconductor industry. Additionally, SIA suggests that Treasury provide examples of what is not considered a facility meeting the "primary purpose" test, especially for facilities that do not meet the 75 percent threshold.

C. "No primary purpose"

As stated above, the definition of the term "semiconductor" should be revised to include polysilicon, boules, wafers, and similar materials with electronic properties manufactured specifically for the purpose of semiconductor manufacturing (§ 1.48D-2(k)). If this expanded definition is adopted, we recommend striking the words "grows" and "grow wafers" in Prop. Treas. Reg. § 1.48D-4(c)(2).

IV. Beginning of construction. (§ 1.48D-5)

The Proposed Regulations specify that the section 48D credit applies to an advanced manufacturing facility the construction of which begins prior to December 31, 2026 (§ 1.48D-5(a)). SIA generally supports this approach adopted by Treasury, but we request further clarification and guidance with respect to certain provisions under this section.

A. "Single advanced manufacturing facility project" (§1.48D-5(a)(3))

The beginning of construction rules provided in the Proposed Regulations have largely been borrowed from the body of guidance for beginning construction that is applicable to energy tax credits. However, because of the nature and composition of energy projects and semiconductor manufacturing projects are different, it is recommended that the Proposed Regulations include some clarifications in the wording that are necessary to make the language clearly applicable to

the totality of advanced manufacturing projects. In particular, language in Prop. Treas. Reg. § 1.48D-5(a)(3) describes what constitutes a single advanced manufacturing facility project and lists included items considered integral to the operation of a "single advanced manufacturing facility project." It is recommended that the proposed language in Prop. Treas. Reg. §1.48D-5(a)(3) be amended to include "tooling equipment (such as for deposition, etching, etc.)" within the list that includes "…clean rooms, chemical delivery systems, chemical storage facilities, temperature control systems, and robotic handling systems…."

B. Additional examples of onsite and offsite activities deemed to meet the physical work test (§ 1.48D-5(c))

Under existing guidance[16] and the Proposed Regulations, there are two methods for establishing when construction begins: the Physical Work Test and the Five Percent Safe Harbor, with a continuity requirement underpinning both methods. SIA generally supports the guidance with respect to determining when construction has begun and the clarifications around estimating costs for purposes of satisfying the Five Percent Safe Harbor. However, to provide taxpayers with further certainty, we request Treasury provide additional guidance with respect to onsite and offsite activities specific to the manufacturing of semiconductors and semiconductor manufacturing equipment that would satisfy the Physical Work Test.[17]

C. "Continuous efforts" test (§ 1.48D-5(e)(3))

The construction of advanced manufacturing facilities is a complex process, and the lead time for construction is much longer than that for many other types of manufacturing facilities. Moreover, market volatility and the cyclical nature of semiconductors, paired with the extraordinarily high cost of building a new advanced manufacturing facility, are all factors that may delay construction in a market downturn. Congressional intent in enacting the advanced manufacturing investment credit was to create a robust and long-lived semiconductor ecosystem, and to afford taxpayers ample opportunity to avail themselves of the credit for ongoing projects.[18] We commend Treasury in recognizing the unique nature of constructing a semiconductor manufacturing facility and providing a 10-year safe harbor for that purpose (§ 1.48D-5(e)(6)). However, for some facilities, like those built in sequential phases to encompass multiple fabs in a single project, construction may extend beyond 10 years.

In the case where the 10-year safe harbor is not met, we request Treasury provide examples of the facts and circumstances that would support the conclusion that the taxpayer satisfied the

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[16] *See* Internal Revenue Service, Notice 2018-59: "Beginning of Construction for the Investment Tax Credit Under Section 48," *available at* https://www.irs.gov/pub/irs-drop/n-18-59.pdf (hereinafter Notice 2018-59).

[17] *See, e.g.,* Notice 2016-31, Notice 2018-59, Notice 2020-12 (providing examples of "physical work of a significant nature" for purposes of the physical work test that are specific to various technologies and industries covered by tax credits under §§ 45, 45Q, and 48).

[18] Office of U.S. Senator Charles E. Schumer (2023, February 24). *Schumer pushes feds for swift implementation of investment tax credit created in his CHIPS & Science Act to get shovels in the ground and boost semiconductor industry jobs in upstate NY, available at* https://www.schumer.senate.gov/newsroom/press-releases/schumer-pushes-feds-for-swift-implementation-of-investment-tax-credit-created-in-his-chips-and-science-act-to-get-shovels-in-the-ground-and-boost-semiconductor-industry-jobs-in-upstate-ny.

"continuous efforts" test. For example, paying or incurring additional amounts included in the total cost of the property is considered indicative of such continuous efforts. [19]

C. Ensure that the continuity safe harbor is not less than the prescribed 10-year period

The semiconductor manufacturing industry employs almost exclusively equipment that is not widely manufactured and is ordered several years in advance of beginning substantial on-site construction of a manufacturing facility. Site preparation for semiconductor manufacturing may also be considered physical work of a significant nature under established beginning of construction principles even though on-site construction has not begun in earnest. In the semiconductor industry, long-lead procurement of custom equipment and project-specific on-site work early in the development cycle is a common occurrence.

Given the long-lead procurement of custom equipment and early project-specific site work inherent in the development of semiconductor manufacturing facilities, taxpayers constructing such facilities may trigger the "beginning of construction" earlier in the development cycle thereby "starting the clock" for the ten-year safe harbor during which a taxpayer must place the qualified property in service. The structure of a continuity safe harbor that measures from the beginning of construction, in the context of semiconductor manufacturing, creates a perverse incentive to intentionally delay the beginning of construction date to as late in 2026 as possible so as to more closely align the time that construction actually begins (as opposed to site preparation activities) to the beginning of the tolling of the 10-year safe harbor period.

We recommend addressing these issues by creating a simple and bright-line approach of a fixed date for the continuity safe harbor, and recommend utilizing December 31, 2036, which is 10 years after the beginning of construction deadline. There is precedent for taking this approach, as a similar rule was imposed in the regulatory guidance amplifying the renewables production tax credit.[20] Given that the tax credit under section 48D does not have a long-term qualification period and does not contain a phase-down period, it would be appropriate to provide taxpayers with the certainty afforded by a fixed placement in service deadline with respect to the continuity safe harbor.

D. Support for excusable disruptions to continuous construction (§ 1.48D-5(e)(4))

SIA supports the inclusion of provisions allowing for excusable delays that could potentially impact a taxpayer's continuous efforts tests (§ 1.48D-5(e)(4)). We appreciate Treasury's acknowledgement that certain disruptions to construction may inevitably occur in large-scale projects, and such unforeseen events should not operate to deprive a taxpayer of eligibility for the credit for otherwise ongoing, continuous construction. The proposal properly enumerates several non-exclusive examples of excusable disruptions, ranging from weather and natural disasters to delays in permitting approvals, supply chain disruptions, and financing.

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[19] *Prop. Treas. Reg.* § .48D-5(e)(3)(i).
[20] *See* Notice 2013-60, Section 3.02 and Notice 2015-25 Section 3.

V. Recapture of the advanced manufacturing investment credit in the case of certain expansions. (§ 1.50-2)

Section 107(b) of the CHIPS Act provides for the "recapture" of the advanced manufacturing tax credit for an "applicable transaction" during the 10-year period from the placement into service of property eligible for the credit. The Act defines an "applicable transaction" as "any significant transaction . . . involving the material expansion of semiconductor manufacturing capacity" by the taxpayer in China or a foreign country of concern (IRC 50(a)(3)(D)(i)). The Act provides for an exception for "a transaction which primarily involves the expansion of manufacturing capacity for legacy semiconductors" (IRC 50(a)(3)(D)(ii)). Consistent with the direction by Congress for Treasury to define "applicable transaction" subject to recapture "in coordination with the Secretary of Commerce and the Secretary of Defense," the proposed regulations by Treasury implementing these provisions largely parallel the Proposed Commerce Regulations implementing the CHIPS grant "clawback" provisions.[21]

The recapture in the Proposed Regulations (as with the "guardrails" in the Proposed Commerce Regulations) were enacted in recognition of the complex role of China in the global semiconductor ecosystem, the global supply chain and economy as a whole, and the national security landscape. In the semiconductor industry, China is simultaneously (1) an enormous market, comprising approximately one-third of all chip sales from U.S. companies, (2) a major part of the semiconductor supply chain, with about 20 percent of front-end capacity and nearly 40 percent of back-end capacity, and (3) a major competitor, with a growing industry in all segments of semiconductor research, design, fabrication, packaging, equipment, and materials. Given this multifaceted and complex relationship, Congress constructed a balanced statutory framework to work alongside other policies (e.g., export controls) to ensure that, as the U.S. provides incentives to attract investments in new semiconductor fabrication and equipment manufacturing facilities to strengthen the economy and make the domestic supply chain more resilient, it would restrict certain new investments in China to address national security concerns and supply chain dependence. The "recapture" provision established under the advanced manufacturing investment credit curtails tax credit recipients' ability to increase advanced semiconductor manufacturing capacity in China, while simultaneously allowing for the continued operation of existing legacy facilities or the construction of new or expanded legacy facilities predominantly serving the China market. Congress sought to allow the continued operation of legacy facilities in China to avoid causing disruption to the global chip supply chain. In executing this complex framework in the Proposed Regulations, however, we believe Treasury, in certain instances, did not strike the right balance. Some aspects of the Proposed Regulations jeopardize the continued commercial viability of existing legacy operations in China of companies based in the U.S. and allied countries, which could potentially result in supply chain disruptions in the global semiconductor industry and harm the commercial competitiveness of the semiconductor industry.

[21] Proposed 15 C.F.R. Part 231, 88 Fed. Reg. 17439 (March 23, 2023).

A. SIA supports the overall consistency and alignment between Commerce and Treasury proposals but additional alignment is still required

SIA supports the overall consistency between the Proposed Regulations and the Proposed Commerce Regulations, as reflected in the recapture and guardrails provisions, respectively. SIA has filed extensive comments with respect to the "guardrails" provisions under the Proposed Commerce Regulations. We attach these comments (see Appendix B) and incorporate them by reference into this letter. We respectfully request that Treasury revise the recapture proposal to be consistent with SIA's proposed revisions to the Proposed Commerce Regulations addressing the guardrails. An aligned set of restrictions on transactions in foreign countries of concern, where applicable, is needed to facilitate compliance with these requirements and reduce administrative burdens, particularly for companies who are both direct funding recipients under the CHIPS incentive program and eligible for the advanced manufacturing investment credit under section 48D. Alignment of the two regulatory requirements will also provide for the more efficient use of government resources.

Further, these revisions are needed to better advance the intent of Congress in enacting the guardrails/recapture requirements: that being, as the CHIPS incentives are being deployed to strengthen the domestic ecosystem, these incentives, while still allowing for the continued commercial viability of existing legacy facilities in countries of concern, should not be used to subsidize investments in foreign countries of concern. Certain provisions in the proposal should be revised to accommodate the continuation of operations at existing legacy facilities in countries of concern needed to ensure they remain operational and competitive. In other words, while both the Treasury "recapture" and Commerce "expansion clawback" rules should operate to restrict new construction or significant expansions of manufacturing capacity in foreign countries of concern, as well as any increase in manufacturing capacity of advanced semiconductors, these prohibitions should avoid disrupting ordinary business activities (e.g., maintenance, the replacement or upgrade of equipment, etc. that do not involve new construction or the physical expansion of a facility) at existing legacy facilities, especially given the length of time of the advanced manufacturing investment credit recapture period.

B. Request consistency/alignment in reporting and documentation requirements, audit procedures, and related matters

The Proposed Regulations consider recordkeeping and reporting requirements to ensure compliance with the law, with a particular view toward ensuring that the IRS is informed of taxpayers' engagement in "applicable transactions." The Proposed Regulations further state that Treasury and the IRS will coordinate with the secretaries of Commerce and Defense to determine whether a transaction is an applicable transaction, which is defined to be consistent with the Proposed Commerce Regulations.

The Proposed Regulations include a request for comments on taxpayers' ability to comply with such requirements and what procedures should be utilized in determining if a taxpayer engages in an applicable transaction. For taxpayers receiving direct funding under the Commerce program, due consideration should be given to the burden taxpayers will bear in reporting to both Treasury and Commerce on what may be the same information regarding a planned applicable transaction. SIA respectfully requests that Treasury and Commerce streamline the

reporting and recordkeeping requirements so as to not be duplicative and overly burdensome on the taxpayer participating in both incentive programs enacted under the CHIPS Act.

Specifically, SIA encourages Treasury and Commerce to consider adopting guidelines similar to those of the Executive Order: Reorganization Plan No. 4 of 1978, whereby the Secretary of Labor transferred certain enforcement authority for overlapping regulations to the Secretary of the Treasury. While both agencies still had an important role in oversight, the Executive Order delegated responsibility for administering the various overlapping rules to a single agency. This action would be equally appropriate in instances where companies are receiving both a grant and claiming the tax credit and therefore subject to the same restrictions in many cases. As the Proposed Regulations are intended to be "harmonized with existing oversight and restrictions on these types of transactions imposed by the Export Administration Regulations (15 CFR parts 730 through 744)," streamlining the review of the recapture of advanced manufacturing tax credit with that of the expansion clawback under the Department of Commerce would be an efficient outcome.

Additionally, the IRS could include a form or attachment to annual tax returns with basic questions for the IRS to ascertain whether an eligible taxpayer may have engaged in an applicable transaction during the taxable year.

C. Establishing to the "Satisfaction of the Commissioner" that a prohibited transaction has been abandoned

SIA recommends Treasury publish standards for establishing what is considered to be to the "Satisfaction of the Commissioner" that an applicable transaction has been abandoned and set standards for notifying a taxpayer that an applicable transaction has been entered into. The regulations or other guidance should set forth with specificity the information required by the IRS contained within its "determination and notice," which should include a description of the geographic location of the activity, the involved parties, and the nature of the activity. Further guidance should also include guidance as to how a taxpayer may demonstrate cessation or abandonment of a project. Those actions could include proof of cancelled contracts, the withdrawal or cancellation of requisite work permits, and the issuance of a public statement that expressly cancels the applicable transaction.

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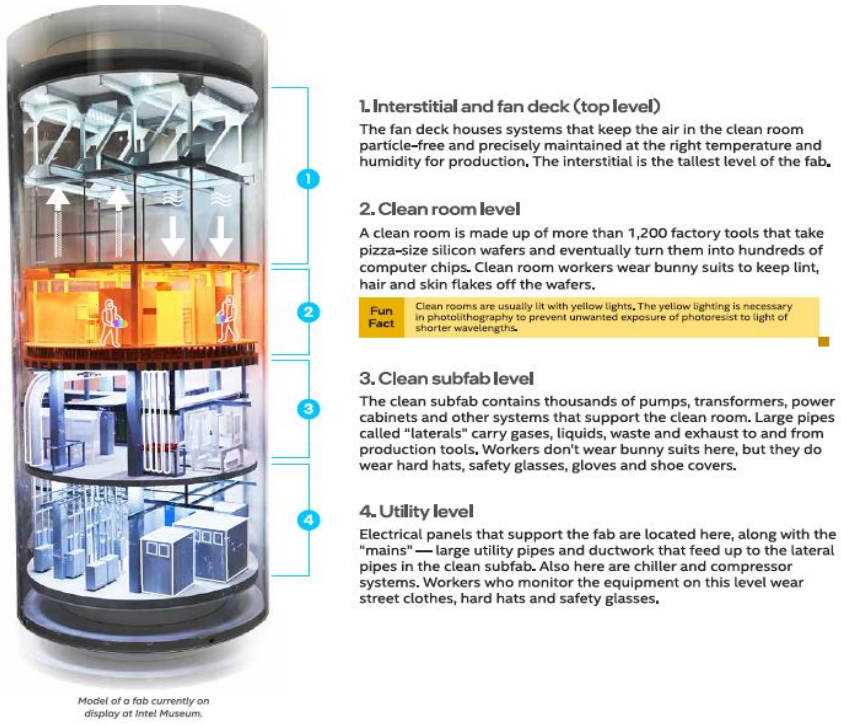
SIA appreciates the opportunity to comment on this proposal and we look forward to continuing to work with Treasury in the development and implementation of these rules.

SEMICONDUCTOR INDUSTRY ASSOCIATION

Appendix A
Brief Overview of
Semiconductor Manufacturing and Equipment Manufacturing

1. Semiconductor Fabrication

Construction of a semiconductor fabrication facility ("fab") requires qualified labor and is capital intensive. The cost of a fab can range from $1-20 billion depending on the type and scale of the project. Construction of a fab requires highly skilled workers to build and install support systems and structures to deliver high purity gases, ultra-pure water, and state of the art air recirculation systems. A cross-section of the inside of a fab is shown below.[22]



Model of a fab currently on display at Intel Museum.

Each level of the fab plays a unique role in the manufacturing process and each level requires specialized equipment, piping, clean-air, and waste management systems. Each of these systems and support structures must meet stringent requirements based on the International Standards Organization (ISO). For example, a fab clean room must meet ISO 14644-3 (updated in 2019), which applies to clean rooms and associated controlled environments that are defined as providing control of contamination to levels appropriate for accomplishing contamination-sensitive activities. Products and processes that benefit from the control of airborne contamination include the aerospace, microelectronics, pharmaceuticals, medical devices, healthcare, and food industries.[23] To meet these standards, companies spend millions of dollars to install systems and support structures that adhere to ISO requirements.

Each level of a fab is integral to the overall operation of the facility. The following is a brief overview of these parts of the fab and how they and how the systems and structures installed in each level ensure an efficient manufacturing process.[24]

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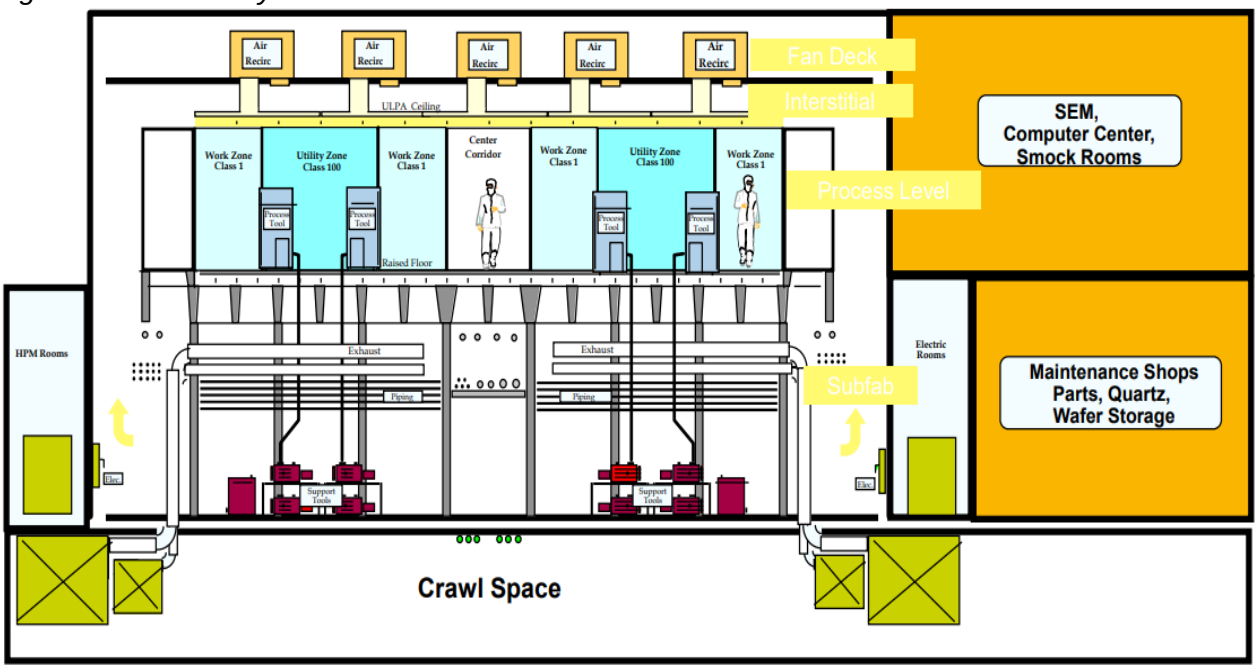
[22] https://www.intel.com/content/dam/www/central-libraries/us/en/documents/what-does-it-take-to-build-a-fab.pdf
[23] https://www.iso.org/obp/ui/#iso:std:iso:14644:-3:ed-2:v2:en
[24] For an overview of the steps in the fabrication process, see White House supply chain report at 35-36.

Fab Layout

Generally, a fab has different levels that work in coordination to filter high purity gases, chemicals, and particle free clean air. These processes occur in specialized piping systems (laterals), pumps, and abatements systems to provide purified water and waste management. These systems are necessary to support the infrastructure and equipment, like lithography machines, that produce semiconductors. Throughout the fab, specialized technicians of varying skill levels monitor these systems to ensure the smooth operation of the fab.

Figure 1: Detailed layout of Fab



Source: NXP

Level 1: Interstitial and fan deck

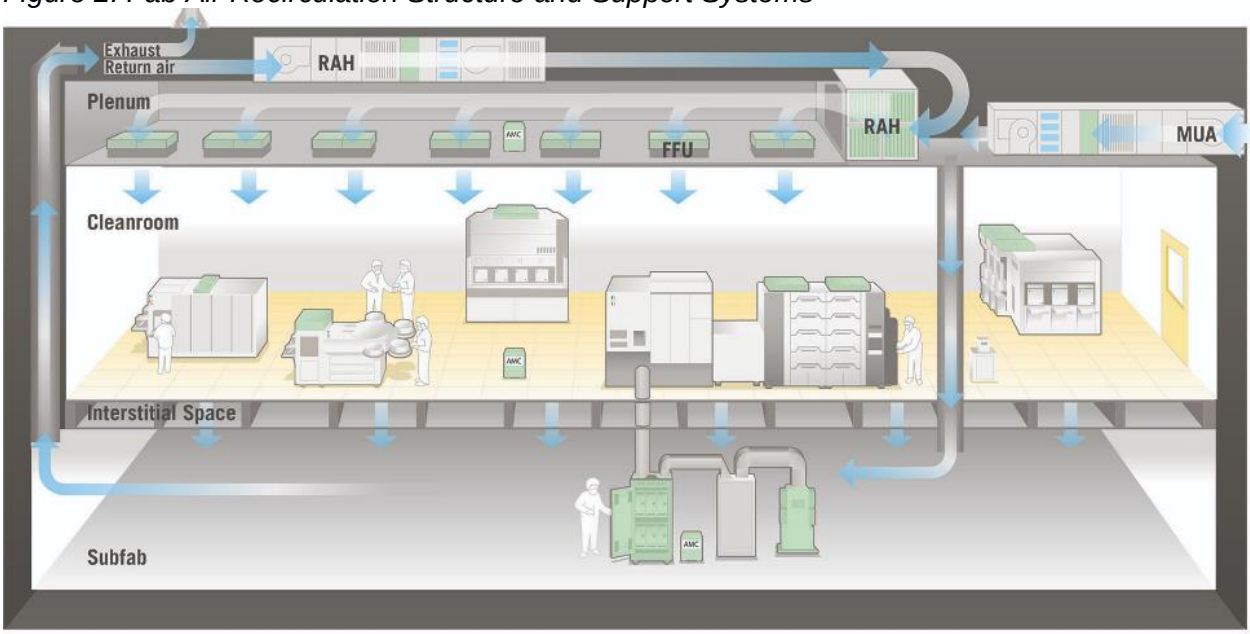
In this level of the fab, specialized recirculating air handler (RAH) units recondition the air and send it back down into the ceiling of the clean room. Clean air is supplied to each bay through a grid of high efficiency particulate air (HEPA) filters. The air flows straight down through the floor, before returning up through the floor. At the fan deck level, RAH units recondition the air and send it back down into the ceiling plenums.

In the cleanest areas, this cycle repeats 600 times per hour, and the entire ceiling is HEPA filters.[25] Many chemicals used in the clean room may be corrosive, so exhaust ducts from fume hoods and wet process areas are Teflon-coated, welded stainless steel. Other processes employ on-site scrubbers to treat exhaust, which then can be sent into standard ducts with vacuum pump exhaust. Exhaust removes about 10% of the air from each cycle, which is

[25] http://www.matthewfickett.com/pdf/Poster%20-%20Cleanroom.pdf

replaced with fresh air. Hazardous process material (HPM) exhausts are often incompatible with other exhausts and must be ducted directly to a dedicated roof fan.

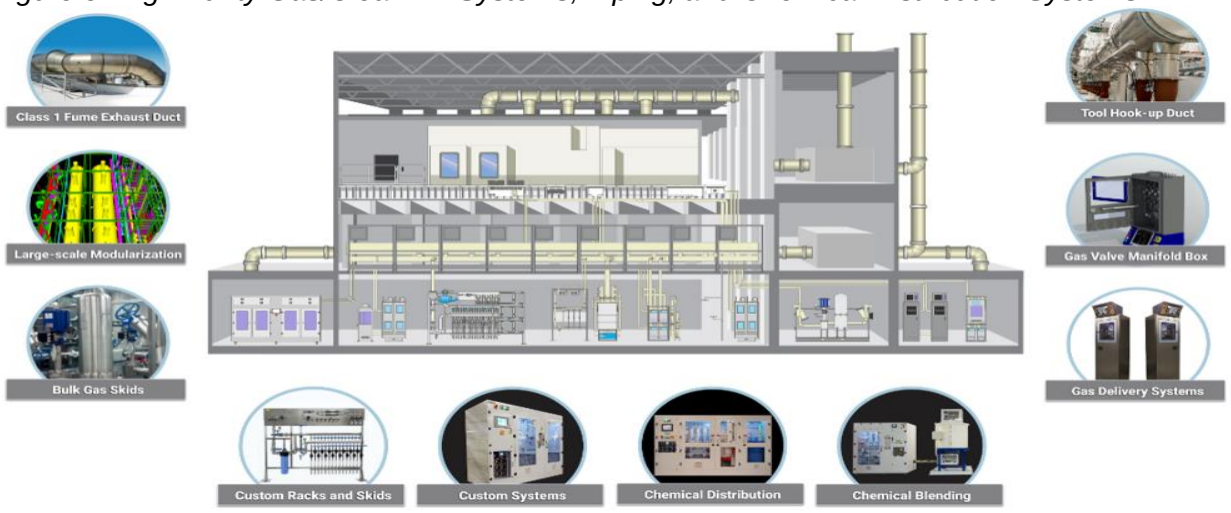
Figure 2: Fab Air Recirculation Structure and Support Systems



Source: Valin

Figure 3 illustrates the many different exhaust, pipe, pump, and chemical distribution systems that are necessary for the functioning of a fab. Each system is highly specialized and must meet exacting standards before installation. For example, when working on a hook up in a facility, expertise in fluid mechanics is needed to ensure proper flow and pressure.

Figure 3: High Purity Gas/Clean Air Systems, Piping, and Chemical Distribution Systems

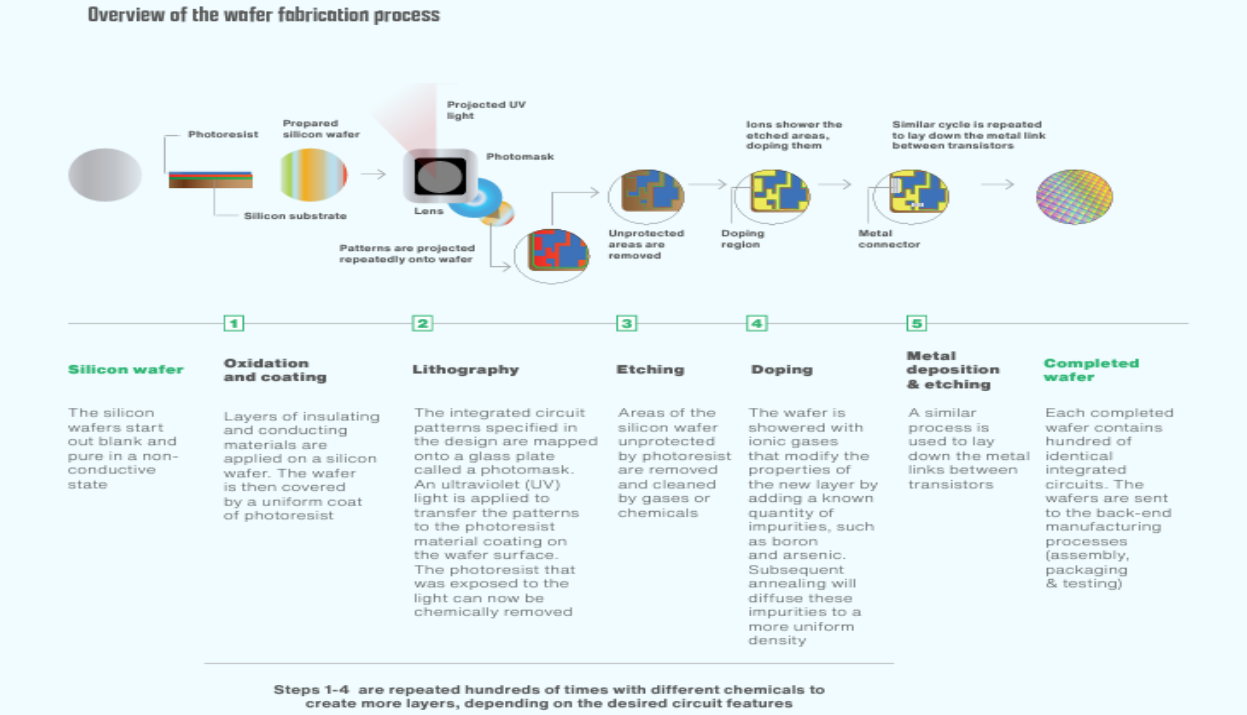


Source: Critical Process Systems Group

Level 2: Clean room

The clean room is where the front-end wafer manufacturing cycle occurs. A clean room may contain over 1000 machine tools to turn wafers to semiconductors. Figure 4 breaks down the manufacturing process and the role of each piece of equipment, and Figure 5 displays those pieces of equipment within a typical clean room. Each tool is essential to the manufacturing process and may cost in the tens of millions of dollars.[26] The equipment includes wet process tools, lithography equipment, analytical tools, deposition and etch tools, and stockers. Throughout the process, clean air is recirculated while sub fab level equipment continuously circulates chemical gas and ultra-pure water while simultaneously pumping out chemical waste.

Figure 4: Manufacturing Process



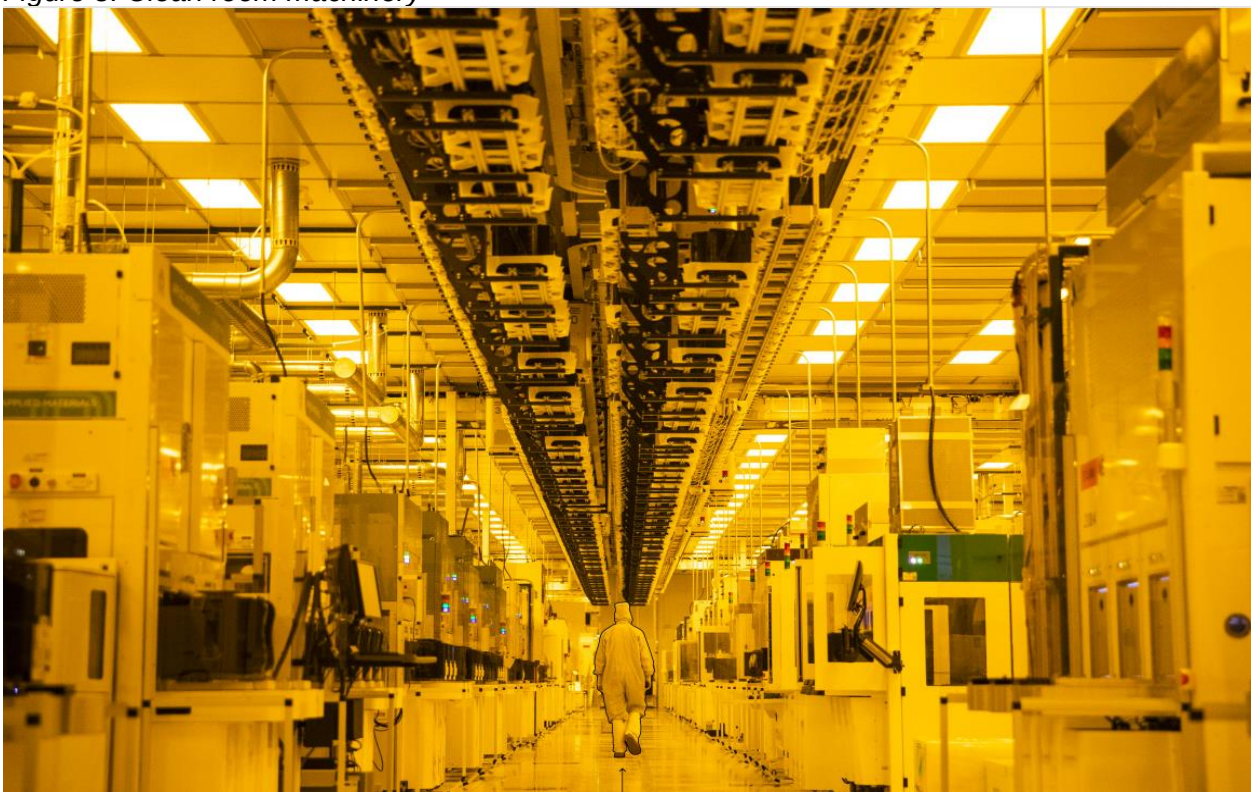
Source: SIA/BCG Strengthening the Global Semiconductor Supply Chain in an Uncertain Era

Each process tool provides essential functions. Chemical Mechanical Polishing (CMP) valve actuation, and its impact on the integrity of the slurry is important as this will allow the system to have a more stable removal rate across a longer period. For the etching process, the precision of chemical dosing over time is critical to ensure that the chemistry used on the wafer will have the right composition, and as a result the right action. For cleaning, focusing on dispensing the exact quantity of liquid on the wafer is necessary to remove every targeted chemistry.

[26] https://www.valin.com/semiconductor-manufacturing-process-products-and-applicability

The clean room itself is finished in non-particulating material such as epoxy paint, glass, or metal. The clean room area is arranged in bays connected by a clean corridor (shown above in Figure 1), where only gowned personnel are permitted. Between the bays, chases (picture shown to the right)[27] are used to access equipment. A common chase provides a location for less-clean storage or equipment. All windows and lights into the clean room are covered with a protective UV-blocking film, to avoid exposing photoresist chemicals. To minimize vibration, the structure under the clean room must be exceptionally durable, and isolated from the rest of the building. All HVAC systems, including the ceiling plenums, are suspended from above to avoid vibrating the floor.

Figure 5: Clean room machinery



Source: Bloomberg

Protection of the clean room from contaminants is so extreme that specialized lighting systems are required. Besides dust particles from workers, lighting systems can be a source of contaminants. To eliminate these contaminants, clean rooms are typically lit with yellow or

[27] https://mitnano.mit.edu/facility-updates/cleanroom-organization-bay-vs-chase

amber lighting that meet strict standards before installation.[28] Some requirements for lighting in the medical-pharmaceutical industry also apply to semiconductor manufacturing.

Level 3: Clean room sub fab

Within the sub fab, pumps and abatement systems extract and neutralize process exhaust, deposits, and other waste materials from the clean room. Without these specialized systems, the repetitive process of producing a die on a wafer will overtime see the process degrade in performance and ultimately shutdown manufacturing. On the sub fab chemical distribution systems, expertise in fluid mechanics, chemical compatibility (instant and over time), mechanical and pneumatic compatibility (for the pump) is needed.

In addition, the level includes ultrapure water systems, uninterruptible power supply (UPS) system, oil-free air compressors, boilers, high purity nitrogen, process cooling water and various waste systems to support the manufacturing processes.[29] The picture to the right shows a glimpse of the scale of just some of the piping, ducts, exhaust, and waste management systems that occupy this level of the fab. Figure 5 above details the specialized systems, structure, and machinery that are required to maintain a clean and efficient manufacturing process. Furthermore, systems like vacuum pumps and gas abatement systems, are designed to reliably serve the production process 24 hours a day and seven days a week.

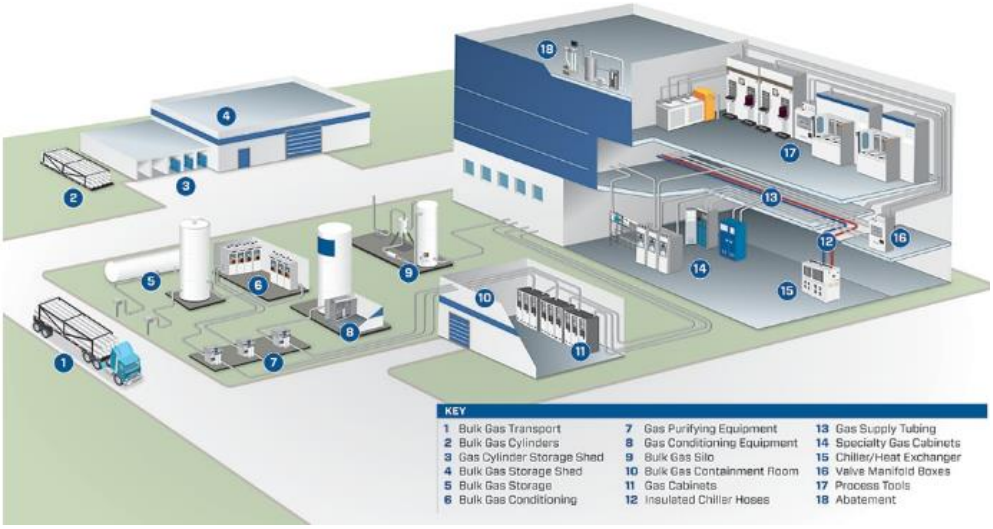
Level 4: Utility Level

The utility level, typically housed on the bottom level but also housed on the side of the structure or within its own facility, provides services that include ultrapure water, bulk high purity gases such as nitrogen and argon, exhaust gas handling and disposal, and clean room air systems. Figure 6 list those systems that are located in the utility space.

[28] https://www.lindner-group.com/en/news/detail/photolithography-led-amber-light-for-clean-rooms-and-semiconductor-manufacturing-6634/

[29] https://www.jedunn.com/projects/p127475-basebuildlayout-dependent

Figure 6: List of utility systems



Source: Swagelock

Examples of Eligible Property

Eligible property under 48D for fabrication, ATP, and manufacturing equipment facilities could include, but is not limited to, the following:

- Photolithography tools
- Deposition and etching tools used in the processes of Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), and Damascene Electro Plating (DEP)
- E-Beam Operation tools (to repair masks), electroplating tools, and ion implant tools
- Mask manufacturing equipment
- Photomasks/reticles/pellicle, steppers, scanners and photoresist related equipment
- Emulation tools
- Inspection and metrology equipment, including scanning electron microscopes, atomic force microscopes, ion milling tools, optical inspection systems, wafer probes and optical scatterometer
- Rapid thermal processing tools (annealing tubes and vacuum ovens), melting laser annealing (MLA) equipment, wafer bonding equipment, physical removal processing tools (flycutter, DieSaw, and backgrind), and edge seal dispense
- Chemical mechanical polishing equipment
- Site preparation
- Construction/expansion/upgrade/modification of facility, including special construction to minimize vibrations and earthquake protection
- Site Infrastructure – energy, water, natural gas, backup power generators, transformers, stormwater management, fire protection, other
- Sub fab
- Clean room equipment and specialty cleaning equipment
- Equipment and installation (wiped-film evaporators)
- Pumps and other tool specific abatement equipment and installation

- Chemical and gas delivery systems - piping, storage and waste systems (including hazardous waste)
- Bulk chemical storage and purification systems (Liquid N2, Ar, H2, etc.)
- Semiconductor grade Water recycling and purification systems
- HVAC Air conditioning and air handling systems, critical cooling water systems, heating systems
- Ultra-pure water systems
- Specialized lighting
- Pollution controls – air (abatement, scrubbers, stacks, etc.), wastewater treatment, waste systems
- Storage systems for critical inputs to the fabrication process (Masks, spare parts, front opening unified pods, etc.)
- Wafer stockers with temperature and air quality control
- Automated material handling system (AMHS) (wafer handling systems to move wafers within manufacturing facility)
- Advanced Wafer routing software systems and databases
- Manufacturing automation and control equipment, including mechanisms to move wafers among tools IT infrastructure
- Backup systems to ensure operational continuity
- Temperature control systems
- Locker/gowning rooms
- Security and/or monitoring systems/devices
- Warehousing and storage, and associated handling systems
- Failure analysis labs and equipment
- Quality assurance equipment including incoming goods, in-process inspection, and finished-good inspection
- Computer Data Center (CDC) and related facilities that is used for manufacturing monitoring, data analysis and related functions
- Software and IT programs that are used for manufacturing purpose;
- Jigs, hand tools, calibration equipment, temperature and pollution monitoring tools and etc. that are used in clean room;
- Transportation, trolleys and carts that are used to transport wafers

2. Assembly, Test, and Packaging Facilities

An IRS notice provides a high-level summary of ATP and its role in the manufacturing process:[30]

> During the front-end process (wafer fabrication), silicon or other materials are prepared and wafers are fabricated and subjected to a number of processing steps to produce multiple copies of an electronic circuit or "die" on the wafer. This wafer fabrication is indisputably considered to be a manufacturing activity.
>
> During the back-end process, after the die are separated and sorted, the following activities are conducted, which are generally known in the semiconductor industry as "assembly and test" activities (hereinafter "semiconductor assembly and test activities"). The good die are put through a series of processes to create the electrical connection(s) necessary for the device to function. Die are attached to a frame, substrate, printed-circuit board, or other material. The completed product is most commonly referred to as a "chip".

Outsourced semiconductor assembly and test (OSAT) vendors are the companies that offer integrated circuit (IC) packaging and test services, including wafer level services after fabrication and prior to separation of die, the separation of die and subsequent packaging and testing of separated die. OSATs provide package design support to fabless and non-fabless companies, packaging to silicon devices that are made by foundries, and test services prior to shipping to the customer. OSATs mainly focus on offering innovative packaging and test solutions for semiconductor companies in well-established markets such as communications, consumer & computing, automotive, aerospace, defense, and space in addition to emerging markets in industrial, medical, the Internet of Things (IoT), artificial intelligence (AI), and wearable devices. OSATs offer cost-effective and innovative packaging solutions that enable higher performance, processing speeds and functionality of ICs with a reduction in space in an electronic device.

OSAT companies come into major play at the end stage of the semiconductor manufacturing process after the wafer fabrication and wafer probe stages. OSATs offer packaging and assembly solutions that involve the processing of bare semiconductors into finished semiconductors, which helps in protecting the die as well as facilitating electrical connections and heat dissipation. After packaging the customer's die, OSATs conduct final testing to ensure that the packaged semiconductor meets performance specifications. OSATs offer a wide range of semiconductor test services that includes various types of final, system-level, wafer, and strip testing along with the complete end of line services up to and including final shipping.

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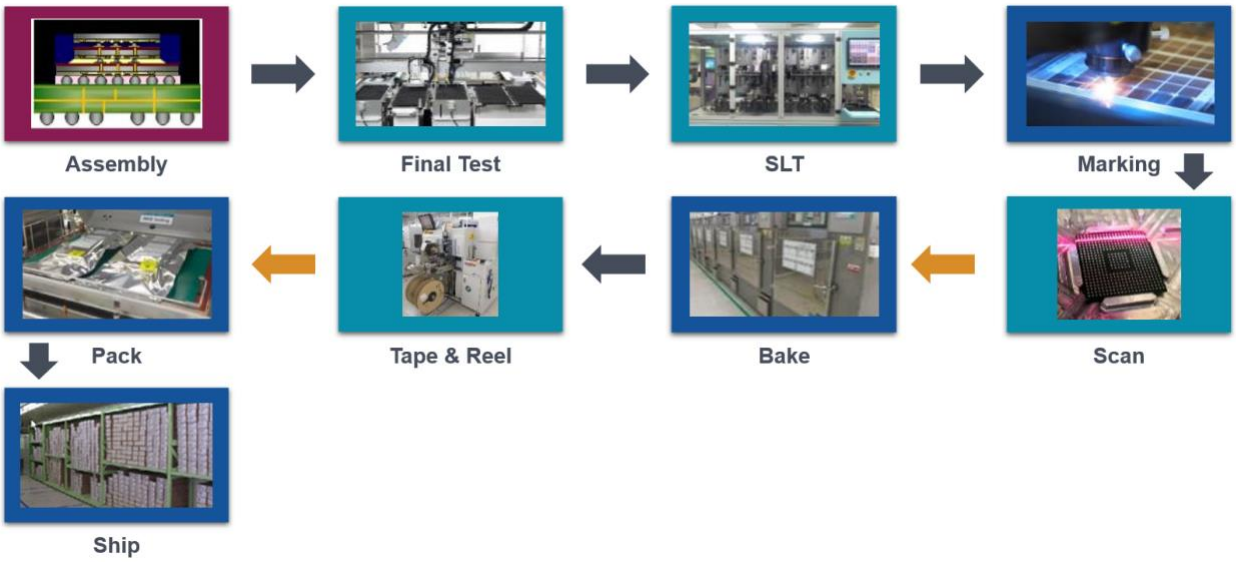
[30] *See* Internal Revenue Service Industry Directive, "Treatment of Semiconductor Assembly and Test Activities as Manufacturing" (March 16, 2006) (footnotes omitted), available at https://www.irs.gov/businesses/treatment-of-semiconductor-assembly-and-test-activities-as-manufacturing. See also *Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth: 100-Day Reviews under Executive Order 14017* (June 2021), *available at* https://www.whitehouse.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf (hereinafter White House Report) at 41-43.

Figure 7. Packaging and test services are an integral part of the worldwide semiconductor supply chain

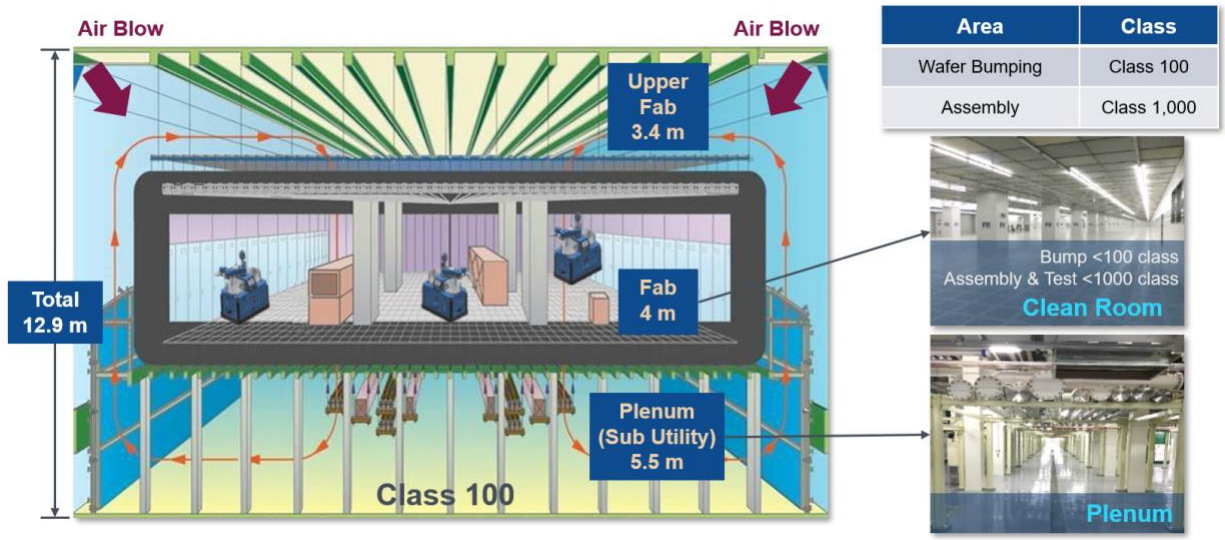
Source: Amkor Technology

Figure 8. Test operations



Source: Amkor Technology

Figure 9. Example of an ATP clean room



Source: Amkor Technology

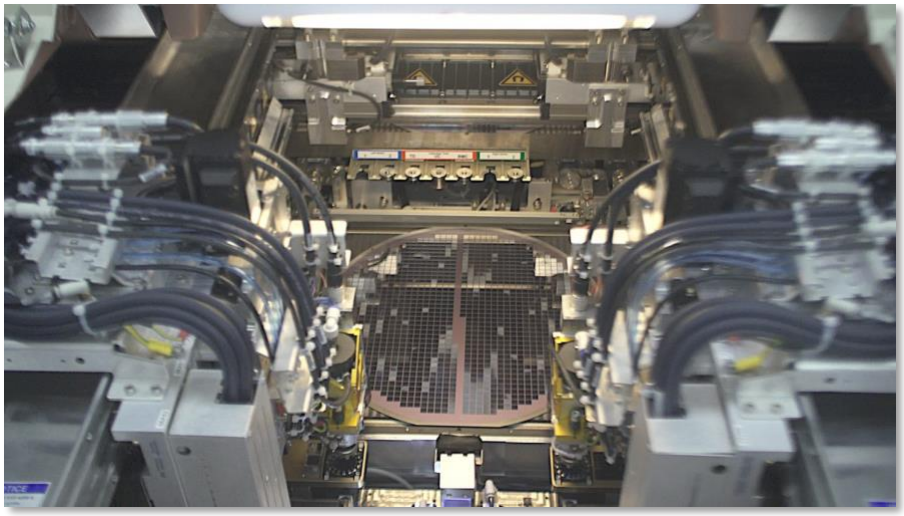
Figure 10. Example of an ATP facility

Source: Amkor Technology K5 Center of Excellence Facility in South, Korea

Figure 11. Example of an ATP clean room

Source: Amkor Technology

Figure 12. Example of fan-out flip chip attach equipment



Source: Amkor Technology

Figure 13. Component kitting

Source: Amkor Technology

Figure 14. FCBGA & SiP thermal conductive bonding

Source: Amkor Technology

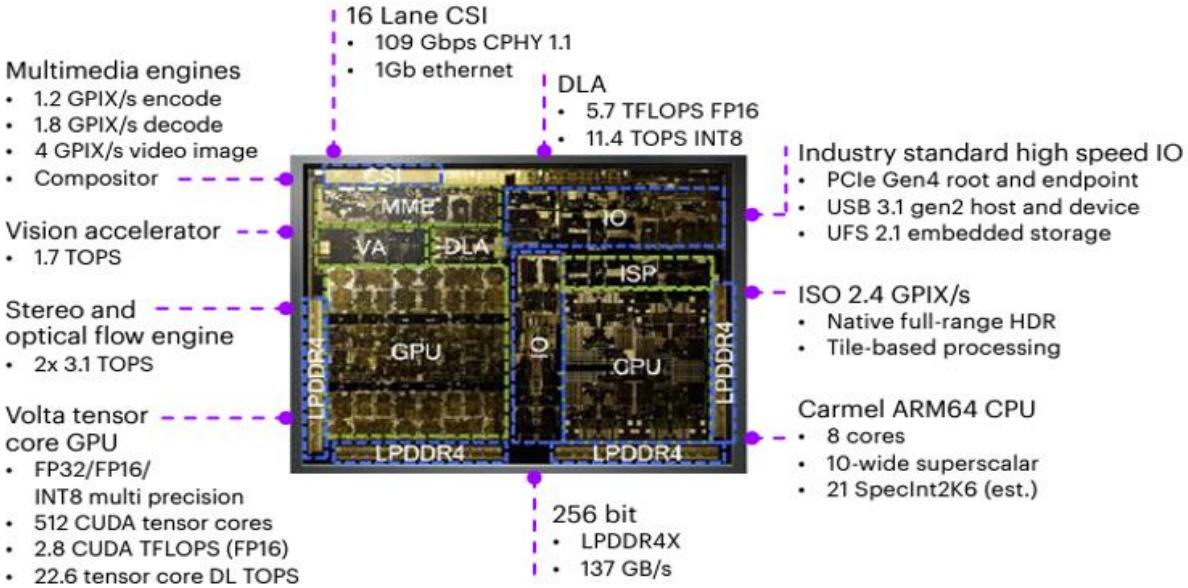
3. Chip Design

Semiconductor Design

Semiconductor design is an integral part of the chip fabrication process. The design stage requires large teams of highly skilled design engineers, each with different specialties, to prepare a design ready for production. Design companies collaborate closely with manufactures and ATP facilities to ensure their designs are successfully fabricated on a wafer and subsequently packaged in a device.

Semiconductor manufacturing is reliant on the key partnership between chip design and the fab, one cannot be done without the other. To illustrate the complexity of chip design, Figure 15 displays a diagram of a chip. Each part of the chip is carefully placed to ensure it provides the right processing power and energy efficiency. Design engineers work closely with the manufacturer to ensure the chip can be produced at the desired specification with the appropriate raw materials. For example, different semiconductor types require different materials to be produce for the desired product. Logic chips, commonly used in a computer processing unit (CPU), are produced on silicon wafers. Semiconductor power devices or radio frequency (RF) based chips, commonly used in applications that are exposed to very high temperatures, can be produced on sapphire wafers using Gallium Nitride (GaN).

Figure 15: Diagram of a sample chip



Source: Accenture

While many kinds of companies engage in semiconductor design, the major types are listed below:

- **Fabless companies.** (~47% of design-related value add) These companies focus exclusively on chip design, and partner with third-party merchant foundries to fabricate (that is, manufacture) their chips.

- **Integrated device manufacturers (IDMs)**. (~51% of design-related value add) IDMs both design and manufacture chips. Within IDMs, design and manufacturing teams work together to bring to market new chips usually at in-house fabrication facilities.

- **Original equipment manufacturers**. (less than 2% of design-related value add) OEMs, like auto makers, use semiconductors as inputs for other products. Some OEMs have begun to design their own chips, primarily for their own products. For example, a cloud computing provider may design custom chips with specific features that execute specific tasks very well. OEMs are a growing presence in chip design and increasingly participate in the same product and talent markets as fabless companies or IDMs.

Another important part of the design ecosystem are electronic design automation (EDA) companies, which provide the design tools and reference flows and serve as trusted intermediaries between design companies and foundries. Third party IP providers design and license IP building blocks (processors, libraries, memories, interfaces, sensors and security).

Figure 16: Design life cycle

Source: Accenture

Fabless companies often work closely with a given foundry's design services team to ensure the compatibility of their designs with the foundry's fabrication processes. Close collaboration is critical, as scaling up new processes involves inherent uncertainties in modeling and reaching target manufacturing yields. Tangible property in respect to 48D could include, but is not limited to, the following:

- Facility construction/expansion/upgrade/modification
- Design automation tools
- Digital verification tools (simulation)
- Verification capital equipment (programmable hardware for circuit emulation)
- Test equipment

Semiconductor Manufacturing Equipment

Production of the equipment used in semiconductor manufacturing is equally capital intensive and requires skilled talent. Furthermore, the facilities that manufacture the equipment are complex and require similar support systems and structures as fabs. For example, these facilities contain clean rooms that require workers to wear protective gear to eliminate contaminants.

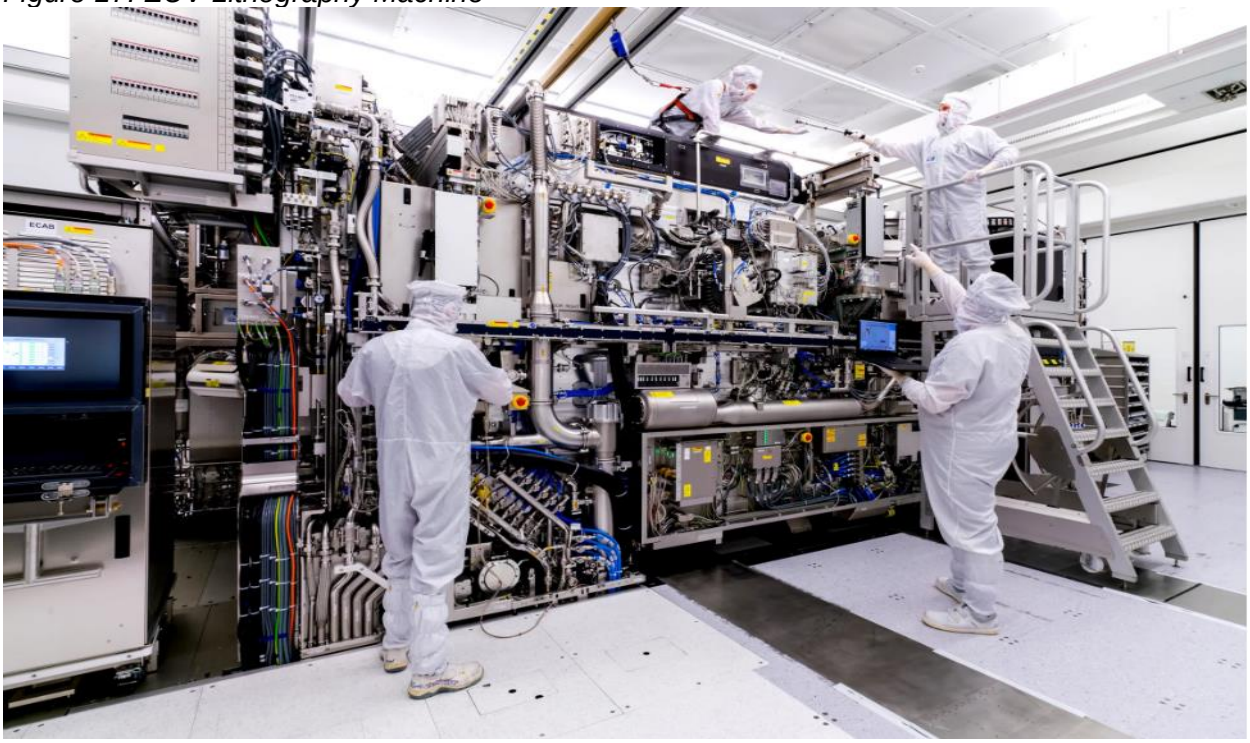
The White House supply chain report summarizes the manufacturing equipment used in the process of producing semiconductors as follows:

> There are multiple categories of SME, each used in a different step of semiconductor production line. There are equipment types specific to manufacturing bare wafers (covered under "Materials" above), processing the bare wafer to semiconductors on a wafer (Front-end), packaging (Back-end), and equipment for manufacturing photomasks (mask manufacturing). Chip manufacturers need all the categories of front-end equipment in their manufacturing line. The cost of complex front-end semiconductor manufacturing equipment is a major reason (along with construction costs) for the high cost of a semiconductor fab. Front-end SME include equipment for fabrication steps, including lithography, etching, doping or ion implantation, deposition, and polishing or chemical mechanical planarization. Of particular note is metal organic chemical vapor deposition (MOCVD) equipment, a specific type of deposition equipment that deposits thin layers of certain metals, used primarily for the production of compound semiconductors, including those based on GaAs and GaN. Back-end SME includes equipment for ATP and advanced packaging.[31]

Current leading-edge lithography equipment, called Extreme Ultraviolet (EUV) Lithography machines, are extremely large and complex systems. These machines contain tens of thousands of parts and kilometers of cabling. These machines are so large that shipping the components can require multiple freight containers, cargo planes, and trucks. The separate components of this machine in itself are complex and require thousands of parts. Some parts are highly specialized and may have a single supplier.

[31] *See White House Report* at 49.

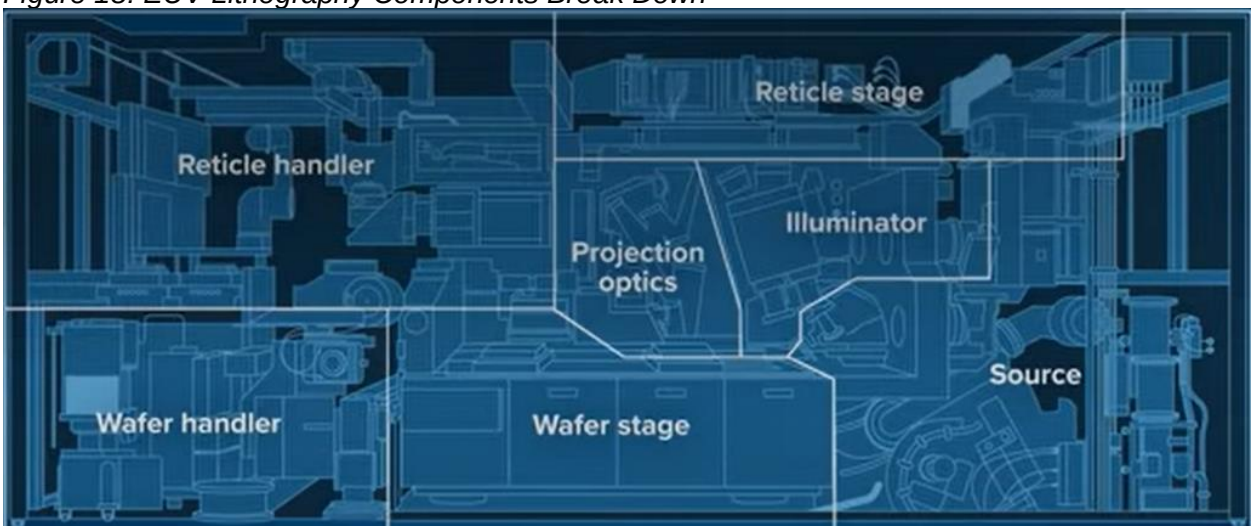
Figure 17: EUV Lithography Machine



Source: Wired

The separate modules of the EUV machine are shown in Figure 18. The modules are specialized and require parts that meet exacting specification. If any part is faulty, the machine will fail to produce chips that can be sold for commercial use. In addition, each module is manufactured in a different facility that is dedicated to the production of that module.

Figure 18: EUV Lithography Components Break Down



Source: CNBC

Leading semiconductor equipment manufacturers make the science of polishing low-aberration optics an art, using advanced equipment only available at a few companies worldwide. Optics worth a quarter of a million dollars are polished within two orders of magnitude more precisely than eyeglasses. Semiconductor equipment manufacturers also specialize in optical contacting of very large surfaces. By achieving an extremely flat surface, two pieces of glass are fused together to form an indestructible bond, without any glue on a larger scale than any other industry.

Optical sensors and metrology systems

Sensors produced by semiconductor equipment manufacturers in the US must also withstand extreme wear and tear conditions. One manufacturer has more than 15 chambers that make up its robust coating capabilities. Its diamond-like carbon coating is like those used on military aircraft cockpit glass. Sensors are developed that bring together the best in complex optical designs, along with optomechanics, electronics and software to perform sub-nanometer measurements to keep lithography systems operating at peak performance. Optical sensors are found throughout lithography, metrology and inspection systems.

As chip patterns continue to shrink, optical sensor designs are pushed to extremes. Advancements focus on reducing measurement time, while capturing larger datasets that help increase a lithography system's precision. This requires US employees to push the boundaries for optics, including state-of-the-art polishing and coating technologies, as well as ultra-fast precision mechatronics.
Specialty glass lenses, like high purity fused silica or ultra-low expansion glass, are also use by photolithography machines to etch chip designs. These lenses are specifically made for the manufacturing of semiconductors and are directly responsible for the lasers used in photolithography, metrology, and inspection. The equipment is customized via a months-long process and must be of the highest durability so that the photomasks and lenses are able to withstand billions of laser pulses used in semiconductor manufacturing. Mirrors and lens assemblies are used in wafer defect inspection (as is the emulation hardware described above), which is a step in the manufacturing process that occurs after wafer printing.

Mechatronic systems

Semiconductor equipment manufacturers in the US design, test and assemble two crucial modules of lithography systems: the reticle handler and the reticle stage. These two modules move and hold the blueprint of the chip pattern that will be printed (known as a 'mask' or 'reticle').

The reticle handler operates with surgical precision to carefully move its payload between locations in the machine, without dropping or distorting it. This sophisticated robot is in constant motion and must account for vibrations that are greater than its position accuracy requirements. It transfers the reticle within 20-25 micrometers of the same location, every time, yet the floor vibrates more than half a meter per second squared.

It's a complex engineering challenge, which becomes increasingly difficult with next-generation EUV lithography tools. Here a system of robots operate in parallel to move the reticle into and

out of the vacuum chamber. For every one million movements, the reticle handler cannot generate more than one particle that lands on the reticle.

Once the reticle is received, the reticle stage securely holds it in place, without distorting or allowing it to move by more than a few picometers. The completely magnetically levitated stage accelerates at more than 15 g, more than three times the g-force experienced by a fighter jet pilot at takeoff, up to a velocity of more than three meters per second. It positions the reticle within fractions of nanometers in all six degrees of freedom at full speed.

The motors that propel the reticle stage generate more than 10,000 newton (N) of thrust force, which would be like dropping a car onto the reticle stage every time it accelerates. It does this billions of times over its lifetime without damaging itself or the reticle, or generating any particles that might contaminate the air.

Light Source Technology

Semiconductor equipment manufacturers also design, develop and qualify EUV (extreme ultraviolet) light sources, as well as manufacture a critical system component called the droplet generator. The droplet generator is the heartbeat of the source, delivering a steady stream of 50,000 liquid tin droplets per second, which fly at more than 150 miles per hour in a vacuum vessel. The size, spacing and frequency of the droplets all impact the amount of EUV light produced.

Each droplet – whose size is a fraction of the thickness of a human hair – is individually imaged and targeted by two high-power CO2 laser pulses, generating a plasma that emits EUV light. A highly polished, multilayer mirror collects and reflects the 13.5-nanometer EUV light to a precise exit point of the vessel and directed at a lithography scanner.

This requires a system of lasers, cameras and other sensors (collectively called vessel metrology) to ensure the creation, optimization and regulation of stable plasma for EUV generation. US engineers must determine the optimal points in space and time for the laser to target droplets to generate the plasma, requiring extreme precision and synchronization. The resulting EUV light output must meet precise energy profile requirements for the scanner so that every die is evenly exposed by EUV light on the wafer.

Tin management is also a unique and challenging problem within the EUV source, since the material is necessary, as it is required to create the light source, but it can contaminate the optics. US personnel of semiconductor equipment manufacturers focus on researching and developing effective mechanisms to capture and remove tin from the vessel, as well as transport the tin out of the system.

Deep ultraviolet (DUV) light sources are also produced in the US. While such technology is more mature and established in the market, manufacturing sites in the US continue to innovate with DUV light sources both from a technology and a cost standpoint. These light sources include excimer lasers using argon fluoride (ArF) or krypton fluoride (KrF) gases to generate light in the deep-ultraviolet spectrum. These lasers generate the light that photolithography scanners use to image patterns on silicon wafers. Significant advances in product performance have been achieved through Solid State Power technology, 193nm lithography and dual

chamber architecture, among many others. DUV light sources are fundamental to virtually all chipmakers. Development, manufacturing and servicing of these light sources in the US contributes to this key portion of the semiconductor supply chain.

SEMICONDUCTOR INDUSTRY ASSOCIATION

Appendix B
Comments of the
Semiconductor Industry Association (SIA)
On the
CHIPS Program Office (CPO)
National Institute of Standards and Technology (NIST)
Proposed Rule
On
Preventing the Improper Use of CHIPS Act Funding
RIN 0693-AB070, NIST-2023-0001
88 Fed. Reg. 17439 (March 23, 2023)

May 22, 2023

The Semiconductor Industry Association (SIA)[32] appreciates the opportunity to comment on the Proposed Rule of the CHIPS Program Office (CPO) within the National Institute of Standards and Technology (NIST) of the Department of Commerce (collectively, "Commerce" or "the Department") on Preventing the Improper Use of CHIPS Act Funding (collectively, "the guardrails" or "the Proposed Rule"). SIA looks forward to future engagement and partnership as the CPO advances its important work in implementing the guardrails on the incentives funded in the historic CHIPS and Science Act.[33]

SIA supports the economic and national security objectives of the CHIPS Act and agrees with the stated mission from the preamble that the CHIPS Incentives Program "aims to strengthen the resilience and leadership of the United States in semiconductor technology, which is vital to national security and future economic competitiveness of the United States." (88 Fed. Reg. at 17440). SIA believes the regulations implementing the guardrails should be designed to achieve its goals while avoiding unnecessary supply chain disruptions and provide predictability and transparency, consistent with the statutory text of the CHIPS Act.[34]

The guardrails in the CHIPS Act were enacted in recognition of the complex role of China in the global semiconductor ecosystem, the global supply chain and economy as a whole, and the national security landscape. For the global semiconductor industry, China is simultaneously: (1) an enormous market, comprising approximately one-third of all chip sales; (2) a major part of the semiconductor supply chain, with about 20 percent of front-end capacity and nearly 40 percent of back-end capacity; and (3) a major competitor, with a growing industry in all

[32] The Semiconductor Industry Association (SIA) is the voice of the semiconductor industry, one of America's top export industries and a key driver of America's economic strength, national security, and global competitiveness. Semiconductors – the tiny chips that enable modern technologies – power incredible products and services that have transformed our lives and our economy. The semiconductor industry directly employs over a quarter of a million workers in the United States, and U.S. semiconductor company sales totaled $275 billion in 2022. SIA represents 99 percent of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. chip firms. Through this coalition, SIA seeks to strengthen leadership of semiconductor manufacturing, design, and research by working with Congress, the Administration, and key industry stakeholders around the world to encourage policies that fuel innovation, propel business, and drive international competition. Additional information is available at www.semiconductors.org.
[33] Public Law 117-167.
[34] 15 USC Ch. 72A

segments of semiconductor research, design, fabrication, packaging, equipment, and materials. Given this multifaceted and complex relationship, Congress constructed a complementary statutory framework to ensure that as the U.S. provided incentives to attract investments in new semiconductor fabrication facilities to strengthen the economy and make the domestic supply chain more resilient, it would restrict certain investments and limit the flow of sensitive technologies to China to address national security concerns and supply chain dependence. Consistent with this approach, the "guardrails" established by the CHIPS Act focus primarily on limiting increases in advanced semiconductor manufacturing capacity in China and the transfer of know-how of certain semiconductors to China by funding recipients, while at the same time allowing for the continued operation of existing legacy facilities and the construction of new or expanded legacy facilities predominantly serving the China market. These exceptions to the guardrails for the continued operation of existing legacy facilities in China are necessary to avoid causing disruption to the global chip supply chain and protect prior investments.

In executing this complex framework in the Proposed Rule, however, SIA believes Commerce, in certain instances, needs to strike a better balance. As set forth in detail below, certain aspects of both the expansion clawback[35] and the technology clawback[36] should be modified to better implement the statute and achieve the proper balance struck by Congress in the CHIPS Act. For example, while Congress expressly exempted existing facilities for manufacturing legacy semiconductors from the "expansion clawback," certain aspects of the Commerce proposal impair the ability of funding recipients to maintain the commercial viability of their existing legacy facilities. Similarly, while Congress restricted funding recipients from engaging in joint research or technology licensing with a foreign entity of concern, Commerce proposal extended this restriction in an overly broad manner to include ordinary business activities such as patent licensing and participation in standards development organizations. If implemented as currently drafted, the Proposed Rule could unnecessarily hamper the competitiveness of funding recipients among industry competitors and increase the administrative burden and cost of compliance with the Proposed Rule's requirements. SIA's comments seek to advance the economic and national security goals of the CHIPS Act while enabling funding recipients to continue these ordinary business activities, as intended by Congress.

I. Expansion Clawback

In enacting the financial assistance program under the CHIPS Act and the "advanced manufacturing investment credit" under Section 48D of the Internal Revenue Code, Congress included "guardrails" to ensure that companies receiving CHIPS grants or claiming the tax credit would not build new semiconductor manufacturing facilities (except for facilities that produce legacy semiconductors and predominantly serve the market of the foreign country of concern) or expand existing facilities that produce non-legacy semiconductors in foreign countries of concern. Congress took this action to prevent the CHIPS funding or tax credit from effectively subsidizing new construction or the significant expansion of non-legacy manufacturing capacity in foreign countries of concern. Congress indicated the guardrails are an essential part of the

[35] 15 U.S.C. 4652(a)(6)
[36] 15 U.S.C. 4652(a)(5)(C)

overall goal of the CHIPS Act to build a stronger semiconductor ecosystem in the U.S. and a more resilient global supply chain.

Certain requirements in the Proposed Rule, however, go beyond the goal set forth by Congress in the plain terms of the statute and otherwise unduly restrict ordinary business activities in the semiconductor industry. SIA calls on Commerce to revise certain aspects of the proposal consistent with the language of the CHIPS Act and provide more flexibility for compliance for funding recipients that have existing legacy manufacturing facilities in a country of concern.

A. The CHIPS Act expressly exempts existing legacy facilities from coverage under the guardrails.

1. Revisions needed to implement congressional intent

On or before the date of a CHIPS grant award, Congress requires Commerce execute an agreement with a proposed recipient specifying that the entity "may not engage in any significant transaction . . . involving the material expansion of semiconductor manufacturing capacity" in China or another foreign country of concern. (15 U.S.C. § 4652(a)(6)(C)(i)). However, Congress created two exceptions to this general rule. The CHIPS Act expressly states that the prohibition shall not apply to:

> (I) existing facilities or equipment of a covered entity for manufacturing legacy semiconductors; or
>
> (II) significant transactions involving the material expansion of semiconductor manufacturing capacity, that – (aa) produces legacy semiconductors; and (bb) predominately serves the market of a foreign country of concern. (15 U.S.C. § 4652(a)(6)(C)(ii)).

Consistent with the broader economic and national security goals of the CHIPS Act, these two exceptions incentivize investments in the U.S. semiconductor ecosystem and rebalance the supply chain to make it more resilient in the long term, without causing disruptions in the short term.

In the preamble to the Proposed Rule, the CPO clearly recognizes the intent of Congress to exclude existing legacy facilities as a means of avoiding a potentially severe disruption of the global semiconductor supply chain:

> In recognition that some potential applicants for CHIPS Incentives may have existing facilities in foreign countries of concern, and to minimize potential supply chain disruptions, the Act includes exceptions for certain transactions involving older (legacy) semiconductor manufacturing in a foreign country of concern. (88 Fed. Reg. at 17440).

The Proposed Rule includes language that mirrors the language of the CHIPS Act, stating that the manufacturing expansion prohibition "does not apply to – (1) A funding recipient's existing facilities or equipment for manufacturing legacy semiconductors that exist on the date of the award." (15 CFR § 231.202(a)).

The proposed definition of an "existing facility," however, dilutes the exemption set forth in the statute. First, the proposed definition states: "Existing facilities shall be defined by their semiconductor manufacturing capacity at the time of the required agreement; a facility that undergoes significant renovations after the required agreement is entered into shall no longer qualify as an 'existing facility.'" (§ 231.103). The Proposed Rule then defines a "significant renovation" as "any set of changes to a facility that, in the aggregate during the applicable term of the required agreement, increase in manufacturing capacity (as defined in 231.119) by adding an additional line or otherwise increase semiconductor manufacturing capacity by 10 percent or more." (§ 231.122).

The Proposed Rule's definition of "significant renovation" is found nowhere in the text of the CHIPS Act and needlessly narrows the scope of the exemption adopted by Congress. The statute clearly states that the required agreement restricting transactions to expand semiconductor manufacturing capacity in a foreign country of concern "shall not apply to" specified circumstances, including "existing facilities or equipment of a covered entity for manufacturing legacy semiconductors." Despite this clear statutory language, the Proposed Rule substantially narrows the exemption provided by Congress for existing legacy facilities and limits the ability of companies to protect and maintain past investments in these existing facilities.

China is an important player in the global semiconductor ecosystem, representing approximately 21% of global overall manufacturing capacity[37] and a substantial share of global capacity for legacy semiconductors (19% of 28-45nm logic, 23% of >45nm logic, and 14% of memory).[38] Approximately two-third of this capacity is held by Chinese companies, with the remaining one-third held by foreign companies.[39] China is also home to the largest share of global assembly, test, and packaging (38%).[40] Potential CHIPS Act funding recipients have numerous existing legacy facilities in China, and it is critical for these companies to be able to protect their past investments in these facilities by ensuring they remain commercially viable.

SIA calls on Commerce to make certain revisions to the proposal, including the modification of the "significant renovation" restrictions on existing legacy facilities to reflect Commerce's stated intent to "ensure minimal disruptions to revenues, for the foreseeable future, to firms that currently have productive capacity in countries of concern." (88 Fed. Reg. at 17443). With these changes, the commercial viability of existing legacy facilities can be maintained during the applicable term of the guardrails and advanced manufacturing investment credit.

Specifically, Commerce should revise the definition of "significant renovation" to limit it to new cleanroom construction or the addition of a manufacturing line that is not part of the legacy facility's designed capacity level. Alternatively, significant renovation could be defined as an increase in the square footage of an existing facility by a specified percentage. Either

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[37] SIA, State of the Industry Report, November 2022 (*Available at* https://www.semiconductors.org/wp-content/uploads/2022/11/SIA_State-of-Industry-Report_Nov-2022.pdf)
[38] SIA/BCG, Strengthening the Global Semiconductor Supply Chain in an Uncertain Era, April 2021 (*Available at* https://www.semiconductors.org/wp-content/uploads/2021/05/BCG-x-SIA-Strengthening-the-Global-Semiconductor-Value-Chain-April-2021_1.pdf)
[39] SIA Research
[40] Ibid.

modification will allow equipment upgrades and replacements, software development efficiencies, maintenance activities, the completion of ramping up activities, and the addition of originally planned lines that may have the effect of increasing manufacturing capacity in order to maintain the facility's commercial viability.

Recommended change to §231.122 Significant renovations

Significant renovations means building new clean room space or ~~Semiconductor manufacturing capacity (as defined in § 231.119) by~~ adding an additional line that is not part of the semiconductor manufacturing capacity level for which the facility was designed. ~~or otherwise increase semiconductor manufacturing capacity by 10 percent or more.~~

If Commerce accepts this revision, modifications to the definition of "existing facility" would be required.

Recommended corresponding change to § 231.103 Existing facility

Existing facility means any facility built, equipped, and operating ~~at the semiconductor manufacturing capacity level for which it was designed~~ prior to entering into the required agreement. Existing facilities must be documented in the required agreement. ~~Existing facilities shall be defined by their semiconductor manufacturing capacity at the time of the required agreement;~~ A facility that undergoes significant renovations after the required agreement is entered into shall no longer qualify as an "existing facility." The Secretary, in consultation with the Secretary of Defense and Director of National Intelligence, may determine that a facility, based on the facts and circumstances, including where construction is underway and the facility is not yet operating, is an existing facility.

These proposed changes will advance the goal of preventing the addition of significant manufacturing capacity in a country of concern while also reducing overall complexity and improving accountability, because physical expansions are easier to identify and less company- or technology- specific than capacity measured by output. This approach will (1) ensure that the exception is not being circumvented by building new, adjacent structures to existing facilities and (2) allow all existing facilities to remain commercially viable and competitive. Owners of these existing facilities should be able to complete their facility as it was designed, which includes the upgrade and replacement of equipment, the finishing of the ramping up process, the installation of equipment that has been purchased but not delivered, full capacity utilization as market conditions require, maintenance and refurbishment of equipment, and other activities that may be needed for the facility to operate at its designed capacity.

2. Alternative proposed revision to implement congressional intent

If Commerce does not accept the proposed revision in I.A.1., SIA recommends alternative revision to these definitions. The Proposed Rule inconsistently defines the baseline for semiconductor manufacturing capacity of existing facilities. The current definition of "existing facility" first describes an existing facility as "operating at the semiconductor manufacturing capacity level for which is was designed," but subsequently states that existing facilities "shall

be defined by their semiconductor manufacturing capacity at the time the required agreement is signed." (§231.103). These appear to be two very different measurements of "manufacturing capacity" for the purpose of determining if the expansion clawback has been violated or whether an exception applies.

Most facilities do not always run at their full designed capacity. Specifically, for many facilities, there could be a significant gap between the planned/designed capacity of a facility and its actual output at the time a funding agreement is signed, given market conditions, ramping up activities, and other factors. Production also fluctuates from one quarter to another based on market conditions and product demand. Others may be awaiting the installation of one or more pieces of new or replacement equipment that had been purchased or ordered before the Proposed Rule was issued and should be considered part of the semiconductor manufacturing capacity level for which the facility was designed. Revising the definition of "existing facility" to account for the full designed capacity at the time the facility was planned will allow funding recipients to, as the preamble states, "maintain productive capacity in foreign countries of concern and produce semiconductors that fall within the thresholds contemplated in the proposed regulation." (88 Fed. Reg. at 17442).

The clarification of this baseline in the definition of "existing facility" is necessary to protect the significant investments in these facilities, which can take years to build and may involve billions of dollars. As the preamble to the Proposed Rule recognizes, "[a]bandoning a finished or ongoing project could jeopardize customer relationships and ongoing revenue" and that once "projects are underway, there likely would be significant costs to reverse such decisions" (88 Fed. Reg. at 17443). There are major unrecoverable costs for a manufacturing facility for which the construction was underway before the Proposed Rule was issued. Some facilities may be in the process of ramping up and are not yet fully operating. Accordingly, such projects, should be considered existing facilities by determination of the Secretary, in consultation with the Secretary of Defense and Director of National Intelligence.

> Alternative recommended change to § 231.103 Existing facility
>
> *Existing facility* means any facility built, equipped, and operating ~~at the semiconductor manufacturing capacity level for which it was designed~~ prior to entering into the required agreement. Existing facilities must be documented in the required agreement. Existing facilities shall be defined by the~~ir~~ semiconductor manufacturing capacity level for which it was designed, including project capacity that may not be currently in production. ~~at the time of the required agreement; a~~ A facility that undergoes significant renovations after the~~ required agreement is entered into~~ date of award under 15 U.S.C. 4652 shall no longer qualify as an "existing facility." The Secretary, in consultation with the Secretary of Defense and Director of National Intelligence, may determine that a facility, based on the facts and circumstances, including where construction is underway and the facility is not yet operating, is an existing facility.

This approach would require applicants to demonstrate through construction plans or otherwise an existing facility's designed capacity in the relevant application materials. Applicants are already required to disclose information about current and future plans in foreign countries of concern, and requiring the disclosure of a facility's design capacity creates certainty for both parties on the baseline capacity, making compliance more practical and achievable.

If the definition of significant renovation is not modified to reflect the changes proposed in I.A.1, a technical correction is needed to clarify that a significant renovation occurs *either* from an additional line that increases capacity *or* another increase in capacity. Additionally, the preamble states that the CPO intends to allow funding recipients to "modestly expand capacity at existing facilities producing mature (legacy) technology" (88 Fed. Reg. at 17443). SIA suggests a limited increase in the threshold of "significant renovation" to at least 15 percent. This will help to maintain Commerce's objectives of only allowing modestly expanding capacity while ensuring existing facilities can be reasonably maintained alongside similar investments located elsewhere over the course of the 10-year period.

> Recommended change to §231.122 Significant renovations
>
> *Significant renovations* means any set of changes to a facility that, in the aggregate during the applicable term of the required agreement, increase semiconductor manufacturing capacity (as defined in § 231.119) by adding an additional line or otherwise increase semiconductor manufacturing capacity, in either case, by [15]~~10~~ percent or more.

B. The guardrails should allow for continued, commercially viable operations at existing facilities through reasonable accommodations

The Proposed Rule should be revised to enable funding recipients to maintain the basic competitiveness of their existing facilities. As currently drafted, the Proposed Rule would prohibit ordinary maintenance and upgrades necessary to allow the continued operation of existing facilities, even if these activities may result in an incidental increase in the capacity of these facilities.

1. Allow for reasonable, limited activities that may moderately increase capacity

The current definitions of "significant transaction" and "material expansion" will have adverse impacts on normal efficiency upgrades and ordinary productivity improvements to existing facilities during the course of facility operation. Funding recipients with existing facilities in a country of concern must be able to conduct necessary activities – such as the purchase of software, increasing the efficiency of existing equipment, replacement tools or parts, and other necessary upgrades – to effectively maintain longstanding business operations and allow such entities to realize the economic value of their investments made prior to the grant of CHIPS Act funding. New semiconductor manufacturing equipment typically has higher throughput compared to older iterations that are less efficient and often may no longer be commercially available for purchase. Likewise, software engineering improvements are periodically needed to maintain competitive operations at a facility. Under the Proposed Rule, any combination of these basic activities over time could result in an increase in semiconductor manufacturing capacity and thereby potentially violate the expansion prohibition and trigger a clawback. Such a result seems contrary to the stated objective of the preamble to "allow recipients to upgrade technology at existing foreign facilities (in compliance with export controls) if overall production capacity is not increased" (88 Fed. Reg. at 17443). The Proposed Rule should be revised to accommodate these routine upgrades, which will evolve over a 10-year period.

As noted above, the CHIPS Act expressly excludes significant transactions involving the material expansion of existing legacy facilities from these prohibitions. However, if Commerce maintains the concept of material expansion as set forth in the Proposed Rule, additional revisions to these definitions are necessary. SIA requests Commerce clarify that material expansions only pertain to additions of physical space or manufacturing lines that increase semiconductor manufacturing capacity, not the upgrade, replacement, or refurbishment of equipment. Running existing tools at higher capacity, upgrades or replacement of software, maintenance or replacement of older machines and parts with higher throughput/output, and/or engineering improvements for routine maintenance to continue current operations that increase capacity above a defined threshold at an arbitrary time should not considered material expansions. Additionally, equipment repair or replacement may be required to comply with environmental, safety, or other regulatory requirements of the country of concern. The Proposed Rule must account for such necessary action, with the alternative potentially being that certain equipment is taken out of operation. Of course, the physical expansion or addition of a manufacturing line at an existing facility (e.g., new buildings, physical expansion of a facility to add new manufacturing lines, etc.) are outside the scope of ordinary maintenance and upgrades and an increase in capacity at an existing legacy facility resulting from such activities would be subject to the prohibition.

The preamble states that the CPO intends to allow funding recipients to "modestly expand capacity at existing facilities producing mature (legacy) technology" (88 Fed. Reg. at 17443). SIA suggests a limited increase in the threshold of material expansion to at least 10 percent. This will help to maintain Commerce's objectives of only allowing modestly expanding capacity while ensuring existing facilities can be reasonably maintained alongside similar investments located elsewhere over the course of the 10-year period.

> Recommended change to §231.111 Material expansion
>
> *Material expansion* means the addition of physical space or an additional line ~~or equipment~~ that has the purpose or effect of increasing semiconductor manufacturing capacity of a facility by more than ~~five~~[10] percent or a series of such expansions which, in the aggregate during the applicable term of a required agreement, increase the semiconductor manufacturing capacity of a facility by more than ~~five~~[10] percent of the existing capacity when the required agreement was entered into.

Alternatively, Commerce could exclude specific aforementioned activities as not qualifying as a material expansion.

> Alternative recommended addition to the end of §231.111 Material expansion:
>
> Upgrades and replacement of software, increasing the efficiency of existing equipment, maintenance and replacements of machines and parts with higher throughput, and engineering improvements for routine maintenance to continue existing facility operations are not considered material expansions.

2. Prevent aggregation of unrelated significant transactions, and increase the threshold amount

The current definition of "significant transaction" with a $100,000 aggregated threshold is extraordinarily low and is applied over the course of the applicable term. Replacing one piece of equipment, upgrading a ventilation system, and the vast majority of other expenses are nearly certain to exceed this threshold considering the regular costs of maintaining facility operations. In many cases, these transactions are likely to be unrelated to each other and taking place in different parts of a facility for different purposes.

Additionally, in order to better capture instances of a significant transaction, SIA encourages the Department of Commerce to consider a substantially higher threshold than $100,000. Given the capital costs associated with semiconductor manufacturing, it would not be unreasonable for Commerce to set a higher threshold.

Recommended change to §231.121(b) Significant transaction

(b) A series of transactions described in paragraph (a) of this section, that are related to each other, which, in the aggregate during the applicable term of a required agreement, are valued at ~~$100,000~~ [increased amount] or more.

3. Allow for the transfer or completion of a transfer of an existing facility from one entity to another.

The rule should accommodate instances where an existing facility in a foreign country of concern is already subject to an executed sale agreement or may be purchased during the course of the applicable term. The Proposed Rule does not include an express provision allowing for such a transfer. The proposal should be revised to allow a transfer of an existing facility (1) from a funding recipient to a non-funding recipient; (2) from a non-funding recipient to a funding recipient; or (3) between funding recipients. Additionally, in some cases, a purchase agreement may have occurred prior to the required agreement, but the sale and transfer of semiconductor manufacturing businesses may take years to close, with the completion of one or more facilities at issue in a transaction delayed until the new owner(s) take over.

The definition of required agreement should be revised to reflect these potential scenarios.

Recommended Change to §231.115 Required Agreement

Required agreement means the agreement required under 15 U.S.C. 4652(a)(6)(C) that is entered into by a funding recipient on or before the date on which the Secretary awards Federal financial assistance under 15 U.S.C. 4652. The required agreement shall include, *inter alia,* provisions describing the prohibitions on certain joint research or technology licensing in § 231.202 and on certain joint research or technology licensing in § 231.203. The required agreement may be amended by mutual agreement of the Secretary and funding recipient at any point to recognize the purchase or sale of an existing facility, as defined by §231.103, from another entity. The Secretary shall not approve the amendment of the required agreement to include an existing facility if that facility undergone a significant renovation since the effective date of this Rule.

4. Measure capacity annually, not monthly

The measurements used to determine semiconductor manufacturing capacity under §231.119 should be on an average basis over the course of a year, rather than per month. This will provide a more accurate picture of the operations and allow for a smoothing of seasonal, natural and regular fluctuations in business operations.

Recommended change to §231.119 Semiconductor manufacturing capacity

Semiconductor manufacturing capacity means the productive capacity of a semiconductor facility. In the case of a semiconductor fabrication facility, semiconductor manufacturing capacity is measured in wafer starts per ~~month~~ year. In the case of a packaging facility, semiconductor manufacturing capacity is measured in packages per ~~month~~ year.

5. Exceptions should apply to affiliates

Consistent with 15 U.S.C. § 4652(a)(6)(C)(iii), the exceptions to the expansion clawback in the statute at 15 U.S.C. § 4652(a)(6)(C)(ii) should apply to affiliates of the funding recipient. The Proposed Rule, however, does not expressly apply the exceptions to affiliates. To make the exception meaningful, and consistent with the statute, the exceptions should apply to the funding recipient and its affiliates.

Recommended change to §231.202(a)(1) Scope

"(1) A funding recipient or its affiliates' existing facilities or equipment for manufacturing legacy semiconductors that exist on the date of the award…"

6. Commerce should have flexibility in implementing the expansion clawback

The regulations should provide Commerce with flexibility in implementing the expansion clawback to tailor restrictions to the circumstances surrounding the funding entity. The CHIPS Act states that a covered entity may not engage in certain transactions "as defined in the agreement" involving the expansion of semiconductor manufacturing capacity in foreign countries of concern. 15 U.S.C. 4652(a)(6)(C)(I). In addition, the legislation provides the Secretary with broad discretion in carrying out the CHIPS Act, including agreements "as may be necessary and on such terms as the Secretary considers appropriate." 15 U.S.C. 4659. These provisions provide Commerce with flexibility in carrying out the Act, such as having discretion to tailor requirements based on the circumstances of an individual funding entity.

C. Revisions to the definition of legacy semiconductor

1. Clarify that certain legacy 3D integration techniques are still "legacy semiconductors"

As SIA expressed to Commerce in its November 2022 response to the CPO Request for Information on Implementation of the CHIPS Incentives Program:

> The Secretary should ensure the expansion clawback provisions are implemented in a manner that avoids unnecessary disruption to existing facilities in China while the U.S. works to diversify and bolster its semiconductor supply chain. Today, China remains an important player in manufacturing, packaging, logistics point, and end-device market for the global semiconductor ecosystem across virtually all segments. Many of these facilities support key products and customers around the world, and as such, disruption to their operations would have a significant negative impact on the firms operating these facilities, as well as the broader electronics ecosystem.

As written, the Proposed Rule may be interpreted as excluding from the definition of legacy semiconductors not only advanced 3D integration concepts, such as "through silicon vias" (TSV) and "through mold vias" (TMV), but also decades-old packaging techniques such as stacking two legacy die on top of each other using wire bonds and other older packaging techniques like clips, flip-chip, and bump connections. These techniques do not create the high bandwidth or functional density needed for advanced computing, AI, or communication applications. The definition of legacy semiconductor should be clarified to include packaging that stacks die on top of each other using wire bonds and to exclude more advanced 3D packaging techniques, like TSV and TMV, occurring in a foreign country of concern.

The CHIPS Act states that "legacy semiconductor" includes any legacy generation of semiconductor technology relative to the 28-nanometer generation or older for logic (15 U.S.C. 4652(a)(6)(A)(i)(I)(bb)). The 3D integration exception to the definition of "legacy semiconductor" should therefore be clarified such that mature node concepts like vertical integration of multiple legacy semiconductors into a single package using, for example, wire bonds, clips, flip-chip, bump connections, etc. are not excepted from the definition of "legacy semiconductors."

> Recommended change to §231.110(b)(3) Legacy semiconductor
>
> (3) For the purposes of packaging facilities, semiconductors packaged utilizing <u>advanced</u> three-dimensional (3D) integration<u>, such as by directly attaching one or more die or wafer, through silicon vias, through mold vias, or other advanced methods.</u>

2. Certain packaging activity should be considered legacy, regardless of node size

It is unclear whether facilities conducting die prep or sort and assembly test that receive 3D integrated silicon products from facilities outside of foreign countries of concern are considered "legacy." Assembly test manufacturing (ATM) is an important – yet lower-value – portion of the semiconductor manufacturing process. While the regulations specifically exclude from the definition of legacy facilities that package semiconductors utilizing 3D integration, many

operations in China perform assembly test, including general (non-3D) packaging. As such, the regulations should specifically include ATM that uses non-3D packaging in its operations in the definition of legacy semiconductor. Given that ATM is generally a back-end operation, with billions of dollars invested in pre-existing facilities, it is appropriate for these operations to be viewed under the definition of "legacy" unless they specifically perform advanced 3D integration in a foreign country of concern.

> Recommended addition of 231.110(a)(4) Legacy semiconductor
>
> (4) Notwithstanding (a)(1-3) above, packaging or other operations in assembly test plants that do not utilize 3D integration, under (b)(3) of this section, in their operations in a foreign country of concern."

3. Modify the definition of legacy semiconductor for logic

The CHIPS Act defines "legacy semiconductor" to include "28-nanometer generation or older" technology. 15 U.S.C. 4652(a)(6)(A)(i). The proposed language defines 28nm technology as having "a gate length of 28 nanometers." This language would improperly exclude from the definition of "legacy semiconductor" technologies using the planar transistor architecture that should be considered as the same 28nm generation technology.

> Recommended change to §231.110(a)(1) Legacy Semiconductor
>
> (1) A digital or analog logic semiconductor that is of the 28-nanometer generation (including 28-nanometer generation or older logic integrated circuits manufactured using a planar transistor architecture) or older ~~(*i.e.*, has a gate length of 28 nanometers or more for a planar transistor)~~;

D. Predominately Serves the Market of Concern

The CHIPS Act includes an exception for legacy facilities that predominantly serve the market of the foreign country of concern, and the Proposed Rule sets forth provisions attempting to implement this exception. The Proposed Rule defines a facility as predominantly serving the market of a foreign country of concern when 85 percent of the output of the facility are "incorporated into final products . . . that are used or consumed in that market," and requires funding recipients to provide documentation demonstrating that a particular facility meets this standard.

SIA noted in its submission to the November Request for Information by the CPO:[41]

> Unlike manufacturers of "ready-to-use" assembled products, semiconductor companies do not typically have comprehensive visibility on the geographic market of end use for their products. This is because they do not sell products directly to consumers but to

[41] Comments of the Semiconductor Industry Association (SIA) on the CHIPS Program Office Request for Information on Implementation of the CHIPS Incentives Program, 87 Fed. Reg. 61570 (Oct. 12, 2022), November 14, 2022 (Available at https://www.semiconductors.org/wp-content/uploads/2022/11/SIA-CPO-CHIPS-RFI-Response-11_14_22.pdf, page 20)

companies such as original equipment manufacturers (OEMs) and other device integrators, and are often sold and re-sold through a long chain of distributors. This makes it difficult, if not impossible, to follow each product to its ultimate user. Accordingly, the market for the output of semiconductor companies is determined by the demand of these large, downstream producers. In this context, serving the market of a given country means meeting demand in a given country for components to be delivered in that country. As a result, location of product shipment rather than location of end use should be the determining measure for market services. Supply chain investments, including in assembly, test, and packaging operations, have been made to align with the location of shipment.

The Merriam Webster definition of "predominant" is "being most frequent or common." Similarly, Black's Law Dictionary defines the term as that which is "greater or superior…to others which it is connected or compared." CPO should interpret the terms in §4652(a)(6)(C)(ii) with flexibility in order to allow operations vital to maintaining healthy supply chains for semiconductors.

As an alternative, SIA would recommend lowering the threshold for "predominately serves the market" to 70 percent. In light of the above difficulty for a manufacturer to determine where the finished product is consumed, funding recipients will likely afford themselves a substantial buffer to ensure compliance, likely in the 5-10 percent range, but in some cases up to 15 percent. Accordingly, the proposed 85 percent threshold, in practice, will be somewhere between 90-100 percent, which would exceed the level of a "predominately" standard. Accompanying this more reasonable threshold, SIA would suggest that Commerce accept "documentation" under §231.302(g) and information in the "statement" under §231.302(h) that is derived from a good faith inquiry by the funding recipient.

E. Improved and transparent timeline for notification review time

Under the Proposed Rule, funding recipients are required to submit a notification to the Secretary regarding any planned transaction for its existing operations, and Commerce may request additional information from the funding recipient. The current proposal, however, is too open-ended and fails to set forth any timeline for intermediate action by the Secretary prior to the initial determination by notifying the funding recipient that additional information will be requested. The result may be an inefficient and open-ended process that could disrupt proposed activities that are permissible under the CHIPS Act and the applicable regulations. To address these concerns, the Secretary should be required to review the notification and request additional information within 10 business days in order to allow the funding recipient to begin preparing to provide additional information as requested by the Secretary. Just as the Secretary is required to make initial determination within 90 days, the Secretary should be required to notify the funding recipient that additional information will be requested within a specified timeline.

Recommended change to §231.304(b) Initiation of review

(b) Upon receipt of a notification submitted pursuant to § 231.301, the Secretary will review the notification for completeness and may request additional information from the funding recipient <u>within 10 business days</u>. Once a notification is deemed complete, the

Secretary will initiate a review of the transaction, notify the funding recipient in writing following the initiation of review, and consult with the Secretary of Defense and the Director of National Intelligence.

F. Improving the process for mitigation of national security risks by including a mechanism for waiver in the required agreement

The Proposed Rule provides a mechanism by which "a funding recipient or its affiliate is planning to undertake or has undertaken a significant transaction that is in violation of [the expansion clawback]" may enter into an agreement with the Secretary to mitigate the risk to national security and/or waive the recovery of funds (§231.306). SIA supports the intent of this provision, but we have certain suggestions to improve its implementation.

The waiver provision currently applies only in the case of a planned or executed transaction that would trigger an expansion clawback. In order to allow Commerce and funding recipients to begin information sharing related to any planned transaction that has the *potential* to violate the expansion clawback, the Proposed Rule should be modified to allow for negotiation to mitigate national security risks at the time of the required agreement. This approach will allow funding recipients greater business planning to determine at the time of the required agreement which (if any) planned transactions may be subject to §231.306. Likewise, this will allow Commerce to up front prioritize economic and national security objectives by avoiding the scenario presented by §231.305(c)(4) where "the funding recipient must cease or abandon the transaction." This will also help to ensure a robust pool of CHIPS incentives applicants remain throughout the grant negotiation process.

Recommended change to §231.306 Mitigation of national security risks

If the Secretary, in consultation with the Secretary of Defense and the Director of National Intelligence, determines that a funding recipient or its affiliate is planning to undertake or has undertaken a significant transaction that is in violation of § 231.202, the Secretary may seek to take measures in connection with the transaction to mitigate the risk to national security. Such measures may include the negotiation of an agreement with the funding recipient to mitigate the risk to national security in connection with the transaction. The Secretary also may decide to waive the recovery of funds. <u>The Secretary may also negotiate in such an agreement with the funding recipient ways to mitigate the risk to national security in connection with a planned transaction that has the potential to violate §231.202.</u>

G. Consolidate review process between Treasury and Commerce on the recapture and expansion clawback

It is likely many funding recipients who receive incentives under the CHIPS Act will also be eligible for the advanced manufacturing investment credit, and such entities would be subject to duplicative prohibitions and competing review processes by both the Commerce and Treasury Departments. To minimize the burden on funding recipients and make more efficient use of governmental resources, Commerce and Treasury should grant enforcement authority to a single agency for those funding recipients who are also claiming the advanced manufacturing

tax credit. Imposing notification and review requirements at multiple agencies would be overly burdensome and time consuming, and result in duplicative agency reviews.

To reduce this duplication, SIA encourages Commerce to adopt guidelines similar to those of the Executive Order: Reorganization Plan No.4 of 1978[42] whereby the Secretary of Labor transferred certain enforcement authority for overlapping regulations to the Secretary of the Treasury. While both agencies still had an important role in oversight, the Executive Order allocated responsibilities of the various overlapping rules to a single agency. This action would be equally appropriate in instances where companies are receiving both a grant and claiming the tax credit and thus subject to the same restrictions. As the Proposed Rules are intended to be "harmonized with existing oversight and restrictions on these types of transactions imposed by the Export Administration Regulations (15 CFR parts 730 through 744)" (88 Fed. Reg. at 17445), streamlining the review of the recapture of advanced manufacturing tax credit with that of the expansion clawback under the Department of Commerce would be an efficient outcome.

Consolidating the enforcement of the prohibited activities and recapture of the advanced manufacturing tax credit would ease both the administrative and compliance burdens for those recipients and taxpayers utilizing both programs to increase U.S. semiconductor manufacturing capacity, while also resulting in a more efficient use of government resources. We encourage the Secretary to consider a similar approach to reduce duplication and ensure that these programs designed to encourage activity in the U.S. are fully utilized.

Similarly, in order to reduce excessive, duplicative, and/or unnecessary compliance and administrative burdens, the Department of Commerce and Department of the Treasury should allow for consistency in reporting and reciprocity of processes such as agreements to mitigate national security concerns and waivers of the recovery of funds under §231.306, as well as any audits. This will allow for cross-departmental coordination and reduce compliance burdens, as well as to avoid any potential misalignment between Commerce and Treasury.

Such a process would be similar to many regulatory processes currently in place around the federal government to ease the potential burden on grant and contract recipients:

- One federal agency (the "cognizant agency for indirect costs") approves the indirect rates for an entity that pursues grants at multiple federal agencies. 2 C.F.R. 200.1; 48 C.F.R. 42.003.
- One federal agency (the "cognizant agency for audit") is the audit agency for an entity that pursues grants at multiple federal agencies. 2 C.F.R. 200.513 ("the designated cognizant agency for audit must be the Federal awarding agency that provides the predominant amount of funding directly (direct funding)").
- One federal agency takes the lead on suspension and debarment matters for all federal agencies. 2 C.F.R. 180.620 ("when more than one Federal agency has an interest in a suspension or debarment, the agencies may consider designating one agency as the lead agency for making the decision.")
- One federal agency approves the novation of all the federal contracts of an entity that is sold by one private entity to another. 48 C.F.R. 42.1202.

[42] Available at https://www.dol.gov/agencies/ebsa/laws-and-regulations/laws/executive-orders/4#section5

II. Technology Clawback

The CHIPS Act prohibits a funding recipient or its affiliates from knowingly engaging in any joint research or technology licensing with a foreign entity of concern that relates to a technology or product that raises national security concerns (15 U.S.C. 4652(a)(5)(C)). Congress adopted this requirement to ensure that companies receiving CHIPS funding would not enable the technological capabilities of a foreign country of concern in a way that harms U.S. economic and national security by transferring critical know-how through joint research or technology licensing. SIA supports this goal and offers several suggestions to improve the proposed regulations implementing this requirement.

A. Improvements to the definitions of "joint research" and "technology licensing"

The proposed definition of "technology licensing" broadly covers "patents, trade secrets, or know how," potentially restricting normal business activities unrelated to national security.

In order to allow funding recipients to best comply with the technology clawback, the Department of Commerce should provide clarity on the type of technology transfers that are captured by the rule. The emphasis should be on agreements involving the transfer of critical technology or know-how and make it clear that customary business discussions that may include general technical information are outside the reach of the rule. Such customary business discussions often include technical information required to 1) optimize a semiconductor component with the rest of an end-system or consumer product's performance or cost, or 2) design a product for the funding recipient to sell to the foreign entity of concern, neither of which should be subject to the technology clawback. Commerce should provide a non-exhaustive list of the types of agreements or transactions that meet the definition and those that would not in order to provide additional distinction from the customary business discussions that occur when services and products are sold to customers.

As stated in the preamble, the Proposed Rule was designed to be "harmonized with existing oversight and restrictions on these types of transactions imposed by the Export Administration Regulations (15 CFR parts 730 through 744)" (88 Fed. Reg. at 17445). Export control licensing is the established mechanism for determining permissible technology and should remain the leading review function. Thus, Commerce should provide clarity on how the technology clawback would interact with existing export licenses for the 26 items listed in Category 3 of the Commerce Control List (supplement no. 1 to part 774 of the Export Administration Regulations, 15 CFR part 774) that are controlled for National Security reasons, as described in 15 CFR 742.4, or Regional Stability reasons, as described in 15 CFR 742.6, such as whether existing approved licenses from the Bureau of Industry and Security would be grandfathered in.

1. Patents should be excluded from the technology clawback

The proposal defines "technology licensing" to include, among other things, the licensing of patents. The inclusion of patents will unnecessarily impede ordinary business transactions that are essential to the semiconductor ecosystem and the protection and monetization of intellectual property. For example, semiconductor companies routinely engage in the cross licensing of patents to avoid patent disputes and costly litigation. Semiconductor companies

also actively participate in international standards bodies, which are essential for interoperability and the overall development of technology, sometimes resulting in codification of standard essential patents (SEPs) in a standard, which are licensed on "fair, reasonable, and nondiscriminatory" (FRAND) terms. Where disputes over patents arise, companies routinely enter into license agreements covering patented technology as a means of avoiding or settling litigation. These and other similar and related practices are routine and happen every day in the semiconductor industry. Patents are published documents, and therefore, the invention in a patent is already available and known to entities in a foreign country of concern. Restricting patent licensing fails to advance what would be a sound policy goal – the transfer of know-how relating to national security – and instead significantly disrupts normal business activities and puts funding recipients at a strategic disadvantage in litigation. Therefore, the proposed definition of "technology licensing" should be revised to exclude patent licensing from the technology clawback.

2. Allow funding recipients to engage in patent cross-licenses

If the definition of technology licensing continues to include patents, the definition should, at minimum, be amended to allow funding recipients to engage in broad patent cross-licenses.

To ensure business as a whole has freedom to operate without costly disruption, including bringing funded products to market, a U.S. company may need to grant patent licenses, including a broad cross-license to a patent portfolio, with a foreign entity of concern (which may own relevant patents) to receive reciprocal assurances sufficient to protect its business. The sale of a product or service provides an implied license to customers, usually referred to as "patent exhaustion"; thus, the current definition of "technology licensing" creates additional concern with otherwise routine and permissible commerce.

Additionally, the proposed technology guardrail fails to appreciate that in the semiconductor sector, as in many industries, the patent rights necessary to commercialize a product are frequently controlled by multiple rights holders and that bringing technology to market may well require negotiation and entering into patent cross-license agreements with foreign entities of concern.

When patent rights are fragmented, bringing a product to market requires negotiating with the multiple parties that hold rights to the different segments of technology and entering into portfolio cross licenses and patent pools to reduce the uncertainty and risk of infringement suit. By prohibiting without exception funding recipients from engaging with a foreign entity of concern in such patent cross-license agreements, the Proposed Rule risks undermining a core vision of the incentives program by investing in the research and development of technologies that cannot, in practice, be brought to market for the benefit of the U.S. or our allies. Moreover, amendments to the technology clawback are necessary to ensure that U.S. companies are not forced to choose between accepting CHIPS grant funding or protecting themselves against patent claims from litigious companies.

To remedy these shortcomings, we recommend excluding agreements that grant only patent rights, in which no technology or know-how is transferred to a foreign entity of concern beyond the publicly available information in the published patent.

3. Allow for participation in international collaborative efforts such as standards organizations

Additionally, Commerce should provide clarification regarding the transfer of know-how in standards development organizations with the intent of the information ultimately being published or made available in research consortia settings, including but not limited to instances where the funding recipient is unable to restrict the participants of the research consortia setting.

By failing to include exceptions in the technology guardrail for international collaborative efforts in standards organizations and in fundamental research activities, the technology guardrail weakens opportunities for U.S. leadership in the global semiconductor sector, which requires that U.S. entities have a seat at the table for standard setting discussions The Administration's recently announced National Standards Strategy for Critical and Emerging Technology[43] emphasizes the importance of U.S. leadership in standards setting in critical technologies, which relies on the ability of funding recipients to fully participate and lead in standards-setting bodies. While SIA supports the strategy's effort to "enhance U.S. government and like-minded nations' representation and influence in international standards governance and leadership," realizing such objective is dependent on "robust standards governance process" involving U.S. companies and, in some cases, foreign entities of concern.[44] The regulations should be revised to ensure that CHIPS grant funding recipients will not be penalized by preventing them from engaging in international standards bodies. A number of funding recipients are likely to be technology leaders who are critical to standardizing technology for the benefit of global and U.S. consumers.

Many entities that would meet the definition of "foreign entities of concern" are members of international standards setting organizations in the semiconductor space. As we have learned from the past several years of U.S. unilateral restrictions on U.S. companies participating in standard organizations with companies on the Entity List, international standards organizations will not exclude non-U.S. participants based on unilateral U.S. restrictions.[45] Furthermore, restricting which companies may participate in standards organizations puts U.S.-based standards development organizations at a disadvantage versus those located outside of the U.S.

Additionally, in a recent rulemaking, the Commerce Department's Bureau of Industry and Security (BIS) aptly described the risk of interfering with U.S. industry participation in such groups:

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[43] The White House, Fact Sheet: Biden-Harris Administration Announces National Standards Strategy for Critical and Emerging Technology, May 2023 (*Available at* https://www.whitehouse.gov/briefing-room/statements-releases/2023/05/04/fact-sheet-biden-harris-administration-announces-national-standards-strategy-for-critical-and-emerging-technology/)

[44] The White House, United States Government National Standards Strategy For Critical And Emerging Technology (*Available at* https://www.whitehouse.gov/wp-content/uploads/2023/05/US-Gov-National-Standards-Strategy-2023.pdf)

[45] Comments of the Semiconductor Industry Association (SIA) on Amendment to Prohibitions Pertaining to the Release of Technology to Standards Organizations Members that are on the Entity List (85 Fed. Reg. 36719 (June 18, 2020). August 17, 2020. (*Available at* https://www.semiconductors.org/wp-content/uploads/2020/08/081420.SIA_.standards.reg_.comment-SIA-Final1.pdf)

> Any impediment to U.S. influence in standards development forums is a national security threat to the United States because not only does it limit U.S. leadership in standards development, but other countries are already racing to fill this vacuum with their own leadership and standards. In many cases, this ceding of U.S. leadership not only undermines democratic values and U.S. national security and foreign policy interests, but it also contributes to a potential future global standards environment that actually works to oppose U.S. interests.[46]

For this reason, BIS amended the Export Administration Regulations (EAR) to authorize the release of specified items subject to the EAR without a license, including to Entity Listed parties, when that release occurs in the context of a "standards-related activity." The BIS rule provides a definition that could be readily adapted by NIST and incorporated into a "release" from the current technology guardrail rule.

4. Allow for the continued sharing of design fabrication or packaging files

In the global semiconductor industry some companies outsource fabrication and/or packaging operations to foundries and OSATs, and in doing so they may make available IP (such as a design file) to manufacturing partners. Under the proposal, such activities could be construed as transferring know-how to a foreign entity of concern, even if it does not involve the manufacturing of semiconductors critical to national security. The final regulation should clarify that the sharing of information, such as design files for fabrication and packaging as part of an outsourced manufacturing agreement, is not covered by the technology clawback.

5. Allow for intracompany transfer agreements

As proposed, the technology licensing definition may restrict funding recipients from entering into intracompany intellectual property license and transfer agreements with their affiliates, or vice versa. This has potentially wide-reaching impact for companies that utilize the well-accepted corporate practice of holding and managing intellectual property in a single entity to enable their global R&D efforts. These internal transfers and intraparty agreements are common, routine agreements and are often designed to protect intellectual property that is owned in the U.S. The proposal should be revised to allow for transfer agreements between a funding recipient and its affiliates, or between or among its affiliates.

6. Ensure general sales of parts are not prohibited

The prohibition at §231.203 on technology licensing "with a foreign entity of concern that relates to a technology or product that raises national security concerns" when combined with the definition of "technology licensing" (§231.123) could be interpreted to prohibit the sale of equipment and parts that are generally used for semiconductor manufacturing. Each part and piece of equipment sold for semiconductor manufacturing is sold with an explicit or implied license to use the intellectual property underlying the part or equipment. Under the Proposed

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[46] *See BIS, Interim Final Rule, Authorization of Certain "Items" to Entities on the Entity List in the Context of Specific Standards Activities, 87 FR 55241, Sept. 9, 2022.*

Rule, the license to use a part or equipment that is part of a sale would fall within the definition of "technology licensing" at §231.123. Because a semiconductor part or equipment could potentially be used to manufacture any semiconductor, including technology or products that raise national security concerns or are "related" to such technology or products, basic sales appear to be prohibited.

7. Ensure warranty, service, and support are not prohibited

Upstream equipment manufacturers have different business models, approaches to research and development, and needs for technology licensing than semiconductor manufacturers. Manufacturers of equipment and tooling spend exhaustive resources on ensuring that machinery and tools supplied to semiconductor manufacturers are operational, work as intended and are repaired as needed. The business involves not only the actual manufacturing of equipment and tooling, but critical service, warranty, and support components. Generally, semiconductor manufacturers do not have this element to their business model. For equipment manufacturers, unlike semiconductor manufacturers, the definition of "research and development" at 15 U.S.C. § 638(e)(5)(C) as incorporated into the Proposed Rule at §231.108 could prohibit ongoing warranty, service and support for customers of a funding recipient. Under the statutory definition, research and development includes the "systematic application of knowledge toward the production of useful materials, devices, and systems or methods, including design, development, and improvement of prototypes and new processes to meet specific requirements." *Id.* Warranty, service, and support that may "relate to a technology or product that raises national security concerns" should not be considered to be prohibited "joint research."

8. Allow manufacturers to "design-in" their devices into the customers' end products

Finally, Commerce should provide clarification regarding what, specifically, "research" and "jointly undertaken" mean. Semiconductor companies typically engage in normal sales activities with their customers to "design-in" their devices into the customers' end products. These discussions can involve technical matters; exchange of data including product features, product reliability, and product limitations; and consideration of alternative semiconductor products to optimize the end system's performance and cost. These standard commercial exchanges could erroneously be characterized as "a systematic application of knowledge toward the production of useful materials, devices, and systems or methods, including design, development, and improvement of prototypes and new processes to meet specific requirements" and thus be considered research under 15 U.S.C. 638(e)(5). Commerce should clarify that research, development, or engineering carried out by a funding recipient together with its customer to establish or apply a drawing, design, or related specification for the funding recipient's product is not "joint research" for purposes of the clawback provision.

Similarly, Commerce should clarify these terms to avoid this outcome in the technology licensing context by permitting disclosures of process and assembly design kits, complex design intellectual property, or foundational design intellectual property provided by a funding recipient or its affiliates to its customer solely for the design of semiconductors to be manufactured by the funding recipient or its affiliates.

9. Collaboration between equipment manufacturers and other upstream suppliers should be protected

Equipment manufacturers must work collaboratively across many countries with other upstream suppliers to ensure that chemicals and materials from specific suppliers will work as intended with semiconductor manufacturing equipment. When a semiconductor manufacturer purchases chemicals and materials necessary for manufacturing, that supply must be tested and evaluated for use on the specific manufacturing equipment. That evaluation and testing is done by the equipment manufacturer in coordination with the specific chemical and material suppliers that will be used by the semiconductor manufacturer. This effort involves not only joint research and development, but also project-specific technology licenses that are given by the equipment manufacturer to the supplier for the purposes of research and testing using the manufacturing equipment. Without these collaborations, delivered semiconductor manufacturing equipment would not work as intended with specific chemicals and materials suppliers and the cost of ownership of semiconductor manufacturing equipment would significantly increase. The definition of "research and development" at 15 U.S.C. §638(e)(5)(C) as incorporated into the Proposed Rule at §231.108 and the definition of "technology licensing" at §231.123 could each individually prohibit ongoing collaborations between equipment manufacturers that receive CHIPS Act funds and other upstream suppliers. These prohibitions would effectively halt the collaboration among upstream suppliers.

10. Consolidated proposed revisions to technology licensing and joint research

To implement the suggestions set forth above in Sections II.A.1 through 9 of this paper, we recommend the following additions to §231.123 Technology licensing:

(a) A contractual agreement in which one party's ~~patents,~~ trade secrets~~,~~ or know-how are sold or made available to another party;

(b) Notwithstanding paragraph (a) of this section, the following is not technology licensing:

(1) Design fabrication or packaging files made available to another party through a contractual agreement in connection with semiconductor fabrication or packaging services, except for any intellectual property that is related to any item listed in Category 3 of the Commerce Control List (supplement no. 1 to part 774 of the Export Administration Regulations, 15 CFR part 774) that is controlled for National Security ("NS") reasons, as described in 15 CFR 742.4, or Regional Stability ("RS") reasons, as described in 15 CFR 742.6, or related to semiconductors critical to national security.

(2) Licensing or transfer agreements conducted exclusively between a funding recipient and its affiliates, or between or among a funding recipient's affiliates;

(3) A standards-related activity (as such term is defined in 15 CFR Part 772);

(4) Agreements that grant patent rights only with respect to "published information" (as that term is defined in 15 C.F.R. § 734.7) and no proprietary information is shared;

(5) An implied or general intellectual property license relating to the use of a product that is sold by a funding recipient or its affiliates;

(6) Licensing related to collaborations between semiconductor equipment manufacturers and other semiconductor manufacturing suppliers for the purpose of testing, evaluation, development and reducing the cost of ownership of semiconductor manufacturing equipment;

(7) Disclosures of a process or assembly design kit, complex design intellectual property, foundational design intellectual property, or other technical information provided by a funding recipient or its affiliates to its customer solely for the design of integrated circuits to be manufactured by the funding recipient; and

(8) Information that is generally available to the public or published (as such term is defined at 15 C.F.R. § 734.7).

To implement the changes set forth above, we recommend the following additions to §231.108 Joint research

(a) *Joint research* means any research and development activity as defined at 15 U.S.C. 638(e)(5) that is jointly undertaken by two or more persons, including any research and development activities undertaken as part of a joint venture, as defined at 15 U.S.C. 4301(a)(6).

(b) Notwithstanding paragraph (a) of this section, the following is not joint research:

(1) A standards-related activity (as such term is defined in 15 CFR Part 772);
(2) Research and development conducted exclusive between a funding recipient and its affiliates;

(3) Research, development, or engineering related to a manufacturing process for an existing product;

(4) Research, development, or engineering involving two or more persons in order to establish or apply a drawing, design, or related specification for a product to be purchased and sold between or among such persons;

(5) Warranty, service, and customer support performed by a funding recipient;

(6) Collaborations between semiconductor equipment manufacturers and other semiconductor manufacturing suppliers for the purpose of testing, evaluation, development and reducing the cost of ownership of semiconductor manufacturing equipment; and

(7) Information that is generally available to the public or published (as such term is defined at 15 C.F.R. § 734.7)

B. Improvements to the implementation of the technology clawback

1. Provide greater clarity on the phrase "relates to" national security

Both the CHIPS Act and the Proposed Rule prohibit joint research and technology licensing with a foreign entity of concern that "relates to" a technology or product that raises national security concerns. Congress used this broad language to ensure that technology relevant to national security would not be transferred to a foreign country of concern. The Proposed Rule provides no specific definition of the term "relates to," and relying on its common use definition, which is very broad, provides insufficient clarity for funding recipients or their affiliates to reasonably identify the activities in scope of the rule. We acknowledge that what "relates to" one of the technologies or products that raise national security concerns is difficult to define with precision, but without further clarity, companies will lack sufficient notice of prohibited activities.

The term "related to," in common use, means to be about or connected with something. In the context of the technology clawback, this means the Proposed Rule would prohibit joint research or technology licensing activities "about or connected with" any technology or product that raises national security concerns. This would cover not only joint research or licensing of technology controlled for national security or regional stability reasons under 26 ECCNs in Category 3 of the EAR for export to the foreign entities of concern, but also of more general information, including well-known semiconductor concepts that are published and freely available to the general public, as well as concepts that are shared between mature stage products and technology and the more sensitive and advanced items described in the definition of "technology or product that raises national security concerns." The phrase "relates to" could also implicate joint research and technology licensing that would not conventionally be considered related to one of the technologies or products that raise national security concerns, but could indirectly have some relation due to shared information, components, or technology that are not specific to a specific technology or product.

2. Addition of a process to mitigate national security risks

The Proposed Rule should be revised to include a process to mitigate national security risks associated with the technology clawback, similar to §231.306 for the expansion clawback. While Congress did not expressly require a process to mitigate national security risks as part of the technology clawback, the inclusion of such a provision would be consistent with Congressional intent. First, 15 U.S.C. §4652(a)(5)(C)(ii) states that the Secretary may determine whether joint research or technology licensing effort with a foreign country of concern relates to a technology or product that raises national security concerns. Similarly, such a determination must be communicated to the covered entity before engaging in such joint research or technology licensing. Such an approach is important for business predictability, as reflected by SIA's comments on the mitigation of national security risks for the expansion clawback (I.F.).

Recommended addition of §231.124(c) Technology or product that raises national security concerns:

> (c) If the Secretary, in consultation with the Secretary of Defense and the Director of National Intelligence, determines that a funding recipient or its affiliate is planning to engage or has engaged in any joint research or technology licensing with a foreign entity

of concern that relates to a technology or product that raises national security concerns that is in violation of § 231.203, the Secretary may seek to take measures in connection with the joint research or technology licensing to mitigate the risk to national security. Such measures may include the negotiation of an agreement with the funding recipient to mitigate the risk to national security in connection with the joint research or technology licensing. The Secretary also may decide to waive the recovery of funds. The Secretary may also negotiate in such an agreement with the funding recipient ways to mitigate the risk to national security in connection with joint research or technology licensing that has the potential to violate §231.203.

3. Limit the technology clawback to the term of the federal financial assistance award.

The CHIPS Act specifies that the technology clawback should be effective "during the applicable term with respect to the award" (15 U.S.C. § 4652(a)(5)(C)). Contrary to the express terms of the statute, the Proposed Rule requires the technology clawback to be included as part of the 10-year duration of the expansion clawback.

This discrepancy should be remedied by differentiating that there are two applicable terms, one for the expansion clawback and one for the technology clawback.

Recommended change to §231.102 Applicable term

(a) For ~~both~~ the prohibition on certain expansion transactions ~~and the prohibition on certain joint research or licensing transactions~~, the applicable term shall be the 10 years following the date of the award of Federal financial assistance, unless otherwise specified in the required agreement.

(b) For the prohibition on certain joint research or licensing transactions, the applicable term shall be the duration of the award, unless otherwise specified in the required agreement.

4. Allow for reasonable continuation of pre-existing contracts or arrangements

The preamble to the Proposed Rule states:

> The Department recognizes that some funding recipients may have pre-existing contracts or other arrangements which commit them to joint research or technology licensing with foreign entities of concern that relate to a technology or product that raises national security concerns. CPO invites comments from interested parties on the extent and nature of these pre-existing arrangements, the ability of funding recipients to abandon them with or without penalty, and the feasibility and impact of exempting joint research or technology licensing done pursuant to an agreement which predates this rule. (88 Fed. Reg. at 17441).

We appreciate Commerce's recognition of pre-existing activities and the complexities associated with addressing these activities. To address this issue, the technology clawback

should apply prospectively only and be triggered only by contracts or other arrangements, or applicable modifications to contracts or arrangements, entered into after the required agreement. This approach is consistent with the statutory language of the CHIPS and Science Act; 15 U.S.C. 4652(a)(5)(C) states that the clawback only becomes operative if national security concerns with specific joint research or a technology license are "communicated to the covered entity *before* engaging in such joint research or technology licensing" (emphasis added).

Applying the technology clawback retroactively, where a funding recipient entered into an agreement with a foreign entity of concern several years before the existence of the CHIPS Act, would add complexity associated with unwinding such arrangements. Moreover, Chinese counterparties presumably have already obtained any know-how regarding a potential technology of concern, and the coverage of pre-existing agreements merely places a potential funding recipient in legal and financial jeopardy.

In addition, the premature termination of joint research and technology agreements strips away the intellectual property protection mechanisms in the agreements and leaves a grant recipient even more exposed to intellectual property misappropriation. It would also be extremely difficult, and in some cases near impossible, for funding recipients to abandon many pre-existing license agreements. Contract law generally does not permit a party to void a contract or the licenses granted under the contract unless there is an applicable termination provision in the contract. It is unlikely that there will be a provision that allows termination in the situation addressed by the proposed regulations. The funding recipient would have no leverage that would allow them to convince a foreign entity to renegotiate the terms of a pre-existing license.

Commerce should also consider the potentially widespread nature of pre-existing contracts, and accordingly, the potential for compliance burdens and confidentiality issues.

Rather than prohibiting existing, current, and ongoing arrangements, we suggest Commerce should require disclosure of general categories of applicable arrangements and require that the arrangement is not expanded or extended beyond its current terms. The Secretary, in consultation with the Secretary of Defense and the Director of National Intelligence, may then determine whether an extension or expansion of such arrangement raises national security concerns and provide an opportunity for funding recipients to mitigate such concerns.

5. Owned by, controlled by, or subject to the jurisdiction or direction of. (§231.112)

It is not clear from § 231.112(b)(1) if "located in the foreign country" modifies "resident of the foreign country" or modifies "citizen, national, or resident of foreign country." As a result, a funding recipient could be prohibited from sharing technology with all Chinese citizens in all parts of the world, which may be unintended.

Additionally, because of § 231.112, the definition of "Foreign Entity of Concern" in § 231.106(c) becomes overly broad. The effect of this is that the Proposed Rule unrealistically includes all Chinese citizens and companies "subject to the jurisdiction" of PRC to fall in the scope of "foreign entity of concern." Given the use of the term "foreign entity of concern" in the prohibition on certain joint research or technology licensing in §231.203, even very routine and necessary

business activity could be blocked. This is an integral part of the day-to-day functioning of the industry. Licensing (including implied and other non-controversial low-level licensing) and joint assessment (i.e. research) of technical issues associated with customer applications pervades almost every aspect of dealings between semiconductor companies, their suppliers and customers. To forbid any such "licensing" or "joint research" with all Chinese citizens and companies, regardless of their connections to government-owned entities, creates a compliance burden that cannot be met and which is probably not intended. Additionally, Commerce should consider the effect on companies based in the U.S. and allied countries that are not funding recipients but that have subsidiaries or affiliates that are organized under the laws of a foreign country of concern or has its principal place of business in the foreign country of concern.

The proposed change below will address the aforementioned issues because it provides consistency by references to the same language pertaining to a foreign entity in §231.105(b)(2-3). SIA also encourages alignment with export controls with respect to restricted entities in order to set a reasonable, practical, and consistent scope for compliance on that issue within the Department's jurisdiction.

> Recommended change to §231.112(b)(1) Owned by, controlled by, or subject to the jurisdiction or direction of
>
> (1) The person acts as an agent, representative, or employee, or any person who acts in any other capacity, at the order, request, or under the direction or control, directly or indirectly, of a government of a foreign country ~~is a citizen, national, or resident of the foreign country located in the foreign country~~;

At a minimum, the definition should be amended to ensure that all citizens of a foreign country of concern located outside the foreign country of concern are not covered by the joint research and licensing prohibition. It is not clear from § 231.112(b)(1) if "located in the foreign country" modifies "resident of the foreign country" or modifies "citizen, national, or resident of foreign country." As a result, a funding recipient could be prohibited from sharing technology with all Chinese citizens in all parts of the world. For example, there may be Chinese doctoral or master's students at U.S. universities, or Chinese-American dual citizens employed by U.S. semiconductor companies, that are inadvertently subject to the restriction. The restriction should exclude persons located outside the foreign country of concern, unless §231.112(b-c) apply.

> Alternative recommended modification to § 231.112(b)(1):
>
> "The person is located in the foreign country and is a citizen, national, or resident of the foreign country or another foreign country of concern ~~located in the foreign country~~."

Additionally, while already implied, Commerce should confirm that affiliates of a funding recipient are not considered foreign entities of concern.

> Recommended addition to the end of § 231.106 Foreign entity of concern.
>
> (g) Notwithstanding paragraphs (a-f) of this section, the following is not a foreign entity of concern:

(1) The funding recipient and its affiliates; or

(2) An entity, as determined by the Secretary, in consultation with the Secretary of Defense and Director of National Intelligence.

III. Additional Topics

A. Semiconductors critical to national security (§231.120)

The definition of "semiconductors critical to national security" includes an expansive range of semiconductor categories. We request Commerce refine the definition to more narrowly target the universe of impacted technologies.

1. Compound Semiconductors & Wide/Ultra-wide bandgap semiconductors

While some compound semiconductor technologies are properly deemed as critical to national security under §231.120, including those already subject to export controls, other compound semiconductors are primarily used in commercial applications, including those intended for sale in renewable energy, energy storage, lighting, electric vehicle, power supplies for servers, or wireless infrastructure applications.

For example, certain compound semiconductor products are used in wireless infrastructure would be covered, including products supporting base stations. Many of these products and technologies are classified as EAR99 or subject to only Anti-Terrorism controls (e.g., 5A991) in the Export Administration (EAR) Regulations, meaning that they are not subject to any export licensing requirements to China as a general matter. Restricting core elements of wireless infrastructure using technology with no export restrictions and are freely available in foreign countries of concern impacts companies seeking CHIPS incentives. It also creates inconsistencies and establishes conflicting requirements for those same items by defining them as "technology or product that raises national security concerns" or "semiconductors critical to national security" when those same products are not subject to National Security controls in the EAR.

For example, SiC power semiconductors such as those used to invert Direct Current (DC) from a solar panel to Alternating Current (AC) for transmission over power lines, or to invert AC from the power lines to DC to charge an Electric Vehicle (EV) battery, or to invert the DC from the EV battery to an AC for the EV's traction motor, are commercial applications that further U.S. climate change mitigation goals, are EAR99 as a general matter and should not be considered a national security concern by inclusion in a broader compound or wideband gap semiconductor category.

2. Packaging fully depleted silicon on insulator (FD-SOI) semiconductors

While SIA recognizes Commerce's objective to limit the manufacturing and knowledge transfer as it relates to FD-SOI, SIA does not believe the same national security objectives are met with respect to the packaging of such technology. Packaging operations used for such devices are not appreciably different than that used for other types of semiconductors and thus should be excluded. However, advanced packaging of FD-SOI should remain covered.

> Recommended change to §231.120(e) Semiconductors critical to national security
>
> (e) fully depleted silicon on insulator (FD-SOI) semiconductors other than with regard to semiconductor packaging operations with respect to such semiconductors of a 28-nanometer generation or older;

3. Radiation-hardened by process (RHBP) semiconductors

The inclusion of "Radiation-hardened by process (RHBP) semiconductors" on the list of semiconductors critical to national security requires additional clarification and definition. As the semiconductor fabrication process technologies have advanced, the integrated circuits produced from the standard commercial process technology have become naturally more radiation resistant in certain respects and more susceptible to radiation effects in other respects. "Radiation-hardened by process" has traditionally meant that special steps were taken in the process technology to enhance the radiation resilience of the products, such as introducing different substrate materials.[47] Radiation hardening can also occur during design. Commerce should work with industry to clarify the coverage of this provision.

B. Affiliate (§231.101)

The definition of affiliate in §231.101 uses a 50 percent threshold. This is a departure from the reference in the statute to an 80 percent threshold (15 U.S.C. 4652(a)(6)(C)(iii)):

> For the purpose of applying the requirements in an agreement required under clause (i), a covered entity shall include the covered entity receiving financial assistance under this section, as well as any member of the covered entity's affiliated group under section 1504(a) of title 26, without regard to section 1504(b)(3) of title 26.

[47] Chinna, Rao & Chavan, Ameet. (2021). Review on Radiation Hardness Assurance by Design, Process and NextGen Devices. Journal of Physics: Conference Series. 1916. 012002. 10.1088/1742-6596/1916/1/012002. (*Available at* https://www.researchgate.net/publication/351937516_Review_on_Radiation_Hardness_Assurance_by_Design_Process_and_NextGen_Devices)

26 U.S.C. §1504(a) maintains an 80-percent voting and value test under 26 U.S.C. 1504(a)(1-2). The Department of Commerce should therefore revise the definition to align with Congressional intent.

Recommended change to §231.101 Affiliate

Affiliate means~~:~~ any member of the funding recipient's affiliated group under section 1504(a) of title 26, without regard to section 1504(b)(3) of title 26, under 15 U.S.C. 4652(a)(6)(C)(iii).

~~(a) Any subsidiary of the funding recipient, *i.e.*, any entity in which the funding recipient directly or indirectly holds at least 50 percent of the outstanding voting interest;~~

~~(b) Any parent entity of the funding recipient, *i.e.*, any entity that directly or indirectly holds at least 50 percent of the outstanding voting interest in the funding recipient; or~~

~~(c) Any entity in which the funding recipient's parent entity or parent entities directly or indirectly hold at least 50 percent of the outstanding voting interest.~~

C. Clarify intended application scope to exclude customers, clients, vendors, suppliers, and subcontractors

Commerce should add a declarative statement that clawbacks under the Proposed Rule are applied to the funding recipient and its affiliates, with clarifications sought above, but not to the subcontractors, customers, vendors, suppliers, or clients of the recipient and its affiliates. This is necessary to ensure clarity that recipients are not required to attempt to flow-down guardrails obligations to partners or clients that are not entities of concern.

IV. Publication of Frequently Asked Questions for Equipment and Materials Manufacturers

Given the unique nature of semiconductor equipment and materials manufacturers as compared to semiconductor manufacturers, many potential issues related to a Final Rule may simply not be capable of being addressed in a rule intended to regulate both sets of industries. As a result, we urge the Department to confirm that equipment and materials manufacturing are not considered "semiconductor manufacturing" for purposes of this Rule, as well as to consider the publication of FAQs or other guidance to clarify the application of this Rule as applied to equipment and materials manufacturers who may be funding recipients.

V. Technical corrections

A. Foreign entity of concern (§231.106)

There appears to be an error on the labeling of the subsections (b)-(e). This should read as subsections (e)-(h).

B. Scope (§231.201)

Insert "significant" to now read: "…for review by the Secretary of a significant transaction…"

C. Retention of Records (§231.204)

As proposed, the retention of records provision inadvertently requires record retention on all significant transactions, which, over the duration of the applicable term, with a threshold of $100,000 could number in the millions across all funding recipients. The provision also does not limit record retention to those significant transactions taking place in foreign countries of concern, instead requiring record retention of global significant transactions. This is an extraordinary, and likely unintended, compliance burden.

Instead, the retention of records provision should only apply to significant transactions involving the material expansion of semiconductor manufacturing capacity in a foreign country of concern. The provision should be limited in scope and to the same effect in line with the intention for record-keeping and for practical compliance effort. This will also be consistent with §231.301.

Recommended change to §231.204(a) Retention of records

(a) During the 10-year period beginning on the date of the Federal financial assistance award under 15 U.S.C. 4652 and for a period of seven years following any significant transaction involving the material expansion of semiconductor manufacturing capacity in a foreign country of concern, a funding recipient or its affiliate planning or engaging in ~~any~~ such significant transaction shall maintain records related to the significant transaction in a manner consistent with the recordkeeping practices used in their ordinary course of business for such transactions.

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SIA appreciates the opportunity to comment on this proposal and we look forward to continuing to work with Commerce in the development and implementation of these rules.