PFAS-Containing Fluorochemicals Used in Semiconductor Manufacturing Plasma-Enabled Etch and Deposition

Semiconductor PFAS Consortium Plasma Etch and Deposition Working Group

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This publication was developed by the Semiconductor PFAS Consortium plasma etch and deposition technical working group. The contents do not necessarily reflect the uses, views or stated policies of individual consortium members.

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About the Semiconductor PFAS Consortium

The Semiconductor PFAS Consortium is an international group of semiconductor industry stakeholders formed to collect the technical data needed to formulate an industry approach to perfluoroalkyl and polyfluoroalkyl substances (PFAS).

Consortium membership comprises semiconductor manufacturers and members of the supply chain, including chemical, material and equipment suppliers. The consortium includes technical working groups, each focused on the:

- Identification of PFAS uses, why they are used, and the viability of alternatives.
- Application of the pollution prevention hierarchy to (where possible) reduce PFAS consumption or eliminate use, identify alternatives, and minimize and control emissions.
- Development of socioeconomic impact analysis data.
- Identification of research needs.

This data will better inform public policy and legislation regarding the semiconductor industry’s use of PFAS-containing materials and will focus research and development efforts. The Semiconductor PFAS Consortium is organized under the auspices of the Semiconductor Industry Association (SIA). For more information, see www.semiconductors.org.

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Executive Summary

Given increased awareness of the vulnerability of semiconductor supply chains, global interest in bolstering semiconductor manufacturing has increased. Ramping up manufacturing efforts would necessitate an increase in the use of certain fluorochemicals, however, which are essential for operations and industry competitiveness.

There are ongoing legislative and regulatory efforts worldwide to categorize many fluorinated chemistries as PFAS-containing materials, and to consequently restrict their usage. However, these efforts suffer from the fact that there are currently disparate definitions of “PFAS,” all of which are structural in nature and do not address differences in persistence, bioaccumulation and toxicity between various fluorinated compounds.

In this white paper, we will look at three specific semiconductor manufacturing processes – plasma (dry) etching, thin-film deposition and chamber cleaning – and make the case that the use of fluorochemicals in these fields fits the definition of essential use: “necessary for highly important purposes for which alternatives are not yet established.” We will provide a high-level overview of the role of fluorocarbon chemistry in enabling innovation and reproducibility in silicon-based computing technologies over the last 30 years. In doing so, we will also illustrate the significant impact of restricting PFAS usage in this industry and the challenges in developing alternatives.

1.0 Introduction

Computing technology has made an indelible impact on all facets of society. From enabling precise, high-volume manufacturing in globe-spanning industries to making vast reserves of information available to a single individual via the internet, it is hard to overstate the importance of computers to modern life. Most recently, enormous performance gains in mobile computing and the consequent proliferation of data generated by networks of such machines have enabled the ongoing Fourth Industrial Revolution.

The general population has become more accustomed to and reliant on the conveniences that the internet provides. This was extremely apparent during the COVID-19 pandemic, as remote work, telehealth and other services were in high demand. These advances could not have been possible without proportionally immense innovations in the field of semiconductor manufacturing. In essence, each successive generation of computing technology has seen dramatic increases in the complexity of the logic, memory and interconnects that constitute semiconductor devices.

To meet computational demands, semiconductor devices have become more complex over the years, first by downscaling the lateral footprint of their features and later by shifting to vertical integration (increasing the number of layers in each device) (Wong, et al. 2020). The number of processing steps used to manufacture each semiconductor device has thus grown dramatically over time, necessitating increasingly high yields in each step (>99.999%) to achieve cost efficiencies (De Backer, et al. 2018). Without consistently reproducible means to achieve such high yields, semiconductor manufacturing would not be possible at the scale that today’s computerized industries require.

PFAS-containing materials are a critical element in achieving stringent yield requirements, but they have come under heightened scrutiny in recent years given growing concerns about the environmental and health impacts of long-chain, nonvolatile substances such as perfluorooctane sulfonate (PFOS) and perfluorooctanoic acid (PFOA). Concerns include high persistence, bioaccumulation potential and potential toxicity (Wang, et al. 2017); for more information, there are articles discussing PFAS use in numerous fields, including aeronautics, biotechnology, cosmetics, pharmaceuticals and medical devices (Glüge, et al. 2020).

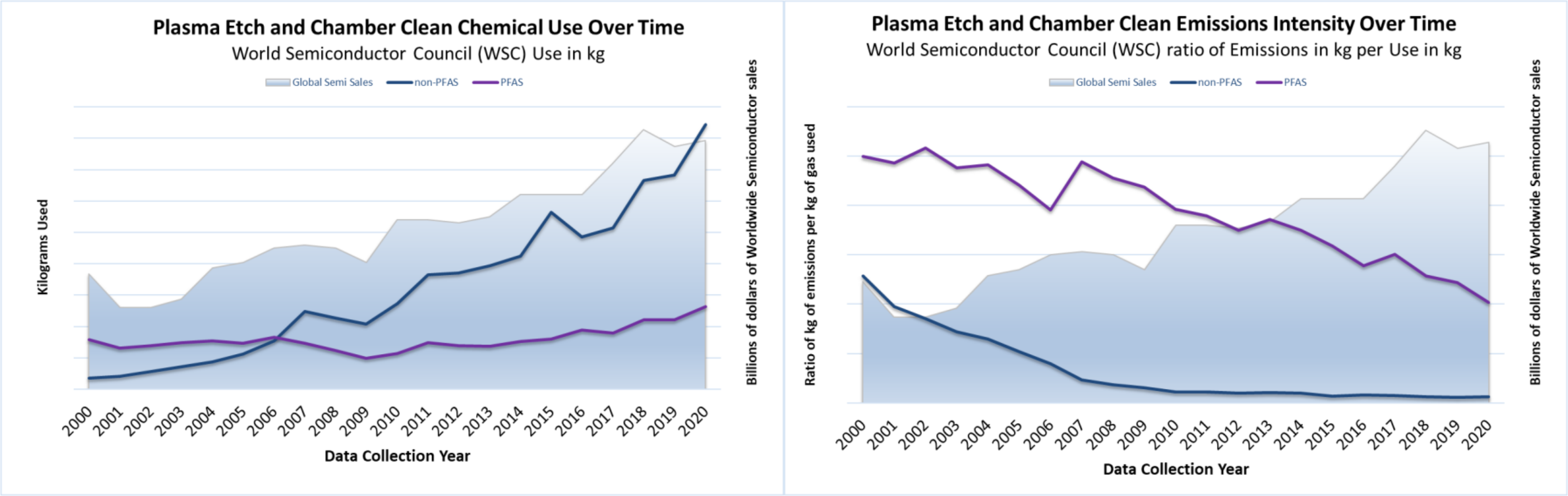
With the evident infeasibility of banning the general use of these chemicals, the notion of “essential use” arose as a way to prioritize areas where the industry could immediately reduce or eliminate PFAS-containing materials. The Montreal Protocol previously employed the concept of essential use for the targeted reduction of ozone-depleting compounds (chlorofluorocarbons [CFCs]), a successful example of a coordinated action to address industrial emissions (Cousins, Goldenman, et al. 2019).

In our role as industry experts, we focus our definition of essential use as “necessary for highly important purposes in semiconductor manufacturing for which alternatives are not yet established.” We intend to apply this definition as a lens to expand the analysis of PFAS usage in our industry beyond broad summaries. Of course, a detailed technical discussion of every PFAS use in semiconductor manufacturing would be far too large for a single publication. Thus, in this white paper we will focus on three processes: plasma (dry) etching, thin-film deposition and the chamber cleaning processes necessary for ensuring the stability of certain manufacturing steps. For those interested in other aspects, Ober et al. have discussed the use of PFAS-containing materials in lithography (Ober, Kafer and Deng 2022) and the Semiconductor PFAS Consortium is publishing separate white papers focused on wet chemistries and packaging.

At this point, we would like to make some important notes about a few of the chemicals used in these specific processes. The fluorinated chemistries predominantly used in plasma etching and chamber cleaning are hydrofluorocarbons (HFCs) and perfluorocarbons (PFCs). Because of their high global warming potential (GWP) and lengthy atmospheric lifetimes (Say, et al. 2021), these gases have been subject to regulation through prominent treaties such as the United Nations Framework Convention on Climate Change, the Kyoto Protocol and the Kigali Amendment to the Montreal Protocol (United Nations 1998); (United Nations 2016). This white paper will include discussions or figures that mention greenhouse gases (GHGs). In many instances, GHGs are directly analogous to HFCs and PFCs; for example, reductions of fluorinated GHGs would result in reductions of HFCs and PFCs.

There have also been targeted agreements between industry and national regulatory bodies, such as the second voluntary PFC Reduction Climate Partnership between the U.S. Environmental Protection Agency (U.S. EPA) and the Semiconductor Industry Association (SIA) on behalf of U.S. semiconductor manufacturing companies (U.S. EPA and SIA 2001); (U.S. EPA and SIA 2001). This partnership also covered noncarbon-containing fluorinated gases such as nitrogen trifluoride (NF_3) and sulfur hexafluoride (SF_6), which have been the subject of regulation in other countries. Specifically, the European Union introduced F-gas regulation (EU 517/2014) (European Union 2014) with the aim of reducing F-gas emissions to two-thirds of 2014 levels by 2030. This system established quotas for HFCs and hydrofluoroolefins (HFOs), which have molecules similar to HFCs but contain carbon double bonds. Like the U.S. EPA/SIA effort, this regulation also targeted noncarbon-containing fluorinated gases such as NF_3 and SF_6.

Figure 1a shows the overall reductions in the ratio of gases emitted to gases used from 2000 to 2020, superimposed with overall growth in the semiconductor market (SIA 2022). This data is even more impressive when considering the actual magnitude of the increase in process gas usage as computer chips become smaller and more complex, as shown in Figure 1b.



(a) **(b)**

Figure 1: Decreased emissions of fluorinated gases used in semiconductor manufacturing plotted with increased semiconductor sales from 2000 to 2020 (a); increased use of fluorinated gases used in semiconductor manufacturing plotted with increased semiconductor sales from 2000 to 2020 (b). Note that with increasing chip complexity, gas usage rates will likely increase faster than per-chip estimates. (Emissions data for reporting years 2000 through 2010 includes the United States, Europe, Japan, Korea and Taiwan. Emissions data for reporting years 2011 through 2020 includes the United States, Europe, Japan, Korea and Taiwan, plus China and member company "rest-of-world" facilities.)

The American Innovation and Manufacturing (AIM) Act of 2020 set more aggressive targets for reducing HFCs, with a proposed 85% reduction in production and consumption over the next 15 years. To ensure compliance, the act institutes an electronic tracking system for the movement of HFCs through commerce, and requirements for third-party auditing of companies' recordkeeping and reporting, among other measures. The U.S. EPA did issue allowances for six applications for a period of five years, one of which is the "etching of semiconductor material or wafers and the cleaning of chemical vapor deposition [CVD] chambers within the semiconductor manufacturing sector."

While HFCs and PFCs have been subject to regulation based on their long atmospheric lifetimes and high GWP, the question has arisen recently as to whether they are PFAS chemicals, and should thus be subjected to additional controls. The lack of an agreed-upon definition for the term PFAS within the multitude of regulatory activities complicates this technical effort. To name just two, an international panel of scientists convened by the Organization for Economic Co-Operation and Development defined PFAS in a 2021 report as "fluorinated substances that contain at least one fully fluorinated methyl or methylene carbon atom (without any H/Cl/Br/I atom attached to it), i.e., ... any chemical with at least a perfluorinated methyl group (-CF3) or a perfluorinated methylene group (-CF2-)" (OECD 2021). The U.S. EPA used a narrower definition in a 2021 action under the Safe Drinking Water Act: "... a structure that contains the unit R-CF2-CF(R′) (R″), where R, R′ and R″ do not equal "H" and the carbon-carbon bond is saturated (note: branching, heteroatoms and cyclic structures are included)" (Wang, et al. 2021); (U.S. EPA 2021).

The situation is complicated by the fact that there are several other definitions in circulation, and no clearly established guideline of which definition to pick (Buck, et al. 2011); (Barnabas, et al. 2022). For instance, the U.S. National Defense Authorization Act for Fiscal Year 2020 (Public Law 116-92) states these two definitions, which provide more differentiation than the U.S. EPA definition (United States Congress 2019):

- The term "perfluoroalkyl substances" means aliphatic substances for which all of the H atoms attached to C atoms in the nonfluorinated substance from which they are notionally derived have been replaced by F atoms, except those H atoms whose substitution would modify the nature of any functional groups present.
- The term "polyfluoroalkyl substances" means aliphatic substances for which all H atoms attached to at least one (but not all) C atoms have been replaced by F atoms, in such a manner that they contain the perfluoroalkyl moiety CnF2n+1 (for example, $C_8F_{17}CH_2CH_2OH$).

To be clear, NF_3 and SF_6 do not fit any definition of PFAS (as neither molecule contains carbon) and are thus out of the scope of this white paper. However, their use in plasma (dry) etching, thin-film deposition and chamber cleaning does generate PFAS byproducts, albeit at a lower volume compared to direct HFC and PFC use.

Since the purpose of this white paper is to document the use of all materials that could potentially meet a regulatory definition of PFAS, along with the performance requirements to meet a need to determine the criticality and/or essentiality of the use, the Semiconductor PFAS Consortium has defined the scope of materials described in this white paper to include all chemistries and materials that contain molecules with -CF2- and/or -CF3 moieties.

2.0 Objectives

As previously stated, specific chemicals that could eventually be classified as PFAS-containing materials include HFCs and PFCs, which are already subject to monitoring regulations and emission-reduction goals due to their GWP. We will outline the necessary attributes of these materials for successful semiconductor manufacturing, including but not limited to reaction rates and selectivity and surface reaction characteristics. We will discuss non-PFAS alternative compounds where available, as well as efforts to develop alternatives. Finally, we'll explore the potential release/exposure pathways of these materials from semiconductor fabrication (fab) facilities and mitigation options.

2.1 Categories and Usage of Fluorinated Chemicals in Plasma Etch, Thin-Film Deposition and Plasma Chamber Cleaning

Fluorinated chemistries used in plasma (dry) etch, thin-film deposition and plasma chamber cleaning can be gases (predominantly HFCs and PFCs), liquids, or solids (organometallic precursors). Table 1 lists some examples of substances used in semiconductor manufacturing processes. See Table A-1 in Appendix A for a more complete summary.

Table 1: Examples of fluorinated chemicals used in semiconductor manufacturing.

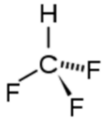
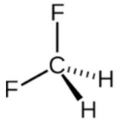
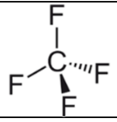
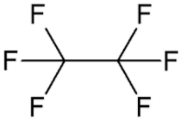
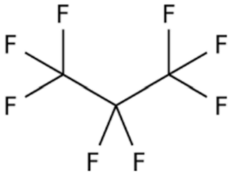
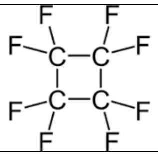
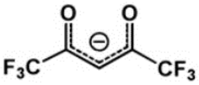
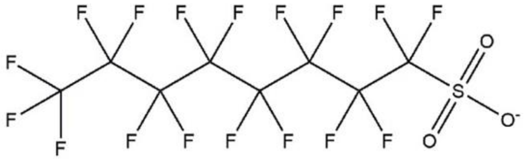
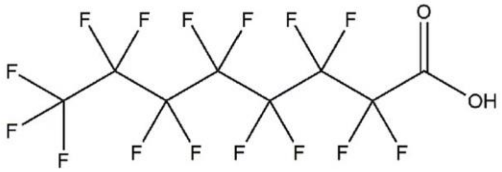
Classification	Name	Chemical Structure
HFC Gas	Trifluoromethane (CHF_3)/ HFC-23	
HFC Gas	Difluoromethane (CH_2F_2)/ HFC-32	
PFC Gas	Tetrafluoromethane (CF_4)/ PFC-14	
PFC Gas	Hexafluoroethane (C_2F_6) / PFC-116	
PFC Gas	Octafluoropropane (C_3F_8)/ PFC-218	
PFC Gas	Octafluorocyclobutane (C_4F_8)/freon-C-318	
Organometallic Precursor Ligands	hfac (1,1,1,5,5,5-hexafluoro-2,4-pentane-dionate)	

Table 2 illustrates the chemical structure of PFOS and PFOA, in order to provide a comparison with the substances shown in Table 1.

Table 2: The chemical structure of PFOS and PFOA.

PFOS	
PFOA	

The longer carbon-chain lengths of these molecules (eight for PFOS/PFOA vs. one to four for HFCs and PFCs) impart radically different chemical properties. In the absence of a plasma, HFC and PFC molecules are generally stable and do not react with other materials. All HFCs and PFCs exhibit low boiling points and are gases at ambient temperature. As a result, emission of these materials will accumulate in the air, rather than in water or soil. Table A-2 in Appendix A lists the ecological information of the safety data sheets for HFC and PFC molecules used in semiconductor manufacturing.

A chemical is deemed likely to bioaccumulate under Registration, Evaluation, Authorization and Restriction of Chemicals (REACH) regulations if the octanol-water partition coefficient (abbreviated log K_{ow} or log P_{ow}) is above 4.5 (Little Pro 2017). For example, the log K_{ow} of PFOS and PFOA (two of the most prominently discussed PFAS compounds) is 5.3 and 6.3, respectively, indicating a high bioaccumulative potential (Geosyntec Consultants 2019). By contrast, none of the HFC or PFC chemistries discussed in this white paper have log K_{ow} values over 3.

Additionally, PFOS and PFOA are both solids at room temperature. The low volatility of PFOS, PFOA and their precursors are responsible for their accumulation in water and soil, rather than in the atmosphere. The environmental degradation processes that generate these two harmful species involve several mechanisms (Evich, et al. 2022). The conditions required to synthesize HFCs and PFCs do not occur outside of an industrial facility. As result, the conversion of the HFCs and PFCs listed in Table 1 to bioaccumulative species like PFOS or PFOA should not occur in the natural environment.

While purely structural definitions of PFAS apply the broadest classification to limit further pollution, this approach also has some downsides. For example, there are negative implications for enforcement given the costs and resource needs of addressing such an abundant group of substances (Cousins, DeWitt, et al. 2020). Exemptions have been granted for substances that meet structural PFAS definitions but are already regulated in some capacity, such as pharmaceuticals (Hammel, et al. 2022). The European Fluorocarbons Technical Committee has also applied similar logic to HFCs and PFCs (European Fluorocarbons Technical Committee 2022).

2.2 The Role of CFx Chemistry

Silicon is the material synonymous with the field-effect transistor (FET). Silicon is ubiquitous because of its availability (it is the second-most abundant element in the earth's crust by mass) and relative ease of its crystal growth. But perhaps silicon's defining factor is that you can easily grow a high-quality dielectric layer over it with a stable, well-ordered interface (silicon oxide) (Marchack and Chang 2012). Dielectric materials are electrical insulators that polarize in the presence of an electric field, thus allowing for the reproducible switching of FET devices between on and off states (that is, the foundation of the bit as "1" or "0").

Although the industry introduced high-dielectric constant materials to replace silicon dioxide in sub-100-nm devices as the gate insulator, silicon dioxide-based materials remain dominant as insulators to isolate the metal wires that power and control the transistors (see the Plasma Etching section) and are often used as hard masks because of their chemical stability. In such cases, the silicon dioxide is deposited onto the silicon wafer and needs to be patterned into small dimensions (the deposition process also coats the reactor interior with silicon dioxide, thus necessitating chamber cleaning).

The patterning and cleaning of silicon dioxide requires HFCs and PFCs. Because silicon dioxide is a very stable solid (glass), forming thermodynamically favorable volatile products (silicon fluorides) requires the highly electronegative fluorine atom. Additionally, carbon reacts with oxygen to form carbon dioxide, which is also stable and gaseous. Thus, manufacturers use HFCs and PFCs to etch silicon dioxide with high etch rates and good selectivity, through the formation of a complex fluorocarbon polymer layer that modulates the etching and deposition reactions, as detailed in the Plasma Etching section (Donnelly and Kornblit 2013); (Oehrlein 2011). Currently, there is no known substitute for fluorocarbon gases that can form volatile chemical species with silicon-based materials at a temperature compatible with the surrounding materials and the device structure under fabrication.

3.0 Plasma Etching

Plasma etching uses a partially ionized, gaseous medium to remove solid materials from targeted areas of a wafer surface. The process is conducted in subatmospheric vacuum reactors to maximize both the efficiency of ionization and the mean free path of the gas phase species, as well as to ensure the quick removal of volatile etch byproducts. The angular distribution of ionic species in the plasma is tightly controlled by the electric field given the plasma sheath and applied power, allowing for anisotropic etching at nanometer-length scales. Additionally, the energy supplied by these ions enables chemical reactions at substrate temperatures well below what wet etchant solutions would require. Tuning reactor parameters such as delivered power, operating pressure and gas flow rates enable further control over plasma properties (electron temperature, neutral/ion ratio and species fluxes) and by extension the reaction environment. This versatility has made plasma etching the primary means of transferring lithographically defined features into the semiconductor, metal and dielectric materials that constitute today’s computer chips (Marchack, Buzi, et al. 2021).

HFCs and PFCs are used primarily in the plasma etching of silicon and silicon-based dielectrics (standard high-aspect-ratio etches such as capacitor, memory-hole etches hard mask patterning, the Bosch process for through-silicon vias and shallow trench isolation). Using back end of line (BEOL) as an example, plasma etching creates pattern via and line structures into dielectric layers to define wiring layouts on the chip. Electroplating fills the defined template with copper, and any excess material is polished from the top of the surface using a technique called chemical mechanical planarization. These steps are collectively known as the damascene process, which was introduced in 1997. The damascene process enabled the introduction of copper, which was deemed unetchable by gas-phase processes at the time (Bernasconi and Magagnin 2018). The BEOL system supplies power and allows communication between the billions of FETs that make up today’s modern microprocessors. Figure 2 shows the final structure of the BEOL in an Intel Broadwell 14-nm technology node product.

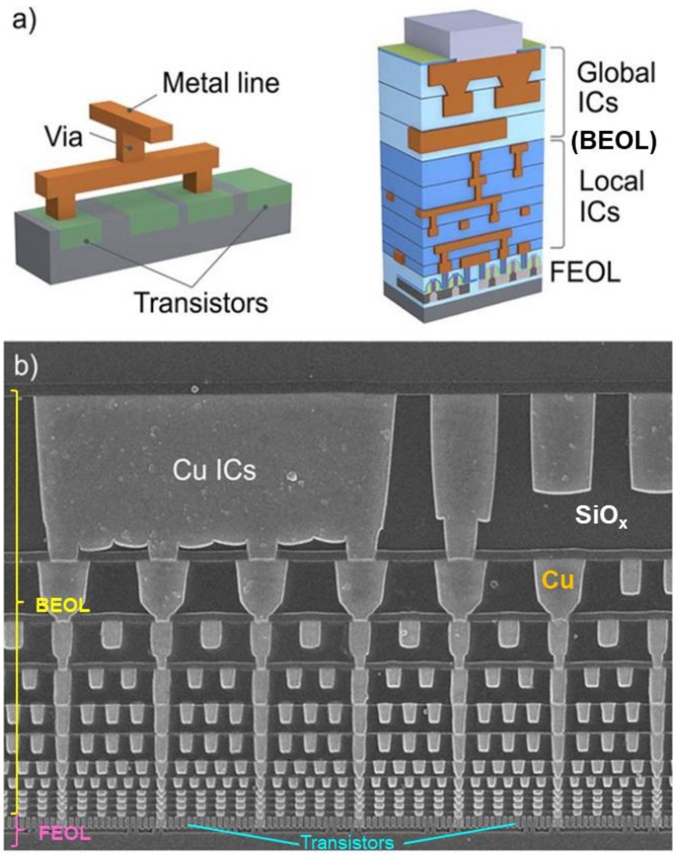


Figure 2: Schematic of a microprocessor structure created by repeated steps of thin-film deposition and plasma etching (a); cross-section of a 14-nm Intel Broadwell chip showing the difference in size between BEOL and front end of line (FEOL) (b). All silicon dioxide layers represent a CVD deposition step and a plasma-etch step to pattern the features filled with copper (Bernasconi and Magagnin 2019)**.**

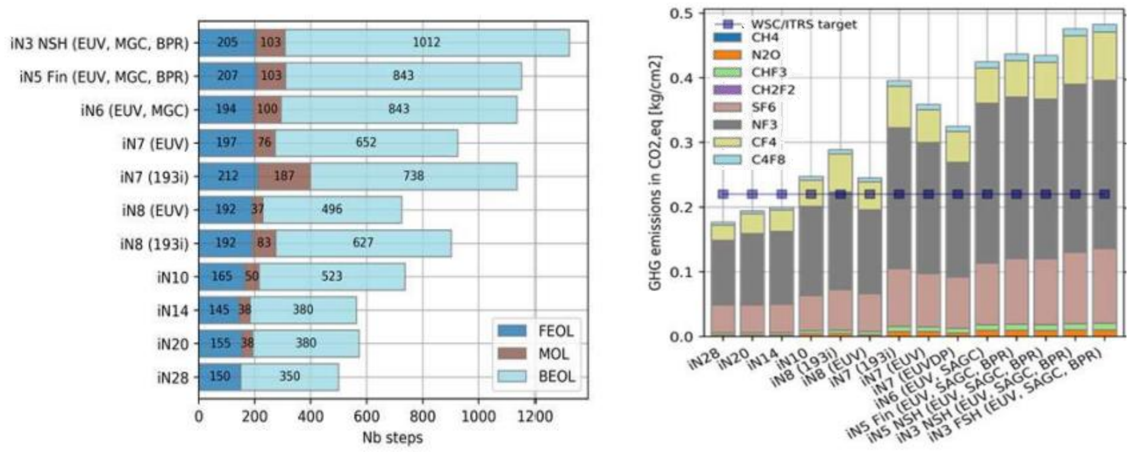
As computer chips have become smaller and denser in recent years, the complexity of the BEOL system has increased substantially. Not only are more layers required to handle the communication demands between increasing numbers of transistors and multicore designs, but the dielectric layers now contain increasing amounts of carbon, hydrogen, nitrogen and other elements, in addition to silicon and oxygen. The additions of these elements reduce the dielectric constant of the layers, which helps maintain performance by reducing resistive-capacitive delay.

To ensure patterning fidelity in these new materials, there have been further studies of different HFC etch molecules (C_4H_9F, CH_3F), with a particular emphasis on understanding the mechanisms of selectivity (Miyazoe, et al. 2018). For other applications of PFAS-containing compounds in plasma etch, see Table A-1 in Appendix A.

3.1 Trends in Plasma Etch

Plasma etch has always played a critical role in the semiconductor industry. Downscaling lithographic dimensions was an initial driver of device performance: metal-oxide semiconductor field-effect transistor performance increased as its dimensions shrunk, a phenomenon known as “Dennard scaling.” It was the adoption of anisotropic plasma etch processes that allowed consistent yielding of submicron features. As device sizes shifted below 50 nm, subsequent delays in the adoption of extreme ultraviolet (EUV) lithography led to innovative self-aligned multiple patterning schemes, which employed sequential steps of highly conformal deposition and etching in order to subdivide a starting lithographic pattern (Raley, et al. 2016). Thus, the number of plasma etch processing steps required to generate a structure at the specified dimensions effectively increased by factors of 2, 4 or more, leading to proportional increases in gas usage. The introduction of new device architectures such as FinFETs required longer over-etch times with highly selective etch conditions to clear material from areas with vastly different geometric layouts (Engelmann, et al. 2017).

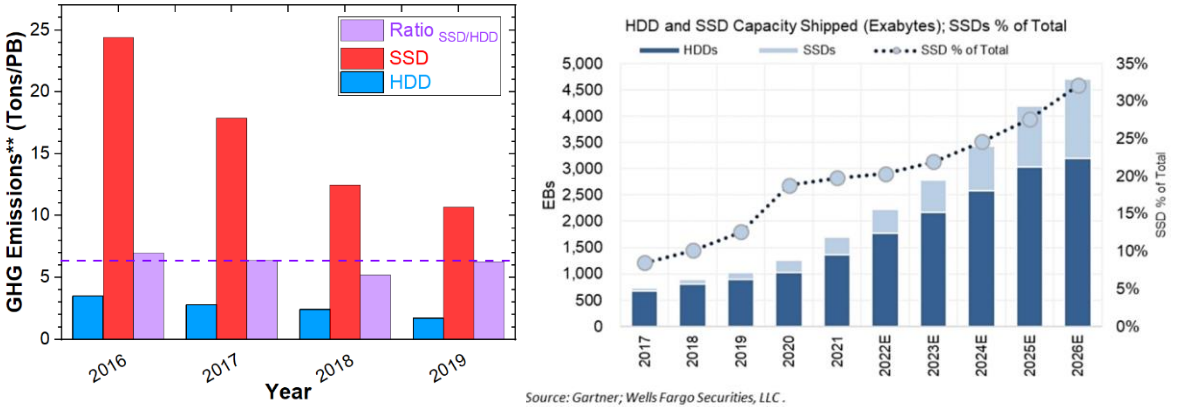
More recently, while the maturation of EUV technology enabled significant reductions in the number of process steps required for logic device patterning at current technology nodes (7 nm), the increasing complexity of middle of line (MOL) and BEOL for future process flows has led to projections that the overall number of process steps will increase by a factor of roughly 2.5 from the 28-nm to 3-nm technology node, as shown in Figure 3a (Bardon, et al. 2020). This corresponds to a projected proportional increase in GHG emissions (measured in kilograms of carbon dioxide equivalent per square centimeter of wafer), as shown in Figure 3b. Such a proportional increase is largely driven by an increase in the number of CVD steps, which in turn requires more chamber cleans using NF_3. We will discuss the chamber cleaning process in the Thin-Film Deposition Chamber Clean Use section.



(a) **(b)**

Figure 3: Number of process steps by technology node (bottom = older), showing a proportional increase in BEOL and MOL steps (a); GHG emissions per square centimeter of silicon wafer per technology node (b) (Bardon, et al. 2020)**.**

There are related trends in process steps and gas consumption in memory devices. Limitations on the progress of downscaling lateral dimensions have led to the vertical shifting of densities, which has necessitated the patterning of features with exceedingly high aspect ratios. Perhaps the most notable example is solid-state drives (SSDs). For example, vertical-channel 3D not-AND (NAND) requires the etching of over 100 dielectric layers, with over 200 planned for future devices (Lee, et al. 2021). According to data from Western Digital (plotted in Figure 4a), the total emissions of scope 1 and 2 GHGs, HFCs and PFCs, NF_3, and SF_6 resulting from the manufacturing of SSD are on average between 6 and 7 times that of conventional hard-disk drive (HDD) technology (Marchack, Miyazoe, et al. 2022). Given the trending growth rate in shipped SSD storage over time, as shown in Figure 4b, it is reasonable to expect a significant rise in HFC/PFC/SF_6/NF_3 gas consumption. Process optimization through improvements in techniques such as endpoint monitoring for chamber cleans can potentially help offset some of this projected consumption, which the Thin-Film Deposition Chamber Clean Use section will cover in more detail. To learn more about future research opportunities related to plasma applications in the semiconductor industry, see the "DOE Report on Science Challenges and Research Opportunities for Plasma Applications in Microelectronics" (U.S. DOE 2023).



Source: Gartner; Wells Fargo Securities, LLC.

(a) **(b)**

Figure 4: GHG emissions (scope 1 and 2, plus carbon dioxide, methane, nitrous oxide, HFCs, PFCs, SF_6 and NF_3) in tons/shipped petabytes for SSD and HDD technology (a); estimated distribution of SSD and HDD market share for 2026, showing growth trends (b) (Mellor 2022)**.**

3.2 Alternatives in Plasma Etch

As previously mentioned, introducing new materials into the device manufacturing process flow (such as low-k dielectrics) necessitated studying potential alternative etch precursors. Suppliers have evaluated chemistries based on their environmental impact; for example, unsaturated fluorocarbons such as C5F8 and fluoroether compounds with lower GWPs (Chatterjee, et al. 2002); (Cha, et al. 2019). Most structural definitions of PFAS under consideration would encompass both of these candidates. The major barrier to implementing alternatives lies in the technology cycle of development and ramp up to high-volume manufacturing.

In essence, if the environmental impact of a process is not considered during the development stage, the ability to change it once implemented may be highly challenging, as depicted in Figure 5. The primary option in such cases is to add or modify abatement solutions to mitigate emissions, thus incurring additional costs and delays to the manufacturing cycle. Another aspect affecting implementation is that certain failure points only arise after scaling a process up to higher volumes – if for example an alternative chemistry has a corrosive effect on consumable parts and materials such as gas delivery systems, exhaust, etc.

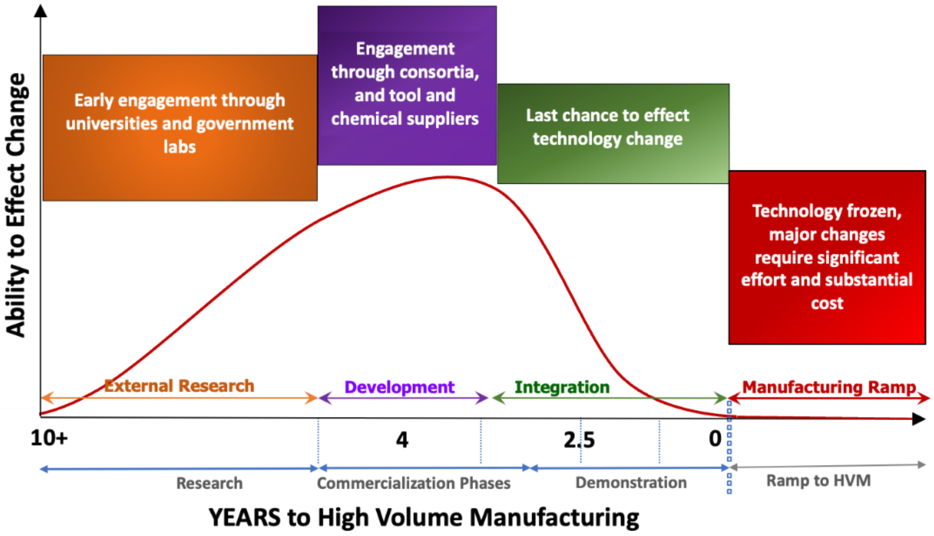


Figure 5: Environmental health and safety (EHS) engagement model.

It is possible to trace other difficulties when designing PFAS replacements to the nature of the C-F molecular structure described at the start of this section. In many instances suppliers examined only the performance metrics (selectivity, etch rate) of alternative chemistries rather than the specific classification of the material as PFAS/HFC/PFC or its GWP potential (Lin, et al. 2018). The impetus to consider sustainability will be most effective if driven from the funding side of the research and development equation. In parallel, improvements to semiconductor fab abatement systems (which treat unused input gases as well as reaction byproducts from the process chambers) could potentially further reduce PFAS concentrations in output streams for processes where it is not possible to avoid HFC and PFC use. For a more detailed discussion on abatement systems, see the Abatement section.

4.0 Thin-Film Deposition Chamber Clean Use

Thin-film deposition is an integral process in semiconductor manufacturing where vaporized materials react on a wafer surface to create thin metal or dielectric layers. These films, or layers, change the electrical properties of the wafer surface and form the basis of the main features in a computer chip. Physical vapor deposition (PVD), CVD and electroplating are the main types of thin-film deposition used in semiconductor manufacturing. Because gases will naturally expand to fill the volume they occupy, vapor deposition processes (PVD and CVD) often result in the depositing of similar amounts of material on the wafers, as well of the interior of the chamber. The resulting change in composition of the exposed interior surfaces can affect the reaction kinetics of the chamber, resulting in yield detractions caused by deviations in deposition rate and quality of the desired film. (Recall that each of the several 100 to 1,000 process steps in semiconductor manufacturing require process yields greater than 99.999% to result in a wafer with an adequate number of functioning chips.)

In the worst-case scenario, the deposited material can flake off in the form of particles, land on the wafer and destroy the devices being built, rendering an entire production line’s output useless. As discussed in the Alternatives in Plasma Etch section, such depositions of silicon-based dielectrics in the BEOL are projected to comprise 73% to 77% of the total steps involved in manufacturing a single complementary metal-oxide semiconductor device at the 5-nm technology node (Bardon, et al. 2020). Thus, cleaning processes for the deposition chambers are increasingly critical for scaling up the manufacture of advanced semiconductor devices. Generating fluorine radicals (reactive species) in plasma discharges has proved effective for achieving the requisite cleaning.

4.1 Historical Overview

Since the 1980s, perfluorocompounds such as C_2F_6 and CF_4 were used as fluorine generation sources for CVD chamber cleans because they were nonflammable, less corrosive and less toxic than many other options (Beu 2005). However, concerns arose about the high GWP and long atmospheric lifetimes of fluorinated GHGs: for example, C_2F_6 has a GWP_{100} of 12,400 and an atmospheric lifetime of 10,000 years; the GWP_{100} of CF_4 is 7,380 and its atmospheric lifetime is 50,000 years. As a result, the industry undertook extensive voluntary efforts to reduce PFC consumption and emissions, as mentioned in the introduction (U.S. EPA 2001); (WSC 1999); (WSC 1999-2014). Initial efforts focused on finding drop-in replacements (C_3F_8, c-C_4F_8 and octafluorotetrahydrofuran [C_4F_8O]) with higher gas utilization efficiency in the plasma clean process. With drop-in replacements, it is not necessary to install new gas lines and additional EHS control systems; however, those chemistries generated a substantial amount of perfluorocarbon byproducts and did not necessarily result in significant GHG reductions.

4.2 The Transition from PFCs to NF_3

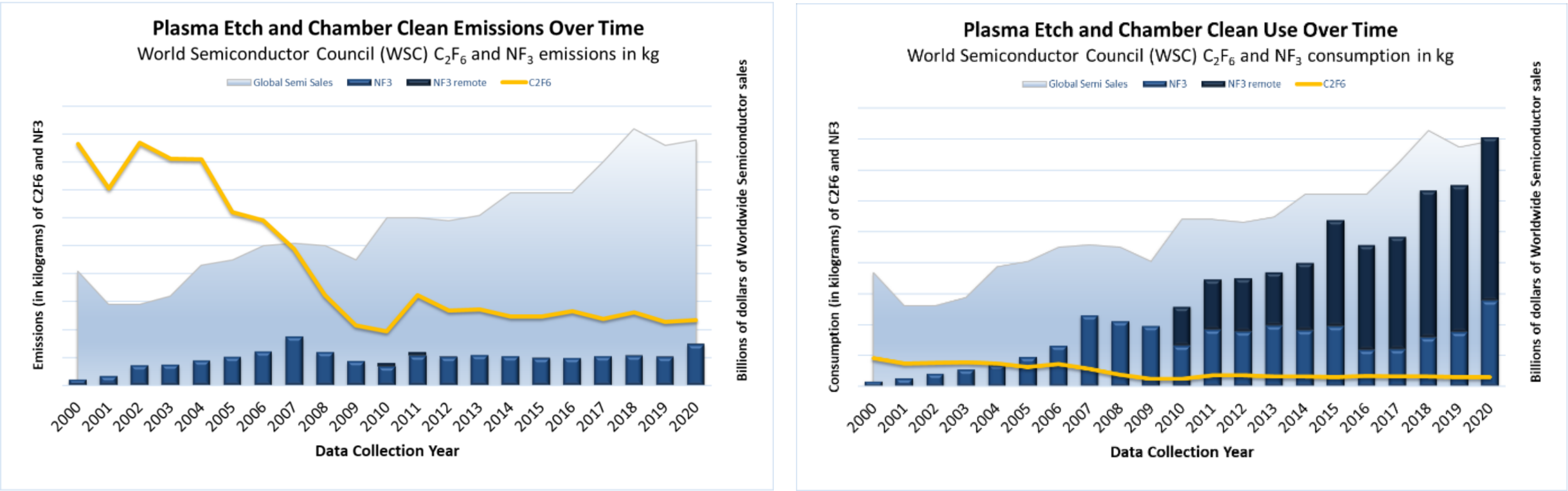
The industry soon moved to using NF_3, which offered several advantages over fluorocarbon gases:

- Higher plasma utilization efficiency (lower overall process GHG emissions).
- Fewer high GWP byproducts.
- The ability to conduct remote plasma cleans, which reduced hardware degradation and subsequent downtime for chamber maintenance.
- Improved throughput from faster clean rates (a consequence of higher utilization efficiency).

Figure 6a shows the consumption in C_2F_6 and NF_3 from 2000 to 2020. In the figure, the increased use of NF_3 is attributed to large increases in manufacturing capacity (EPS 2018). However, given the increased plasma utilization efficiency of NF_3, the overall emissions of NF_3 increased by only 89%, as shown in Figure 6b.

This change did not come without drawbacks: NF_3 does possess a high GWP_{100} (17,400) but this statistic is largely offset by its high utilization efficiency in remote plasma systems. NF_3 is also an oxidizer and thus is not a drop-in replacement; moreover, increased process utilization efficiency results in hydrofluoric acid (HF) and fluorine (F_2) byproducts, which require additional EHS controls. While NF_3 itself does not contain carbon, it is possible for CF_x byproducts to form through its reaction with carbon-containing silicon oxide films. While pure F_2 gas has a GWP_{100} of zero, its high toxicity and corrosivity requires specialized transportation and safety measures to ensure proper handling in a high-volume manufacturing setting (for example, nickel or nickel-alloy fittings and valves are needed for concentrations exceeding 30%). Nonetheless, recent research efforts have continued to investigate the suitability of F_2 as a potential alternative, with on-site approaches noted for providing lower power requirements (Boudaden, et al. 2018); (Cigal, Lee and Stockman 2016).

While initially motivated by the goal of reducing global warming, these efforts have resulted in a dramatic reduction of perfluorocarbon gas use in semiconductor manufacturing on a per-chip basis. Process endpoint optimization and improvements in abatement technology (Fujii, et al. 2008); (Lee, et al. 2013) have also made reductions possible. Appendix B discusses endpoint optimization in more detail, while the Abatement section discusses abatement systems in more detail.



(a) **(b)**

Figure 6: World Semiconductor Council (WSC) increasing NF_3 and decreasing C_2F_6 use (a); increasing NF_3 and decreasing C_2F_6 emissions from 2000-2020, superimposed with increases in sales of semiconductors over the same time (WSC 1999-2014) **(b). (Chemical use and emissions data for reporting years 2000 through 2010 includes the United States, Europe, Japan, Korea and Taiwan. Chemical use and emissions data for reporting years 2011 through 2020 includes the United States, Europe, Japan, Korea and Taiwan, plus China and member company "rest-of-world" facilities.)**

5.0 PFAS Used in Advanced Deposition and Etch Processes

5.1 CVD/ALD Deposition of Organometallics

The use of fluorinated compounds, and more specifically polyfluorinated compounds as ligands in deposition precursors, has a long history (Shin, et al. 1996). The presence of fluorine in the molecules serves two predominant and important roles. First, the presence of fluorine atoms in organic compounds reduces the intermolecular dispersion force and thereby increases the volatility (lowering the boiling temperature) significantly (Norman and Perez 2012). Second, the presence of fluorine in the molecule is known to improve the chemical stability of such compounds (Fenton 1971).

In vapor deposition, these two properties are both important: high volatility and good thermal stability are necessary to vaporize and transport the precursor into the deposition chamber; furthermore, for atomic layer deposition (ALD) processes, the thermal stability of precursors plays an even more important role to selectively deposit material in a self-limiting manner as a monolayer on a chemically activated substrate. Equipment manufacturers are evaluating new metals and metal-containing films to reduce electrical resistance and thus energy dissipation in shrinking integrated circuit designs. These processes require the deposition of a variety of pure metal and metal alloy films, many of which have not been previously integrated into semiconductor manufacturing. The deposition of these films will be enabled by the use of not only this particular ligand, but myriad other fluorine-containing ligands.

Also, the high volatility and desirable combination of good thermal stability and controllable reactivity of metal complexes containing fluorinated ligands makes these PFAS molecules attractive for the thermal (plasma-free) selective chemical vapor etching of metals. One example is the etching of metals in a selective and self-limiting manner, in which metal organics are volatilized and removed from the surface conformally (Kang, Kim and Rhee 1999). Highly selective and controllable processes such as these can reduce the number of steps in semiconductor processing and significantly reduce the overall chemical and energy content of such electronic devices.

Although the fluorinated materials used in vapor deposition or etching as described in this section are typically air- and/or moisture-sensitive, it is possible that they or their atmospheric decomposition could pose an EHS risk if released without suitable abatement. The high purity and chemical reactivity of these precursors necessitates careful production, packaging and transporting to their point of use in high-integrity (usually stainless steel) vessels that are hermetically sealed and have a leak rate $<10^{-8}$ cc-atm/sec. Furthermore, in both CVD processes and thermal chemical vapor etching, the process equipment is in a closed system, with a high percentage of process effluents captured and abated downstream of the process.

5.2 PFAS Chemistries Used in Area-Selective Deposition Processes

Many advanced semiconductor processes currently in production as well as future processes rely on area selective deposition schemes to achieve scaling, yield and power consumption goals. These processes take advantage of a variety of mechanisms including pre-treatment, intrinsic selectivity, self-assembled monolayers (SAMs) and small molecule inhibitors. Parsons and Clark have provided a review of the area selective deposition process, along with the requirements for pre-treatment steps and cleaning steps (Parsons and Clark 2020). The addition of the fluorine molecule to SAMs has the potential to change the physical properties of the resulting monolayers, largely because of the electrostatic character of the C-F bond. Zenasni, Jamison and Lee have summarized the effect of mixtures of fluorinated SAMs, such as perfluorinated decanethiol and fluorinated alkanethiols (Zenasni, Jamison and Lee 2013).

Advanced semiconductor process flows may become increasingly reliant on area selective deposition techniques, and the use of PFAS molecules may be necessary to enable the overall manufacturing sequence. Depending on the application, the properties imparted by fluorination may render the techniques unfeasible. Additionally, the rates of usage of the PFAS-cleaning molecules within such area selective deposition processes are very low, and waste vapors are typically routed to a point-of-use (POU) thermal abatement unit as an effective environmental control.

5.3 Molecular Vapor Deposition for Surface Functionalization

Another area where PFAS is necessary is surface functionalization. One recent application is in microelectromechanical systems (MEMS), which are fabricated from silicon using both standard semiconductor processes and specialized MEMS fabrication processes. This extends microelectronics to also include sensing and actuating functions. Widespread applications of semiconductor MEMS include inertial sensors for the measurement of acceleration or yaw rate, pressure sensors, and micromirrors.

Because MEMS have moving structures in micrometer dimensions, some of these devices require precise control of attractive surface forces to prevent moving structures from sticking together. Stiction of a MEMS element prevents the movement of the structures, which leads to a failure of the function and must therefore never happen during use.

Coating the MEMS surfaces with a material of low-surface energy significantly reduces surface forces. Vapor phase deposition from the molecular vapor of functionalized reactive silanes has proven to be the most suitable method for forming such coatings during the MEMS wafer process (Ashurst, Carraro and Maboudian 2004). Molecular layers of fluorocarbon molecules are particularly advantageous for such anti-stiction coatings (Mayer, et al. 2000); (Ashurst, Carraro and Maboudian 2004). Given the special nature of C-F chemical bonds, fluorocarbon compounds offer surface energies that are among the lowest of all known materials, together with the excellent temperature stability required for wafer bonding at >400°C in the subsequent wafer process, high mechanical and chemical robustness, low friction, and excellent electrical isolation (Janssen, et al. 2006); (Zhuang, et al. 2007).

6.0 Abatement

Semiconductor fabs are equipped with segregated exhausts and exhaust management technologies (scrubbers or thermal oxidizers) to treat gaseous effluent from processes (Sherer 2013). Acid exhaust ducts carry a mixture of corrosive gases and mists, as well as particulate from multiple process tools to "central" or "house" wet scrubbers, while solvent exhaust ducts carry volatile organic compounds (VOCs) emitted from various processes to central or house thermal oxidizers.

The exhaust from semiconductor process reactors includes not only the unreacted input materials but also reaction byproducts. For example, C-F input gases will form C-F byproducts in the plasma process (such as C_2F_6 and O_2 clean processes generating CF_4). Inorganic fluorine compounds or F_2 will generate C-F byproducts when etching or cleaning carbon-containing films. For some processes, abatement is installed on the exhaust of the process tool or at the POU. Figure 7 shows a flow diagram schematic of such a setup. For additional information on air emissions control and abatement, see the Semiconductor PFAS Consortium white paper, "Background on Semiconductor Manufacturing and PFAS."

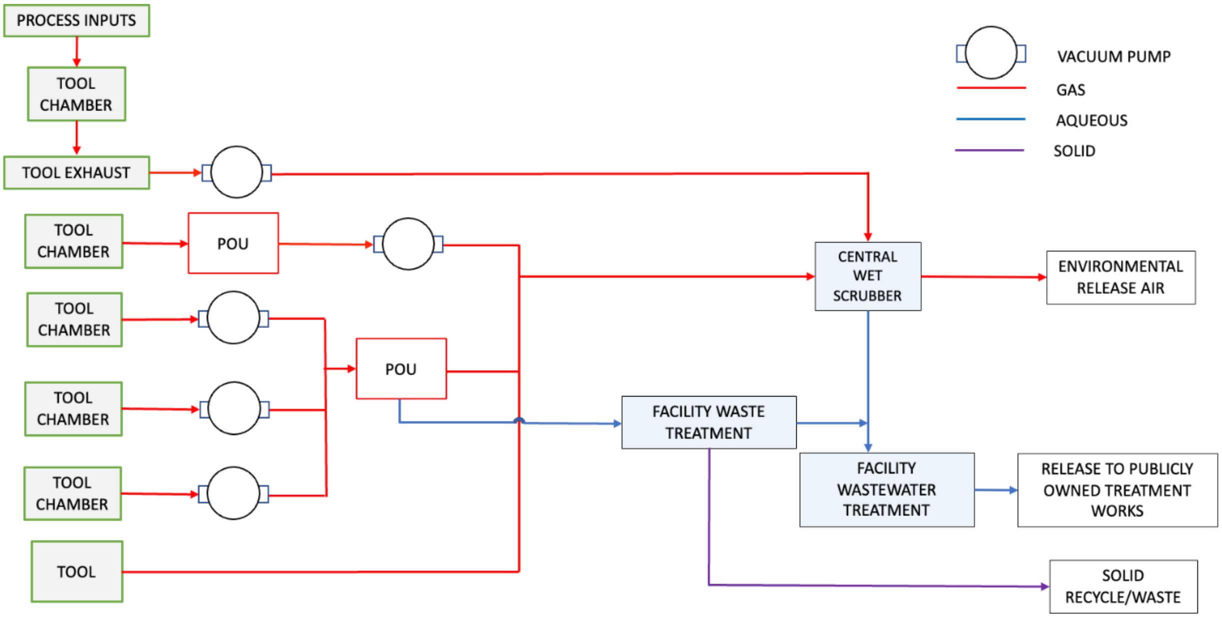


Figure 7: Example process exhaust with pre-pump plasma installed on one chamber of a cluster, post-pump abatement installed on two process chambers of a plasma-enhanced CVD tool, and one tool chamber without POU abatement.

The abatement of fluorinated GHG (F-GHG) air emissions from semiconductor processes poses these challenges:

- The C-F bond is difficult to break.
- Etch and plasma CVD processes occur under a vacuum, with F-GHG flow rates tens to hundreds of standard cubic centimeters per minute in etch processes (Hong and Uhm 2003) and several liters per minute in chamber cleans (ISMI 2005). Vacuum pumps use nitrogen as a purge gas; thus, post-pump emissions are diluted and require significant energy input to convert F-GHGs into water-scrubbable byproducts. F-GHG emissions continue to be further diluted as they move downstream of the process chamber into central exhaust ducts. Because of dilution, semiconductor F-GHG abatement technologies cannot demonstrate very high destruction or removal efficiency (DRE), such as the 99.99% removal specified for concentrated F-GHG emissions from other industries (United Nations 2016).
- Abatement systems require space and infrastructure (such as natural gas fuel lines, which may not be installed in an existing fab); moreover, the products of abatement (HF, COF2) require further treatment such as water scrubbing, fluoride removal or elementary neutralization, which may not have capacity for the increased waste streams. If a fab is not initially designed with F-GHG abatement systems, retrofitting may be infeasible.

As described in the Objectives and Transition from PFCs to NF_3 sections, the semiconductor industry has undertaken extensive efforts to develop and evaluate F-GHG emissions reductions technologies, including alternative chemistries and processing (where feasible), process optimization to reduce gas consumption, recovery and recycling, and abatement. (Mocella 1996); (Beu 2005); (Illuzzi and Thewissen 2010). Although not the only practice in driving HFC and PFC emissions reductions, abatement plays a key role in voluntary industry efforts to reduce emissions.

As illustrated in Figure 8, abatement evaluations and development began in 1994, with researchers and abatement suppliers pursuing multiple technologies (shown in light blue). The International SEMATECH Manufacturing Initiative's "1998 Current State of Technology: Perfluorocompound (PFC) Emissions Technology Transfer No. 98053508A-TR" found only one commercially available POU abatement technology (a burn-wet system) capable of achieving >90% DRE for all PFCs; however, it further found that: "The typical combustion device uses significant quantities of water (up to 8,600 gallons per day per device) and creates wastewater that requires treatment for fluorides in the fab's industrial waste treatment (IWT) system. Many sites do not have the IWT capacity to handle widespread installation of such abatement devices. In addition, some devices require gas distribution systems in the fabs for oxygen and natural gas (a gas not commonly used in fabs)."

In the intervening 25 years, the development of F-GHG abatement systems advanced significantly. Devices now achieve improved DRE, with reduced consumption of water and other resources.

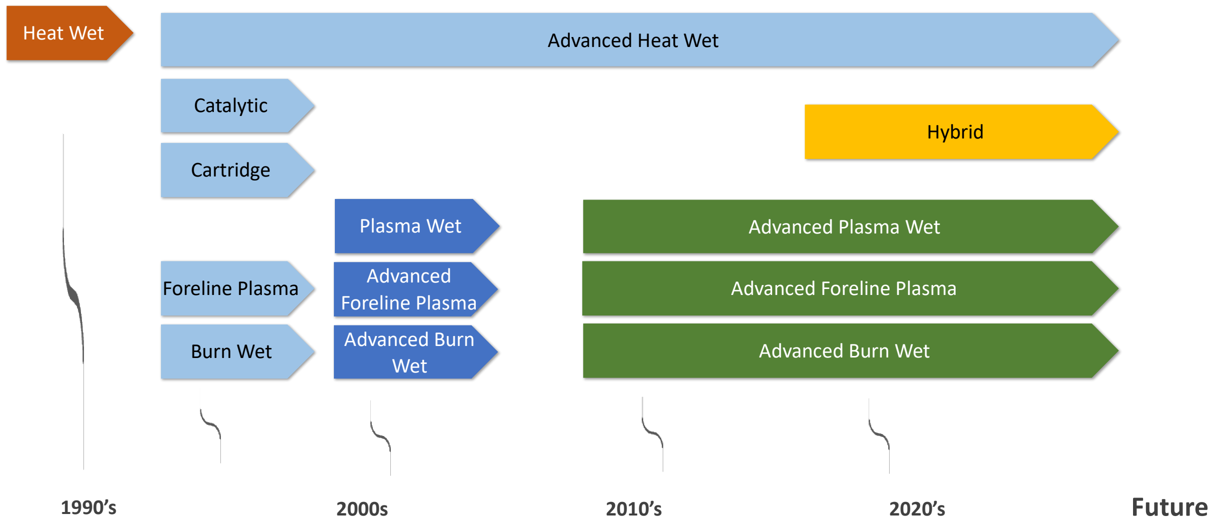


Figure 8: Semiconductor industry F-GHG abatement development timeline.

As part of their post-2010 PFC reduction goal-setting effort, the WSC developed "Best Practice Guidance for Semiconductor PFC Emission Reduction" (WSC, World Semiconductor Council PFC Working Group 2017). The guidance calls for the implementation of advancements made in the previous two decades to develop and commercialize reduction methods in fabs constructed after 2011, as well as in existing fabs where feasible. As a result, both the number and efficiency of POU abatement devices have increased over the past 20 years (WSC, World Semiconductor Council PFC Working Group 2017). Table 3 shows quantified increases between 2009 and 2022.

Table 3: Industry surveys show increased installations of abatement over time.

	2009 ISMI survey (ISMI 2005)	**2022 U.S. SIA survey** (SIA 2022)
Number of fabs using POU	21	33
Total POU	1,111	>2,000
Maximum POU per fab	158	>500

The Intergovernmental Panel on Climate Change (IPCC) acknowledges the impact of abatement technologies in its “IPCC 2019 Refinement” (Beu, Raoux, et al. 2019). Table 6.16 in that document lists abatement technologies capable of abating semiconductor process GHG emissions and the specific gases that each technology can abate (Beu, Raoux, et al. 2019).

Semiconductor manufacturers and abatement suppliers have performed thousands of DRE measurements under actual or simulated process conditions, and provided the data to the IPCC so that they could develop updated default DRE factors (see Table 6.17 in the 2019 document) (Beu, Raoux, et al. 2019). Default values range from 89% for CF_4 (the most difficult fluorocarbon to abate) to 95% to 99% for other fluorocarbon gases. If a fab wishes to claim a DRE that does not correspond with the default value or installs a technology not previously demonstrated, it is possible to develop site-specific DRE values through experimental data.

Abatement manufacturers continue to develop new and improved abatement technologies and, as such, it is possible to demonstrate efficacy in specific semiconductor applications with experimental data. Each POU abatement technology has additional utility use, space, cost, operation, safety, air and wastewater considerations that require application-specific evaluations (Beu 2005). Table 4 is a nonexhaustive list of technologies used to abate GHGs in semiconductor fabs.

Table 4: Process GHG emissions abatement technology and efficacy (Beu, Raoux, et al. 2019)**.**

Abatement Type	**Cartridge**	**Catalyst**	**Hot-Wet >850°C**	**Plasma**	**Combustion**
Description	Dry-bed passive scrubber with active media that is heated or operates at ambient temperature Target gas consumes active media Media must be disposed	Catalyst media catalyzes reaction with target gas(es) to form less hazardous or water-scrubbable compounds Media is not consumed but may be poisoned by other process effluent May use pre- or post-wet scrubbers	Electrically heated system Uses air, hydrogen or natural gas to enhance oxidation, followed by wet scrubbers	Plasma and reactants (water vapor, air hydrogen, oxygen) convert target gas(es) to water-scrubbable compounds May be subatmospheric (installed directly before the vacuum pump to abate concentrated etch process emissions) or post-pump (effluent diluted with a nitrogen pump purge). Could be combined with wet or cartridge scrubbers	Natural gas- or hydrogen-fueled combustion followed by dry or wet scrubbers
Demonstrated to abate HFC and PFC chemistries by inclusion in Table 6.16 of the "2019 Refinement"	Limited to c-C_4F_8, CHF_3, NF_3, SF_6, N_2O	Limited to CF_4, NF_3, SF_6, N_2O	Limited to C_3F_8, C_4F_6, c-C_4F_8, NF_3	All process GHGs	All process GHGs

Additionally, quantifying baseline emissions and reductions requires the development of standardized emissions testing guidelines and emissions estimating methodologies. The industry and the U.S. EPA developed consensus process emission characterization and DRE protocols to ensure consistency in measurements (Laush, Sherer and Worth 2006); (U.S. EPA 2010); (JEITA 2011); (Benaway, et al. 2014). They worked first through the WSC and then the IPCC to develop standardized emissions estimating guidelines (Bartos, et al. 2006); (Beu, Raoux, et al. 2019). Aggregating available and scientifically sound testing capabilities required industry investment and engagement with testing experts. Testing protocols required:

- The installation or modification of sampling ports on manufacturing and abatement equipment.
- The modification of utilities needed for sampling (such as electricity and nitrogen).
- The mobilization of specialized sampling equipment and sampling personnel.
- The development of data processing and analysis expertise.

The development of air emission testing protocols that support the semiconductor industry's exhaust infrastructure and emissions characteristics will take time. The U.S. EPA is "developing test methods for measuring PFAS source emissions" (U.S. EPA 2023); however, current testing methodologies do not capture the full scope of PFAS-containing materials as defined in the Semiconductor PFAS Consortium white paper, "Background on Semiconductor Manufacturing and PFAS."

Current technological trends in semiconductor manufacturing are leading to increases in the quantity and number of process chemistries. These include the PFAS-containing materials discussed in this white paper, as well as non-carbon-containing F-GHGs such as NF_3 and SF_6. Despite increases in chemical consumption, the semiconductor industry has successfully reduced PFC emissions through a combination of process optimization, substitution and abatement. Abatement will continue to serve as an important option to reduce F-GHG air emissions, which results in a corresponding reduction of PFAS air emissions.

7.0 Conclusions

Fluorocarbon chemistry has played a critical role in the evolution of semiconductor device technology. The choice of these chemicals was inextricably linked to the material systems that enabled scalability and reliability in large-scale manufacturing.

With semiconductor manufacturing highlighted as an issue of national importance in the Creating Helpful Incentives to Produce Semiconductors (CHIPS) and Science Act, the potential classification of some of these chemistries as PFAS has enormous implications, as viable alternatives do not presently exist. We have illustrated critical differences between HFCs and PFCs, which are currently subject to separate regulation, and longer-chain compounds such as PFOS and PFOA, particularly with regards to bioaccumulation potential and volatility. We have also made the case in this white paper as to why these chemistries, as employed in thin-film deposition, dry etching and chamber cleaning processes, constitute an "essential use" case.

The industry has a demonstrable history of engineering solutions to reduce both the consumption and emission of HFCs and PFCs in response to environmental concerns (WSC 1999-2014). The industry can harness a substantial knowledge base to further improve the performance of abatement systems. Incorporating environmental sustainability objectives into future roadmaps will be of increasing importance moving forward, with evaluations such as this one playing a fundamental role in such developments.

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Appendix A
Tables A-1 through A-3

Use Application for PFAS	Critical Purpose Served	PFAS-Containing Materials in Use/Unique Properties Provided	Known or Potential Non-PFAS Alternatives	Current Viability of Non-PFAS Alternatives
BEOL interconnect patterning (damascene process)	Definition of trench and via patterns in dielectric films before filling with metal	C_4F_8, C_4F_6, CF_4, CHF_3/ selectivity to mask materials, selectivity to different dielectrics (ability to stop on certain layers), profile control of trench/via sidewalls	NF_3, SF_6, CH_4, C_2H_4	Low. Combining hydrocarbons (flammable) with NF_3 (oxidizer) creates safety hazards. Creating a CF_x layer for mask selectivity requires a combination of chemistries that may not be controllable. CF_x generation as a byproduct is also guaranteed.
High-aspect-ratio channel (3D NAND)	Definition of ultra-high-aspect-ratio channel in multiple dielectric layers	C_4F_8, C_4F_6, CF_4, CHF_3/ selectivity to mask materials, selectivity to different dielectrics (ability to stop on certain layers), profile control of channel, high-etch-rate anisotropic process	NF_3, SF_6, CH_4, C_2H_4	Low. Combining hydrocarbons (flammable) with NF_3 (oxidizer) creates safety hazards. Creating a CF_x layer for mask selectivity requires a combination of chemistries that may not be controllable. CF_x generation as a byproduct is also guaranteed.
Waveguide fabrication in silicon photonics processes	Patterning of waveguides into silicon and silicon-based dielectric materials	CF_4, CHF_3, selectivity to mask materials, ability to reduce line-edge and line-width roughness of patterned features to reduce transmission losses caused by scattering	NF_3, SF_6, CH_4, C_2H_4	Low. Combining hydrocarbons (flammable) with NF_3 (oxidizer) creates safety hazards. Creating a CF_x layer for mask selectivity requires a combination of chemistries that may not be controllable. CF_x generation as a byproduct is also guaranteed.
FEOL hard mask patterning	Transfers lithographic patterns into a hard mask for subsequent definition of transistors	CF_4, CHF_3, selectivity to mask materials, ability to reduce line-edge and line-width roughness of patterned features to reduce transmission losses caused by scattering, ability to detect process endpoints from the optical emission signature of carbon-containing byproducts such as C-O and C-N	NF_3, SF_6, CH_4, C_2H_4	Low. Combining hydrocarbons (flammable) with NF_3 (oxidizer) creates safety hazards. Creating a CF_x layer for mask selectivity requires a combination of chemistries that may not be controllable. CF_x generation as a byproduct is also guaranteed. Endpoint detection may be complicated because of secondary reactions.

Use Application for PFAS	**Critical Purpose Served**	**PFAS-Containing Materials in Use/Unique Properties Provided**	**Known or Potential Non-PFAS Alternatives**	**Current Viability of Non-PFAS Alternatives**
FEOL spacer patterning	Define spacer structures (dielectric encapsulation that protects the sidewalls of transistor features)	CHF_3/high selectivity to transistor gate materials and underlying substrate	CH_3F, other molecules with fewer than two fluorine atoms	Low. Limited data on alternate chemistries such as C_4H_9F, CH_3F performance. Byproducts will contain CF_x.
Through-silicon via etch	Create deep via structures through entire wafers for packaging applications	C_4F_8, C_4F_6/thermal resistance, inertness toward aggressive chemicals, nonflammability, low vapor pressure and offgassing at high operating temperatures and low pressures, good stick-slip behavior	SF_6, CH_3F, CH_4, C_2H_4	SF_6 is already employed as an etchant. There are currently no assessments for the effective polymer deposition of CH_3F. CH_4 and C_2H_4 are flammable, which create additional hazards. Potential for CF_x formation by mixing SF_6 and CH_x.
Cleaning processes for CVD and PVD chambers	Remove deposit buildup on chamber walls to ensure reproducibility and prevent yield loss caused by contamination	CF_4, C_2F_6, C_3F_8	NF_3, F_2	NF_3 is a common alternative (see the Thin-Film Deposition Chamber Clean Use section); however, it is possible to generate CF_x byproducts when incorporating carbon into low-k dielectrics.
Deposition precursors for ALD	Improved volatility and stability of ligands for the uniformity of metal deposition and reproducibility of processes	Transition metal compounds containing the tfac (1,1,1-trifluoro-2,4-pentane-dionate) and hfac (1,1,1,5,5,5-hexafluoro-2,4-pentane-dionate) ligands	No known viable alternatives	N/A
Surface treatment processes for area-selective ALD processes	Remove metal-oxide contaminants from surfaces before deposition		Unknown	Mechanisms need investigating

Table A-1: Purpose and properties of PFAS-containing materials for plasma etch, chamber clean and deposition in semiconductor manufacturing.

Chemical Formula	**Chemical Name**	**Chemical Abstracts Service (CAS) Number**	**Boiling Point in Celsius (°C)**	**Log K_{ow}**
CF_4	Tetrafluoromethane (R14)	75-73-0	–128	1.18
CH_2F_2	Difluoromethane (R32)	75-10-5	–52	0.21
C_2F_6	Hexafluoroethane (R116)	76-16-4	–78	2
CHF_3	Trifluoromethane (R23)	75-46-7	–82	0.64
C_3F_8	Octafluoropropane (R-218)	76-19-7	–37	2.82 (estimated)
c-C_4F_8	Octafluorocyclobutane (RC318)	115-25-3	–6	0.43 (estimated)
$C_8HF_{15}O_2$	PFOA	335-67-1	189	5.3
$C_8HF_{17}O_3S$	PFOS	1763-23-1	145	6.3

Table A-2: CAS number, boiling points and log K_{ow} for common PFAS-containing materials used in the semiconductor industry with PFOA/PFOS values for comparison. Estimated values from (PubChem 2023)**.**

Treatment Method	**Effective for HFCs or PFCs?**	**Example Reactions**	**Other Releases**
Chemisorption absorber	No	Reactive gases only – no PFC/HFC treatment	
Physisorption absorber	No	Reactive gases only – no PFC/HFC treatment	
Wet scrubbing	No	Used to treat acid gases and passes PFCs $SiF_4(g) + 2F_2(g) + 2H_2O(l) + CH_3F(g) + CF_4(g) = 2HF(ia) + H_2SiF_6(ia) + O_2(g) + CH_3F(g) + CF_4(g)$	Wastewater requires adjusting the pH
Hot chemisorption absorber	Yes	High-temperature reaction of calcium oxide, only for reactive PFCs (for example, NF_3) $1.5SiF_4(g) + 3F_2(g) + 8CaO(s) + CH_3F(g) + CF_4(g) = 6.5CaF_2(s) + 1.5CaSiO_3(s) + CO_2(g) + 1.5H_2O(g) + CF_4(g)$	Exhaust requires the additional treatment of hazardous air pollutants Possible hazardous waste disposal required

Treatment Method	Effective for HFCs or PFCs?	Example Reactions	Other Releases
High-temperature oxidative catalyst plus scrubber	Yes	Often preceded with wet scrubber to protect the catalyst $3O_2(g) + 2CH_3F(g) + CF_4(g) = 6HF(g) + 3CO_2(g)$	Exhaust requires the additional treatment of hazardous air pollutants Wastewater requires adjusting the pH Possible hazardous waste disposal required
High-temperature hydrolytic catalyst plus scrubber	Yes	Often preceded with a wet scrubber to protect the catalyst POU and end of pipe offered $2H_2O(g) + CF_4(g) = 4HF(g) + CO_2(g)$	Exhaust requires the additional treatment of hazardous air pollutants Wastewater requires adjusting the pH Possible hazardous waste disposal required
Heat wet	In some cases	Reactive PFCs only Sometimes augmented by fossil fuel $SiF_4(g) + 3F_2(g) + 2H_2O(l) + CH_3F(g) + CF_4(g) = H_2SiF_6(ia) + 5HF(ia) + CO_2(g) + CF_4(g)$	Exhaust requires the additional treatment of hazardous air pollutants Wastewater requires adjusting the pH
Burn wet	Yes	Flame energy and type can vary for different PFCs; for example, high energy for CF_4, lower energy for CH_3F $4SiF_4(g) + 4F_2(g) + 3CH_4(g) + 4O_2(g) + CF_4(g) = 4H_2SiF_6(ia) + 4HF(ia) + 4CO_2(g)$	Exhaust requires the additional treatment of hazardous air pollutants Wastewater requires adjusting the pH
Plasma (foreline and exhaust plasma and wet scrubber)	Yes	Plasma energy can vary for different PFCs; for example, high energy for CF_4, lower energy for CH_3F $3O_2(g) + 2CH_3F(g) + CF_4(g) = 6HF(g) + 3CO_2(g)$ or $2H_2O(g) + CF_4(g) = 4HF(g) + CO_2(g)$	Exhaust requires the additional treatment of hazardous air pollutants Wastewater requires adjusting the pH
Wet – heat – wet	In some cases	As per thermal wet – prewet, used to remove etch byproducts such as SiF_4 to improve the abatement mean time between service (MTBS) Carbon compounds may dissolve in the wet stage	Exhaust requires the additional treatment of hazardous air pollutants Wastewater requires adjusting the pH

Treatment Method	**Effective for HFCs or PFCs?**	**Example Reactions**	**Other Releases**
		$3SiF_4(g) + 3F_2(g) + 2H_2O(l) + CH_3F(g) + CF4(g) = [WS\ 2H_2SiF_6(ia) + SiO_2] + [HW\ CF_4(g) + 3F_2(g) + CH_3F(g) + 2H_2O(l) = 7HF(ia) + CO_2(g) + CF_4(g)]$	
Wet – burn –wet	In some cases	As per burn wet – prewet, used to remove etch byproducts such as SiF_4 to improve the abatement MTBS Carbon compounds may dissolve in the wet stage $3SiF_4(g) + 4F_2(g) + 2H_2O(l) + CF_4(g) = [WS\ 2H_2SiF_6(ia) + SiO_2] + [BW\ 4F_2(g) + CF_4(g) + 3CH_4(g) + 4O_2(g) = 12HF(ia) + 4CO_2(g)]$	Exhaust requires the additional treatment of hazardous air pollutants Wastewater requires adjusting the pH
Wet – plasma – wet	In some cases	As per plasma wet – prewet, used to remove etch byproducts such as SiF_4 to improve abatement MTBS Carbon compounds may dissolve in the wet stage $3SiF_4(g) + 3F_2(g) + 2H_2O(l) + CH_3F(g) + CF_4(g) = [WS\ 2H_2SiF_6(ia) + SiO_2] + [HW\ 3F_2(g) + CH_3F(g) + CF4(g) + 4H_2O(l) = 11HF(ia) + 2CO_2(g)]$	Exhaust requires the additional treatment of hazardous air pollutants Wastewater requires adjusting the pH

Table A-3: Common technologies for the treatment of HFCs and HFCs.

Appendix B
Case Study: 200-mm Conversion to NF_3 Remote Plasma Clean for Thin-Film Chamber Cleans

NF_3, as a replacement for carbon-based cleans, has been an accepted alternative for the past 20 years. Newer semiconductor fabs using 300-mm wafer processing technology almost exclusively use NF_3 as the sole chamber clean gas, and most use a remote radio-frequency power source for almost 98% dissociation of NF_3 for high efficiency.

Initially, the thought was that 300-mm wafer fabs would soon replace 200-mm fabs, but market conditions have dictated the continued operation of many 200-mm fabs. One wafer fab, located in Dallas, Texas, and operated by Texas Instruments, began converting 200-mm tools using carbon-based cleans to NF_3 remote plasma clean systems in 2017. Although this effort focused more on reducing GHG emissions, metric tons of carbon dioxide-equivalent emissions are directly analogous to reductions in PFAS-containing materials when discussing HFCs and PFCs.

Figure B-1 shows the decrease in GHG emissions since conversions began in 2017, with C_2F_6 emissions decreasing 60% over a 5-year period and CF4 emissions decreasing 35%.

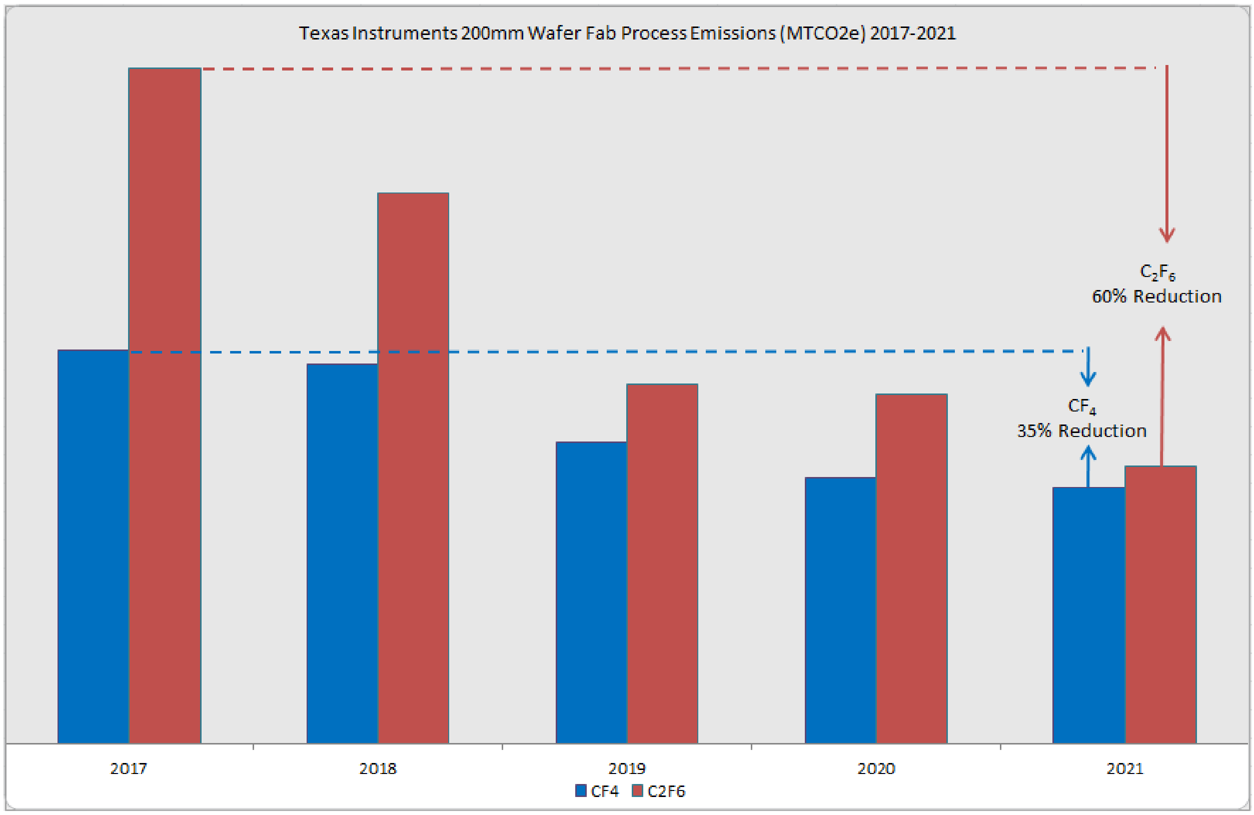

Figure B-1: Reduction of PFAS-containing materials through the retrofitting of 200-mm thin-film chamber cleans to remote plasma systems. The reduction of CF_4 may be greater than 35% because of U.S. EPA Subpart I emission factors for CF_4 generation. While many factors affect emissions, including production and variable product mix, reductions in PFAS-containing materials are significant over these other effects.