SEMICONDUCTOR INDUSTRY ASSOCIATION

Comments of the
Semiconductor Industry Association (SIA)
to the
CHIPS Program Office (CPO)
on the
Draft Programmatic Environmental Assessment (PEA) for Modernization and Internal Expansion of Existing Semiconductor Fabrication Facilities under the CHIPS Incentives Program

Submitted February 9, 2024

The Semiconductor Industry Association (SIA)[1] appreciates the opportunity to submit these comments to the CHIPS Program Office (CPO) of the Department of Commerce ("the Department" or "Commerce") in response to the draft programmatic environmental assessment (PEA)[2] for the modernization and internal expansion of existing semiconductor fabrication facilities under the CHIPS Incentives Program.

SIA appreciates the Department's efforts to streamline the environmental review of CHIPS projects under the National Environmental Policy Act (NEPA). In order to achieve the national security, economic growth, and supply chain resiliency objectives of the CHIPS Incentives Program, it is essential for CHIPS-funded projects to be constructed in a timely manner. As Secretary of Commerce Gina Raimondo stated in testimony last October to the Senate Committee on Commerce, Science, and Transportation: "These are national security imperative projects. […] Environmental concerns matter. We are not in any way suggesting we should do anything that hurts the environment or is unsustainable. That being said, we do need to […] streamline the process, speed the process, make the process more efficient and user friendly."[3]

In general, the PEA provides an accurate description of chip manufacturing and associated environment, health, and safety (EHS) controls. It extensively references respected industry sources regarding semiconductor manufacturing and EHS protections in the fabrication process. SIA offers some suggested points to further improve the accuracy of the document, and we appreciate CPO's extensive efforts to reflect the industry's ongoing commitment to protecting workers, communities, and the environment.

SIA also notes some topics in the PEA that would benefit from clarification or elaboration, and SIA suggests CPO address circumstances under which certain projects

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[1] The Semiconductor Industry Association (SIA) is the voice of the semiconductor industry, one of America's top export industries and a key driver of America's economic strength, national security, and global competitiveness. SIA represents 99% of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. chip firms. Through this coalition, SIA seeks to strengthen leadership of semiconductor manufacturing, design, and research by working with Congress, the Administration, and key industry stakeholders around the world to encourage policies that fuel innovation, propel business, and drive international competition. Learn more at www.semiconductors.org.

[2] Draft PEA. *Available at:* https://www.nist.gov/system/files/documents/2023/12/26/CHIPS%20Modernization%20Draft%20PEA.pdf

[3] Senate Commerce Hearing. *Available at:* https://www.commerce.senate.gov/2023/10/chips-and-science-implementation-and-oversight

are excluded from the definition of a major Federal action. Alternatively, SIA suggests CPO consider on a case-by-case basis whether a given project rises to the level of a major Federal action.

SIA offers comments on the below topics to CPO:

1. **The projects within scope of the draft PEA should not automatically trigger NEPA review.**

While SIA appreciates the goal of the PEA in streamlining reviews under NEPA, it is unclear whether the projects covered by the PEA should be subject to Federal environmental review. SIA urges the CPO to evaluate whether the projects covered under the PEA are properly characterized as "major federal actions" within the scope of NEPA.

The programmatic scope under Section 1.1 includes "actions associated with modernization and internal expansion at existing current-generation and mature-node semiconductor fabrication facilities." CPO also notes that "such projects include the replacement or upgrade of existing equipment, the addition of new semiconductor manufacturing equipment within the existing facility footprint, and expansion of cleanroom space."[4] Section 2.1 of the PEA specifically lists five possible activities within the scope of the proposed action:[5]

- Replacing existing equipment
- Upgrading of existing equipment
- Adding new semiconductor manufacturing equipment
- Expanding cleanroom space and adding new cleanroom equipment
- Disposing of equipment that is replaced

A major Federal action is defined as "an action that the agency carrying out such action determines is subject to substantial Federal control and responsibility." 42 USC § 4336e(10)(A). The definition excludes those non-Federal actions "(I) with no or minimal Federal funding; or (II) with no or minimal Federal involvement where a Federal agency cannot control the outcome of the project;" and "loans, loan guarantees, or other forms of financial assistance where a Federal agency does not exercise sufficient control and responsibility over the subsequent use of such financial assistance or the effect of the action." Id. at § 4336e(10)(B)(i), (iii). The projects covered under the PEA must be for the modernization or internal expansion of an existing, currently operating facility. Unlike many other major Federal actions where the agency is providing a large percentage of the project cost, the Department of Commerce expects to provide to covered entities awards for these projects which "range between 5-15% of project capital expenditures."[6]

[4] Draft PEA, at 2
[5] Draft PEA, at 4
[6] CHIPS Notice of Funding Opportunity (NOFO) for Commercial Fabrication Facilities, at 11. *Available at:* https://www.nist.gov/system/files/documents/2023/06/23/CHIPS-Commercial%20Fabrication%20Facilities%20NOFO%20Amendment%201.pdf

SIA believes that such a range reflects a minimal amount of Federal funding. Moreover, while the Federal incentives are an important part of ensuring that the project takes place in the U.S. and can serve to accelerate project timing or expand project scale, these incentives are a small amount relative to the total project cost.

Given that the amount of the federal incentive payment is expected to be for only a small percentage of the overall project cost, it is far from clear that the Department of Commerce would have "*substantial* Federal control *and* responsibility" over a project undertaken by a private entity, such as those at a currently operating semiconductor fabrication facility. This is particularly the case where the applicant would proceed with the project even in the absence of federal funding. SIA is not aware of any documentation by the Department of Commerce that demonstrates such "substantial" control and responsibility. Moreover, a 5-15% cost share is unlikely to meet the standards established by the courts for a project to be federalized and deemed a major Federal action.[7]

In the context of the CHIPS Act, the first award announced by CPO is illustrative. At the BAE Systems facility in Nashua, NH, CPO will provide approximately $35 million in incentives for a modernization project that will replace aging tools.[8] Approximately 85-95% of the purchase and installation of semiconductor manufacturing equipment at this location will be funded through sources outside of CHIPS funding, including private funds. Outside of the provision of funds, the Department of Commerce is not responsible for any aspect of the project. Even if Commerce believes it exerts control over its specific use of funds, it would only be responsible for a fraction of a project, such as shares of certain pieces of equipment, which then only represent a fraction of the total output of the whole facility. SIA does not believe this meets the bar of "substantial Federal control and responsibility," and that the types of projects described in the PEA are likely to be non-major Federal actions that do not trigger a NEPA review.

At minimum, CPO should assess on a case-by-case basis whether a particular project falling within the scope of the PEA should be characterized as a major federal action before applying the PEA to a project or requiring the preparation of a project-specific EA. Making a proper determination regarding NEPA applicability is important in light of limited agency resources and will allow CPO and applicants to focus those limited resources.

SIA notes that the Council on Environmental Quality (CEQ) is currently undertaking its phase 2 rulemaking regarding its implementing regulations for NEPA based on the amendments made as part of the Fiscal Responsibility Act. In the meantime, CEQ

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[7] While there is no precise formula for determining whether a specified amount of funding constitutes a major federal action that triggers NEPA review, federal courts have evaluated the level of funding to determine whether it is sufficient to trigger NEPA review. See, e.g., Tourtt v. NASA, 485 F. Supp. 23 38 (D.R.I. 2007) (A project receiving 18% of its funding from the federal government is not a "major federal action" where the funding agency "could not exercise discretion and control over the design, location or choice of alternatives for the non-federally funded portions.").

[8] CHIPS Funding Updates. *Available at:* https://www.nist.gov/chips/funding-updates

states that "Federal agencies are responsible for determining how the amendments apply to their ongoing NEPA reviews and should consider congressional intent to facilitate more efficient NEPA analysis when making this determination."[9]

In the event Commerce determines a NEPA review is needed for such projects, it should make its best effort to reduce or eliminate the need for such a review through agreements with applicants regarding implementation of best management practices. Any site-specific review would be unnecessary based on the contours of the agreement between CPO and the covered entity to, where applicable, utilize best available technologies and implement best management practices that address climate change and climate resilience, utilities, air quality, water quality, human health and safety, hazardous and toxic materials, hazardous waste and solid waste management, and/or environmental justice.[10]

2. **Commerce should modify the PEA to reflect a number of items in need of correction, clarification, or elaboration.**

The PEA provides a comprehensive view of semiconductor manufacturing and accurately determines that it is not likely that significant environmental impacts would occur as a result of the proposed action. Nonetheless, SIA would like to bring to the attention of the CPO a few items that should be corrected, clarified, or elaborated in the PEA:

Section 2.0

SIA encourages Commerce to state a case for limiting the range of alternatives to proposed action and no action by describing its review of the technical and economic feasibility of any alternative considered and rejected for detailed consideration.

Section 2.1

A. **Inclusion of additional types of activities for which there is no new land disturbance after the major Federal action commences**

SIA agrees that the lack of land disturbance is an appropriate threshold for the PEA. Accordingly, the PEA should be expanded to include other types of projects for which there is no additional land disturbance as a result of Federal funds being awarded. This would require revising the PEA to accommodate expansions and new facilities and buildings on an existing footprint with disturbed land.

In the list of activities included in scope of the PEA, Commerce should add a bullet for construction of new buildings (e.g., fabs, etc.) on an existing facility footprint. This aligns with Commerce's stated intent to include within the scope of the PEA only those

[9] Amendments to NEPA from the Fiscal Responsibility Act of 2023. *Available at:* https://ceq.doe.gov/laws-regulations/fra.html
[10] Draft PEA, Appendix A, at A-1

projects that do not result in any new land disturbance. CPO already includes such activities under 2.4.2 when it states:

> "All of these improvements to auxiliary process support infrastructure must occur on previously disturbed spaces within the existing facility footprint, such as existing concrete pads or other areas already significantly modified from the previous natural state (e.g., conversion of a parking lot space into a gas tank storage space would be covered as the area being modified had previously been converted from includes natural state to a human-made structure.)"

The construction of a new facility on a previously disturbed space should be explicitly included as within scope of the PEA rather than limiting the PEA to work undertaken within existing facilities.

This is necessary to accommodate within the PEA those projects involving ongoing or completed construction activities on an existing footprint. This should be inclusive of any area of disturbance as of the date NEPA analysis begins and include permitted disturbance. For disturbance for which a permit is pending, the CPO should rely on the NEPA analysis of the jurisdictional agency.

A corresponding change would be necessary under 2.4 to include within the types of activities under the proposed action the construction of new facilities on previously disturbed land within the existing footprint of the facility. Likewise, the PEA would need to be revised to reflect that expansions need not necessarily be *internal* – or, alternatively, that modifying a space that had been previously been converted from its natural state to a human-made structure would fall under scope of *internal.*

B. Inclusion of other node sizes and the full range of semiconductor manufacturing activities

The scope of the PEA should not be limited to current-generation and mature-node facilities that manufacture semiconductors. SIA instead recommends the PEA should cover all projects involving the modernization or expansion of semiconductor manufacturing facilities, regardless of the node size. This would include facilities for the manufacturing of leading-edge semiconductors and semiconductor back-end production facilities.[11] These activities are substantially similar to those processes for older nodes

[11] As defined in the NOFO, at 5-6:

- "Leading-Edge Facilities for logic or memory that utilize the most advanced front-end fabrication processes which achieve the highest transistor and power performance. For logic, this currently includes facilities that produce semiconductors at high volumes using extreme ultraviolet (EUV) lithography tools. For memory, this currently includes facilities capable of producing 3D NAND flash chips with 200 layers and above, and/or dynamic random-access memory (DRAM) chips with a half-pitch of 13 nm and below.
- "Back-end Production Facilities for the assembly, testing, or packaging of semiconductors that have completed the front-end fabrication process. This category includes advanced packaging of semiconductors. The Department is particularly interested in projects that ensure competitive operating costs within the United States (e.g., through automation)."

CPO may also consider a PEA for the modernization or expansion of facilities for semiconductor manufacturing equipment and semiconductor materials, though this would require additional documentation for the different manufacturing processes.

and the PEA does not set forth a justification for restricting the PEA to current-generation and mature nodes.

Commerce provides in the PEA a comprehensive analysis of the semiconductor manufacturing process as a general matter, without specific reference to node size. The document fails to support the contention that these environmental effects are unique to current-generation and mature-node manufacturing. SIA does not believe that there will be a categorical distinction between the environmental assessment of a facility based strictly on node size or between front-end and back-end processes. Instead, the environmental impacts are generally based on other variables, such as the size of the project. Therefore, the scope of the PEA should be expanded to include leading-edge manufacturing and back-end manufacturing.

SIA believes that wafer production should also be included within scope of the PEA as a standalone facility activity. Wafer production includes, but is not limited to, the processes of crystal growth, wafer slicing, polishing, cleaning, epitaxial deposition, bonding and metrology. CPO states that semiconductor wafer production already could be included in the scope of the PEA if it "occurs at the same facility as chip production" (Section 2.2.2), but it is not included if the facility is "dedicated solely to wafer production." CPO should recognize that in today's semiconductor ecosystem, only a trivial amount of wafer production takes place at the same facility as a chip. Chip manufacturers outsource this step to wafer manufacturers. It reasons that the PEA should cover this important process in all cases, regardless of whether any semiconductor wafer production process step is co-located with the other steps of semiconductor manufacturing. After all, CPO expanded the definition of semiconductor manufacturing to include "wafer production, semiconductor fabrication, or semiconductor packaging"[12] and further notes that "the semiconductor chip manufacturing process begins with wafer production."[13] If CPO is unable to revise the scope of the PEA to include wafer production, SIA encourages CPO to develop a similar PEA for wafer production facilities.

C. Action area / geographic scope

The PEA states that the action area encompasses states with existing facilities. SIA appreciates Commerce's utilization of SIA's semiconductor ecosystem map for the purpose of illustrating the distribution of existing facilities in the U.S. However, the PEA notes that Figure 2.1-1 does not reflect an exhaustive list of existing facilities. CPO should also include the private establishments identified by the Bureau of Labor Statistics under NAICS code 334413 for semiconductor and related device manufacturing. BLS identifies, as of June 2023, almost 2400 existing manufacturing establishments across 34 states.[14] By comparison, the SIA map only includes 22 states,

[12] 15 CFR Part 231, Subpart A, §231.116
[13] Draft PEA, at 7
[14] BLS data available at: https://data.bls.gov/cew/apps/table_maker/v4/table_maker.htm#type=0&year=2023&qtr=2&own=5&ind=334413&supp=0

and, for example, does not include the BAE facility that is the subject of the first CHIPS award. However, the BLS reporting does not include those states with suppressed employment and wages – meaning that it excludes some of the states identified by SIA, including Delaware, Kansas, Maine, Virginia, and Vermont. Therefore, the geographic scope should reflect at least the 39 states with establishments documented by SIA or BLS, and potentially others.

Section 2.2.2

CPO states that the chipmaking process "begins with wafer production." As SIA has previously commented to CPO, the first step of semiconductor manufacturing should be defined as the production of semiconductor-grade polysilicon and compound semiconductor substances, such as silicon carbide and gallium nitride. SIA also notes that semiconductor-grade polysilicon is typically 99.99999999999 percent pure,[15] rather than the 99.999 percent indicated in the PEA. Accordingly, CPO may also consider including within scope facilities for the production of semiconductor-grade polysilicon and compound semiconductor substances.

Section 2.3

The CHIPS funds provided by Commerce are incentives to companies to expand their U.S. manufacturing operations, and as part of its decision-making process, Commerce states in the NOFO that it intends to consider the "degree to which the request for CHIPS Incentives is reasonable and necessary to make the project viable in the United States."[16] The PEA states that the no action alternative "assumes that the applicant would not complete the proposed modernization/expansion project, and the facility would continue production at the same rate, using the same equipment, and within its existing facility footprint."[17]

SIA believes this assumption should be amended to reflect that the project could still occur to some degree even in the absence of CHIPS Act funding, based on a variety of factors, including the Advanced Manufacturing Investment Credit[18] and various state and local incentives. CHIPS funds, while a vastly important factor, may not be the sole determining factor in whether a project may proceed in some form. The PEA would therefore benefit from considering an intermediate range of outcomes under the no action alternative that contemplate whether project may instead be deferred, delayed, slowed, or scaled down. Alternatively, even if the analysis of the no action alternative proceeds on the premise that a project would not move forward, the PEA should still acknowledge that a range of outcomes are possible if CPO decides not to award CHIPS funding.

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[15] White House 100-day Review under EO 14017, "Building resilient supply chains, revitalizing American manufacturing, and fostering broad-based growth." Available at: https://www.whitehouse.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf

[16] NOFO, at 63

[17] Draft PEA, at 16

[18] Internal Revenue Code §48D.

Therefore, in some cases, it is possible that there is no difference between the environmental effects of the no action alternative and the proposed action alternative. In other cases, there would be a difference. CPO should allow for the full range of possible outcomes under the PEA.

Please note this comment on the no action alternative applies throughout the draft PEA, including such sections as 3.4.2.1, 3.5.2.1, 3.6.2.1, 3.7.2.1, 3.8.2.1, 3.9.2.1, 3.10.2.1, 3.11.2.1, 3.12.2.1, and table 3.13-1.

Section 2.4

The PEA states that "an applicant must demonstrate compliance with all existing facility permits." SIA suggests clarifying that an applicant must demonstrate substantial compliance with permits. It is possible that for some years- or decade- old permits there could be reporting or bookkeeping items that arise, but that do not have any environmental effect.

SIA also suggests clarifying that applicant may agree to implement appropriate best management practices (BMPs) to avoid converting procedural, non-effects-based BMPs into regulatory standards. This comment would apply to other sections of the PEA, such as 3.5.2.2 and 3.6.2.2.

Section 3.0

For some of the topics considered under this section regarding affected environment and environmental consequences, SIA would encourage CPO to update the draft PEA in order to ensure it applies to the range of projects as intended by CPO.

- Regarding impacts to terrestrial biological resources, SIA recommends requiring that a proposed action be covered if it will have at most *negligible effects* on terrestrial vegetation, terrestrial wildlife, terrestrial biological resources, or terrestrial special status species such as migratory birds.

- Regarding impacts visual resources, SIA recommends that a proposed action be covered if it will have at most *negligible effects* on visual resources.

- Regarding transportation and traffic, SIA recommends that the PEA cover projects where anticipated operational change in peak and average daily traffic either: 1) falls below any local, state, and federal thresholds for conducting a TIA or equivalent study, or 2) a traffic study has been completed and traffic can be accommodated with existing or planned infrastructure improvements.

- Regarding wetlands and floodplains, SIA recommends that the PEA cover projects where equipment modernization and expansion will occur within land within the existing footprint of the facility, inclusive of any area of disturbance as

> of the date NEPA analysis begins, and including permitted wetland disturbance or disturbance for which a wetland permit is pending. For disturbance for which a wetland permit is pending, the CPO should rely on the NEPA analysis of the jurisdictional agency.

Section 3.2

SIA recommends the first sentence of the paragraph should be revised as below:

> The environmental consequences analysis considers how the condition of a resource may change as a result of implementing the **alternative** ~~two alternatives~~ …

Section 3.2.1

The citations identified in this section regarding direct and indirect effects are to CEQ's 1978 regulations that were superseded in 2020 and amended by CEQ in 2022. The current CEQ definition of "effects" is found at 40 CFR 1508.1(g):

> Effects include ecological (such as the effects on natural resources and on the components, structures, and functioning of affected ecosystems), aesthetic, historic, cultural, economic, social, or health, whether direct, indirect, or cumulative. Effects may also include those resulting from actions which may have both beneficial and detrimental effects, even if on balance the agency believes that the effects will be beneficial.

SIA suggests CPO update this section to address these amendments to regulation. The preceding and following discussion does not address the difference between the 1978 regulations and the current ones to allow Commerce to rely on "context" and "intensity" of the 1978 regulations, despite the fact that it has been amended.

Section 3.4

As documented in numerous third-party reports, semiconductors are key to a decarbonized economy and the fight against climate change. This section would benefit from considering the positive effects of semiconductor manufacturing through its increased "handprint," which enables other sectors to reduce their carbon emissions and environmental impact. The 2022 Joint Statement of the World Semiconductor Council (WSC)[19] notes: "The deployment of semiconductor-enabled technologies has empowered energy efficiency improvements, accelerated renewable energy, minimized

[19] The World Semiconductor Council (WSC) is an international forum that brings together industry leaders to address issues of global concern to the semiconductor industry. Comprised of the semiconductor industry associations (SIAs) of the United States, Korea, Japan, Europe, China and Chinese Taipei, the goal of the WSC is to promote international cooperation in the semiconductor sector in order to facilitate the healthy growth of the industry from a long-term, global perspective. It also supports expanding the global market for information technology products and services and promoting fair competition, technological advancement, and sound environmental, health and safety practices.

emissions and waste, and revolutionized the way the economy functions in the digital age." For this reason, the World Economic Forum estimates that semiconductor-enabled technology can reduce GHG emissions by 15 percent, which is almost one-third of the 50 percent reduction required by 2030.[20] SIA incorporates by reference a 2023 white paper from the WSC titled, "Semiconductors Enabling Carbon Emissions Reductions."[21]

The exact kinds of modernizations and expansions contemplated by the draft PEA, and the CHIPS Act in general, are the types of projects that will develop and manufacture chips that are more advanced and more efficient – chips that are necessary inputs for carbon-intensive industries throughout the economy to reduce their carbon footprint. This includes industries such as energy production and transmission, automotive and electric vehicles, smart buildings and appliances, telecommunications and connectivity, and data centers and high-performance computing.

For this reason, for every unit of Scope 1 or Scope 2 emissions generated by the semiconductor industry, it has helped avoid 5 times more emissions for end-users.[22] The World Economic Forum notes that scaling up digitalization in high-emissions industries can reduce greenhouse gas emissions by up to 20% by 2050, offering a significant contribution to achieving a net-zero trajectory.[23]

CPO should consider this important aspect of the semiconductor industry in its analysis of impact on climate change, as well as in the summary of cumulative effects discussed in Section 4.5.

Section 3.4.1.2

This section describes the use of Continuous Emissions Monitoring Systems (CEMS) to measure process and combustion GHG emissions. Semiconductor manufacturing facilities and processes are extremely complex and CEMS are not a viable option. Instead, both the EPA in the GHG reporting rule and the IPCC 2019 refinement of Volume 3 Chapter 6 provide Tier 2 methods to estimate process GHG emission through use of default emission factors and abatement destruction/removal efficiency values applied to gas consumption. Fluorinated heat transfer fluid emissions are estimated using a mass balance approach.

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[20] World Economic Forum, "Digital technology can cut global emissions by 15%. Here's how", 2019 (https://www.weforum.org/agenda/2019/01/why-digitalization-is-the-key-to-exponential-climate-action/)
[21] World Semiconductor Council, Joint Statement May 2023, Annex 1. Available at: https://www.semiconductorcouncil.org/wp-content/uploads/2023/06/WSC-2023-Joint-Statement-FINAL-with-Annex-1.pdf#page=17
[22] Goldman Sachs Asset Management, "Green Capex: Capturing the Opportunities." Available at: https://www.gsam.com/content/gsam/us/en/institutions/market-insights/gsam-connect/2022/Green_Capex_Capturing_the_Opportunities.html
[23] World Economic Forum, "How digital solutions can reduce global emissions," 2022. Available at: https://www.weforum.org/agenda/2022/05/how-digital-solutions-can-reduce-global-emissions/

Section 3.4.2.2

If practical, SIA would recommend CPO supplement this section with additional quantitative analysis that demonstrates the proposed action would have negligible to minor, long-term, global effect on climate change from GHG emissions.

For example, CPO mentions in Section 4.3, “The semiconductor industry in the U.S., through its direct, onsite emissions from manufacturing processes and offsite fossil energy used to generate the electricity it consumes is estimated to contribute approximately 0.18 percent of aggregate annual U.S. greenhouse gas emissions (GHG) or approximately 11.5 million metric tons (MMT), expressed in CO2e.” This acknowledgement that the semiconductor industry represents such a small share of GHG emissions should be included in this section.

Accordingly, any increase in GHG as a result of manufacturing growth in the semiconductor industry for projects included in the PEA would likely result in negligible effects.

Section 3.5.1.2

The information in this section is based on references from 2001 and 1994, which may be outdated and may not reflect current semiconductor operations. This section should be updated, and experts at SIA member companies would be happy to provide additional information to assist in this effort.

Section 3.5.1.3

This section would benefit from discussions with SIA company air experts to ensure its accuracy. The abatement systems described are central units that abate high volume, low concentration streams. Figure 3.5.1 has little to do with air abatement technology but instead is focused on reducing a facilities Scope 1 and 2 CO2 equivalent emissions. Accordingly, SIA recommends CPO remove Figure 3.5-1.

Section 3.5.2.2

Where possible and applicable, this section would benefit from supplementary quantitative analysis that details the potential impact on air emissions in order to reach the determination that these effects would be “adverse and negligible compared to current conditions, but they could be beneficial and minor” if relevant mitigation and best management practices occurred.

Section 3.6.1.2

This section would benefit from discussions with SIA member companies to ensure its accuracy. Specific chemistries are characterized as “wastewater” with no description of their concentrated waste stream and its treatment or disposal. No mention is made of

industrial wastewater (IWW), the drain commonly used for certain acids, bases, corrosive aqueous formulations, such as TMAH developer, and ultrapure water rinses. IWW is treated on-site in an elementary neutralization.

TARCs are highlighted as the largest single source of PFAS in semiconductor manufacturing and that TARCs contribute a large portion of the PFAS found in wastewater discharges.[24] Page 39 incorrectly states: "some facilities send approximately 40 percent of waste antireflective coating (containing PFAS) to wastewater treatment facilities." Antireflective coatings are either organic formulations or aqueous. Organic ARCs drain to solvent waste and are sent offsite where they are burned as fuel in a cement kiln or disposed via hazardous waste incineration. Aqueous top ARCs are typically sent to industrial wastewater.

Section 3.6.2.2

Additional discussion or quantitative analysis would be helpful to support CPO's determination that the effects would be adverse and minor compared to current conditions, or potentially beneficial and minor, depending on the new measures to reduce the pollutant load in the wastewater.

Section 3.7.1.1 / 3.7.1.2 / 3.7.1.5

CPO should expand its discussion of current industrial hygiene (IH) operations in semiconductor manufacturing to reflect the full range of the current industry practice. For example, IH professionals use the American Conference of Governmental Industrial Hygienists (ACGIH)[25] threshold limit values (TLVs) as the starting point for comparing chemical exposure assessment data, as the OSHA PELs generally do not reflect the current state of knowledge regarding chemical toxicology research and exposure assessment science. ACGIH is a trusted partner in the industrial hygiene community and its TLV development process is well understood by most IHs. ACGIH publishes new and revised limits annually, and the supporting documentation is invaluable in explaining how the limit was derived and what studies were considered in the limit's development. For example, ACGIH categorizes the data considered in TLV development and makes it clear how the limits are related to that data (e.g., Confirmed Human Carcinogen, Suspected Human Carcinogen, Confirmed Animal Carcinogen, Not Classifiable as Human Carcinogen, Not Suspected as a Human Carcinogen, Dermal Sensitization, Respiratory Sensitization, Skin / Danger of Absorption, etc.). These categorizations help the IH community understand the type of controls necessary to protect workers against the chemical hazard.

[24] Draft PEA, Appendix B, at B-7

[25] American Conference of Governmental Industrial Hygienists, see: https://www.acgih.org/ -- SIA would be happy to facilitate a discussion with industry industrial hygiene experts to support documentation on worker health and safety beyond the information currently provided in the PEA.

Section 3.7.1.4

In the last paragraph of this section, SIA suggests CPO include supplementary information reflecting that in modern fabs, process equipment is located in the clean room where a stringent clean regime is maintained as a requirement for production which also ensures no chemical releases. Examples of the high degree of engineering controls used to ensure employee exposure is minimized include exhaust, interlocks, and monitoring. In all semiconductor manufacturing, equipment systems operate with intrinsic controls that minimize or eliminate chemical liquid or vapor exposure potential during normal equipment operations. Hazardous gases and chemicals are transferred to process tools in transfer lines that are contained (and sometimes double contained) in addition to the leak detection methods already discussed by CPO. Chemicals are stored and delivered into the manufacturing area using secondary containment and methods to prevent personnel exposure. Safer designs and packaging of chemicals improves safety throughout the full chemical life cycle. All personnel with potential exposures utilize personal protective equipment (PPE) that meets or exceeds necessary performance and safety requirements.

Section 3.8.1.2

This section would benefit from discussion with SIA company chemical experts to ensure its accuracy. The first bullet, “The photolithography process uses the most chemicals during fabrication,” is incorrect. The second bullet is likely a misinterpretation. Dry etching gases mentioned in bullet 3 are not highly toxic and highly reactive, but dopants (bullet 4) can be. Silicon is not flammable. Table 3.8-1 should be updated to reflect chemicals more commonly found in modern semiconductor manufacturing.

Section 3.8.2.2

As appropriate, SIA recommends that CPO expand on its discussion of effects and duration in the last paragraph in this section to support its conclusion.

Section 3.10.1.2

CPO should mention the specific facility addressed in the example in Chandler, AZ – in this case, to refer to Intel’s facility in this jurisdiction.

Section 3.10.3.1

In its comment, that “semiconductor manufacturers also are pursuing practices and projects to make their operations more sustainable, including reducing energy and water use,” CPO should expand its citation to include U.S.-headquartered semiconductor manufacturing companies, in addition to those already cited.[26]

[26] For example, other companies have adopted similar practices, including Intel: https://csrreportbuilder.intel.com/pdfbuilder/pdfs/CSR-2022-23-Full-Report.pdf ; Texas Instruments: https://www.ti.com/lit/ml/szzo086b/szzo086b.pdf?ts=1705963681595 ; Micron: https://media-www.micron.com/-/media/client/global/documents/general/about/2023/2023_micron_sustainability_report.pdf?la=en&rev=387083ff29e9481bba445a1d6972a41f and others.

Section 3.11.1.2

SIA suggests CPO add that the site-specific issues will be addressed on a case-by-case basis, but the programmatic effects can be assessed.

CPO may also consider directly comparing locations of facilities potentially falling under the NOFO to those locations with environmental justice communities. It would be beneficial for CPO to conduct additional analysis that demonstrates the EJ impact is not necessarily "unknown."

Section 3.12.1

SIA suggest CPO add that the site-specific issues will be addressed on a case-by-case basis, but the programmatic effects can be assessed.

Section 4.0

As previously discussed, and per the amended CEQ regulation, SIA recommends that CPO include discussions of cumulative effects in its resource-specific discussions on direct and indirect effects, consistent with the definition of "effects" at 40 CFR 1508.1(g).

Section 4.3

In the first paragraph, SIA suggests that CPO include reference and citation to the Fifth National Climate Assessment.[27]

Section 4.4

SIA recommends CPO clarify the description of the WSC 2030 Voluntary Agreement on PFC Emission Reductions to reflect the following:

> To build on this success, the global industry is implementing another reduction goal to **achieve a PFC emissions reduction rate of 85 percent** ~~reduce PFC emission rates by 85 percent~~ by 2030 (with a baseline of 81 percent in 2021).

Appendix A

The appendix on best management practices appropriately addresses the environmental due diligence companies may undertake and is well-referenced.

SIA notes that some of the best management practices described are either impossible or extremely difficult to implement as part of a facility modernization or expansion, depending on the project. A modernization or expansion more limited in nature may be

[27] See: https://nca2023.globalchange.gov/. "The Fifth National Climate Assessment is the US Government's preeminent report on climate change impacts, risks, and responses. It is a congressionally mandated interagency effort that provides the scientific foundation to support informed decision-making across the United States."

focused only on replacing or adding new tools or production lines. In some cases, there may be inadequate space or unreasonable costs to accommodate certain pollution control technologies or renewable energy systems. It is highly unlikely that such a project would include extensive unrelated projects and retrofits, such as the installation of on-site renewable energy where it doesn't already exist.

CPO should clarify that the best management practices and best available technologies that could be part of the project are limited to only those specifically related to the project. At the mutual agreement of the company and CPO, unrelated best management practices or best available technologies could still be implemented in order to avoid or mitigate environmental effects.

Appendix B

SIA appreciates CPO's acknowledgement that there is ongoing research and investigation regarding the use of PFAS in the semiconductor industry, and that topics relating the PFAS are best reserved for future study. The broad definition of PFAS currently used in certain states brings many fluorocarbon substances into scope and identifying and quantifying all uses takes time. Table 2 of Appendix B provides example PFAS use applications; however, the table is missing reference to fluoropolymer articles in semiconductor manufacturing and related equipment, as well as assembly, test, and packaging and substrate use applications.

SIA observes that the Appendix B narrative descriptions of semiconductor manufacturing processes and the role of PFAS is overly general and imprecise, compared to the descriptions provided in Section 2 and 3 of the PEA. More appropriate and accurate descriptions are provided in the Semiconductor PFAS Consortium White Papers, available at www.semiconductors.org/PFAS, as opposed to the paper developed by RINA (Jones, 2022), which in some places may be out of date following new research produced by the Consortium. SIA would be happy to facilitate engagement between CPO and the Semiconductor PFAS Consortium to clarify some of the items discussed in Appendix B.

SIA also suggests resolving the below technical items:

- CPO states, "There are more than 3,000 PFAS manufactured and used in the United States (U.S.)." A 2023 Consumer Products Safety Commission (CPSC) report compiled available sources from the U.S. EPA to form a list of 16,229 distinct PFAS currently identified.[28]

- In the section "PFAS in semiconductor fabrication facilities," CPO identifies six process steps, which do not correspond to the processes specified in 2.2.2. It must be noted that PFAS are critical to the proper functioning of photolithography formulations used to transfer the pattern onto the wafer; they are used in certain

[28] CPSC, "Characterizing PFAS Chemistries, Sources, Uses, and Regulatory Trends in U.S. and International Markets Final White Paper." *Available at: https://www.cpsc.gov/s3fs-public/CPSC-PFAS-WhitePaper.pdf*

deposition precursors and formulations to meet critical functionality; fluorocarbon gases are essential for plasma etch where anisotropic etching is needed and are used as a safe source of fluorine in older CVD chamber clean processes; PFAS are used in certain wet chemical processes including some aqueous and organic etch, clean and pattern collapse formulations, certain CMP slurries, and in some plating formulations. As CPO noted, PFAS are also utilized in assembly, test, and packaging.

- CPO states, "...the most abundant use occurs during photolithography..." It is not clear what the meaning of "abundant" is; however, PFAS articles, such as semiconductor manufacturing equipment, have the greatest number of distinct use applications, and their combined mass is much greater than that of PFAS used in photolithography. Under the broad PFAS definitions adopted in some states, fluorocarbon- and certain hydrofluorocarbon- containing plasma etch and deposition chamber clean gases are considered PFAS. These gases are used in greater amounts than PFAS used in photolithography.

- CPO identifies TARCs as "the single largest source of PFAS in semiconductor manufacturing." It would be more accurate to say TARCs are the largest single source of PFAS in photolithography.

- CPO states, "PAGs utilize fluorine to enable greater solubility and development during the etching process." This should be corrected to state that the PAGs acid anions are fluorinated so that they can generate very strong acids during imaging, that can migrate at a controlled rate through the photoresist layer to react with acid labile groups in the photoresist polymer and render them soluble in an aqueous base during the photolithography development step.

- The paragraph beginning "Beyond photolithography …" does not sufficiently capture the range of uses of PFAS in semiconductor fabrication. (For example, depending on the definition, PFC and certain HFC gases may be considered PFAS. This paragraph could also include wet chemical applications, F-HTFs and fluorocarbon gases used in process equipment chillers, PFAS vacuum pump fluids, greases and other PFAS lubricants, and fluoropolymers.) CPO could consider incorporation by reference of the Semiconductor PFAS Consortium technical white papers.[29] SIA appreciates CPO's effort to capture the role of PFAS in the semiconductor manufacturing process. This is an important topic to the industry, government agencies, and civil society, and therefore it is important that the PEA documentation from CPO is fully comprehensive and accurate. SIA is happy to facilitate discussion with company technical experts on this topic.

[29] https://www.semiconductors.org/download-all-pfas-technical-papers/

- CPO states, “Wastewater discharge from semiconductor facilities presents the greatest risk for PFAS contamination of the environment.” Depending on the definition of PFAS, this may not necessarily be the case. For example, gases are generally used and released in much greater quantity, and fluorinated heat transfer fluid releases to the air can also be substantial. Fluoropolymer articles, which are outside the scope of many definitions of PFAS, could also be considered here. SIA notes that the presence or use of PFAS does not connote exposure and/or risk. Accordingly, SIA does not believe CPO is in a position to determine the greatest possible source of contamination.

- CPO states, "While most photolithography waste is handled as a solvent and incinerated, only 40 percent of TARC waste is treated." TARC is an aqueous formulation that is incompatible with solvent waste. In most semiconductor facilities, 100% of TARC that is used goes to the industrial wastewater drain, unless segregated in a separate drain and collection system for disposal. Implementing such action could require hardware and software modifications to the track tool.

- CPO cites, "The current detection methods are limited to a few PFAS compounds (Jones, 2022)." Meanwhile, the current EPA method for measuring PFAS in water is limited to about 40 PFAS compounds.

- CPO cites, “Due to the chemical stability of PFAS there are currently few adequate substitutes for PFAS in semiconductor fabrication (SEMI, No date).” This statement falls far short of the list of compelling reasons listed in the Consortium papers and identified in Table 2. This statement does not reflect the full complexity of semiconductor manufacturing processes and the many different and unique application-specific roles that PFAS plays.

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SIA and its member companies appreciate the opportunity to provide comments to CPO on the draft PEA. We request an opportunity to meet and further discuss these comments, and we look forward to continuing to work with the CPO.