Encouraging Innovation: The Policies and Partnerships Needed to Support Semiconductor Startups

- Semiconductor startup and investment landscape in 2024 -

Daniel Armbrust

SIA Webinar
– April 4, 2024 –

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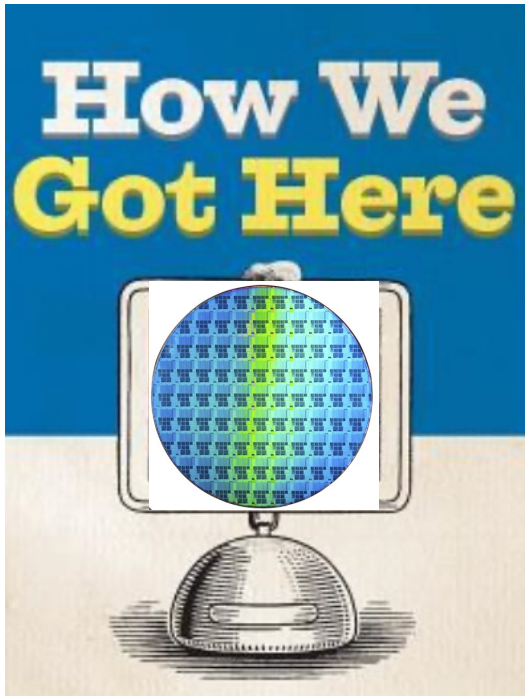
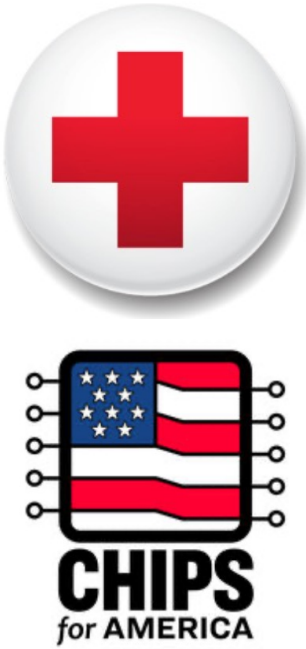
Remarks today are made in his personal capacity, and his remarks should not be attributed to the Department of Commerce, the Industrial Advisory Committee of the CHIPS Act, or the US Government.

Semiconductor startups and investments





Bottom line up front (BLUF)

Semiconductors are resurgent

Company valuations and profitability
- 8 of the top 20 market caps in tech
- 3rd most profitable industry

AI is profoundly hardware limited -- it's the next gold rush

Essential assets in a geopolitical sea change away from globalism

Semiconductor startups face daunting challenges

Escalating cost of innovation: prototyping access and costs

Sustained decline of venture capital for semiconductors

Achieving product-market fit remains challenging

Diminished customer appetite to award design wins to startups

A surge of investments are underway

CHIPS Act(s) in various countries and regions

VCs are wading back in as there are green shoots in Deep Tech and specialty funds – A contrarian opportunity

Reasonable M&A and IPO opportunities for startups

Chiplets and advanced packaging can advantage startups

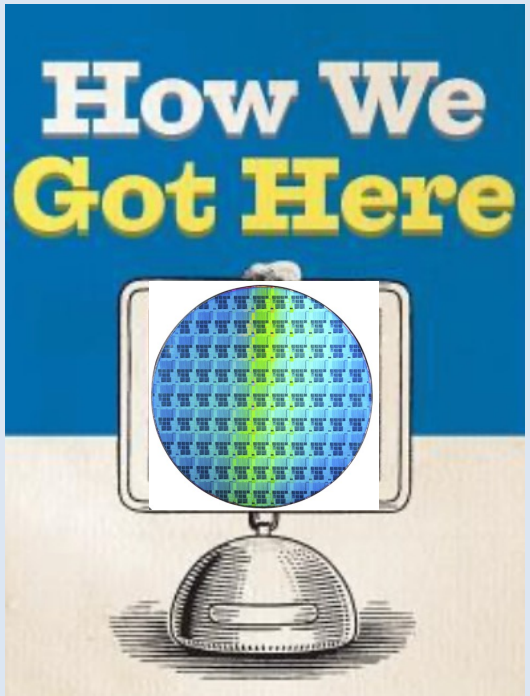
But more research will not lead to commercialization unless we continue to build the startup playbook

Aggressively implement CHIPS Act investments for prototyping and startup funds with a sense of urgency

Supplement with existing government programs and funding streams

Strengthen startup ecosystem for translation to industry

Semiconductor startups and investments



BEHIND THE STARTUP

CHIPS for AMERICA

How did we get here?

1950's – Invention of the transistor by Bell Labs and dissemination through licensing core technology

1960's – Integrated circuits driven by gov't needs, invention of venture capital and startups in Silicon Valley

1970's – Invention of microprocessors and DRAM memory

1980's – Japanese DRAM threat leads to formation of SIA / SRC / SEMATECH to restore US competitiveness

1990's – Foundry business model lead by TSMC in Taiwan

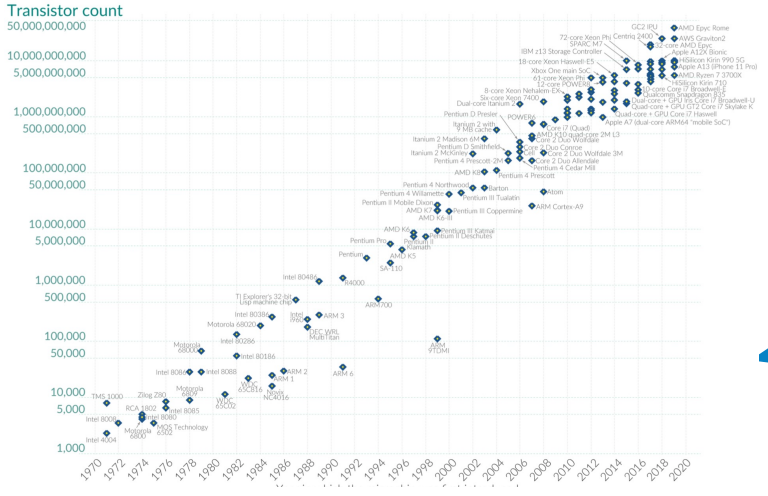
2000's – Beginning of industry consolidation; decline in venture capital investment

2010's – Moore's Law slowdown, the rise of AI, and emergence of a Chinese threat, pricing power

2020's – Pandemic chips shortages, CHIPS Act(s), China's access restrictions, Generative AI

Moore's Law economic-based prediction

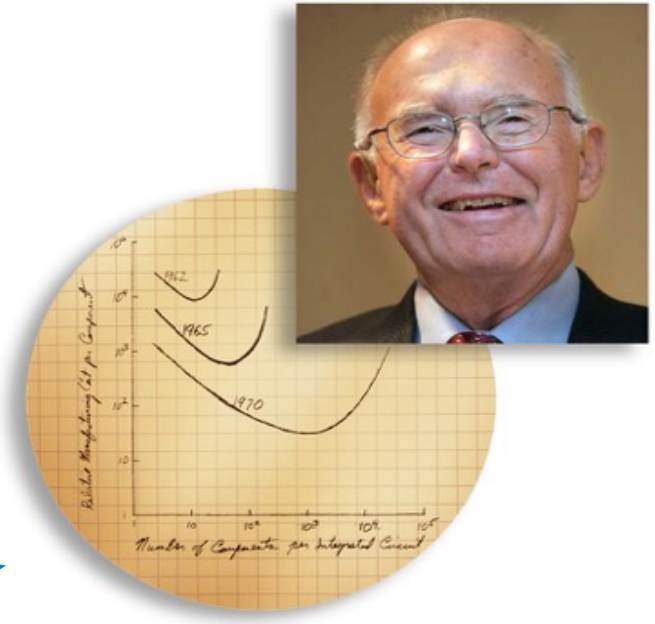
Transistors on a Chip



Source: Wikipedia

More R&D (innovation)

Lower cost/function

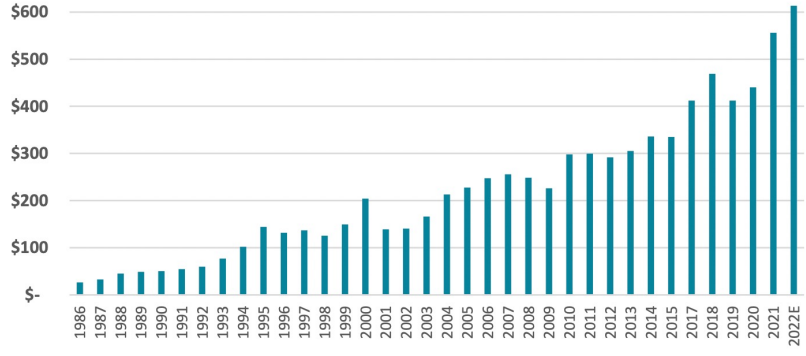


$'s

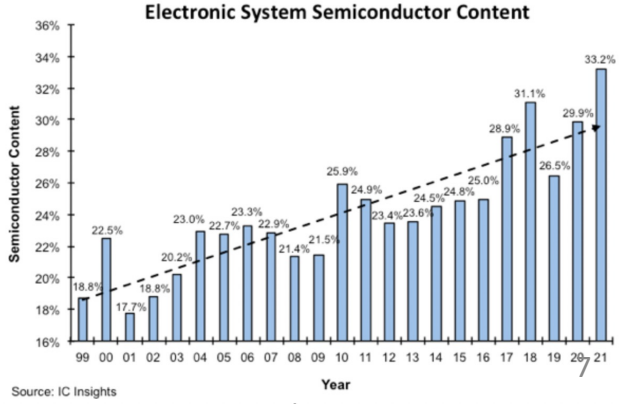
Increasing semiconductor revenue

Expanding applications (more silicon)

Semiconductor Revenue

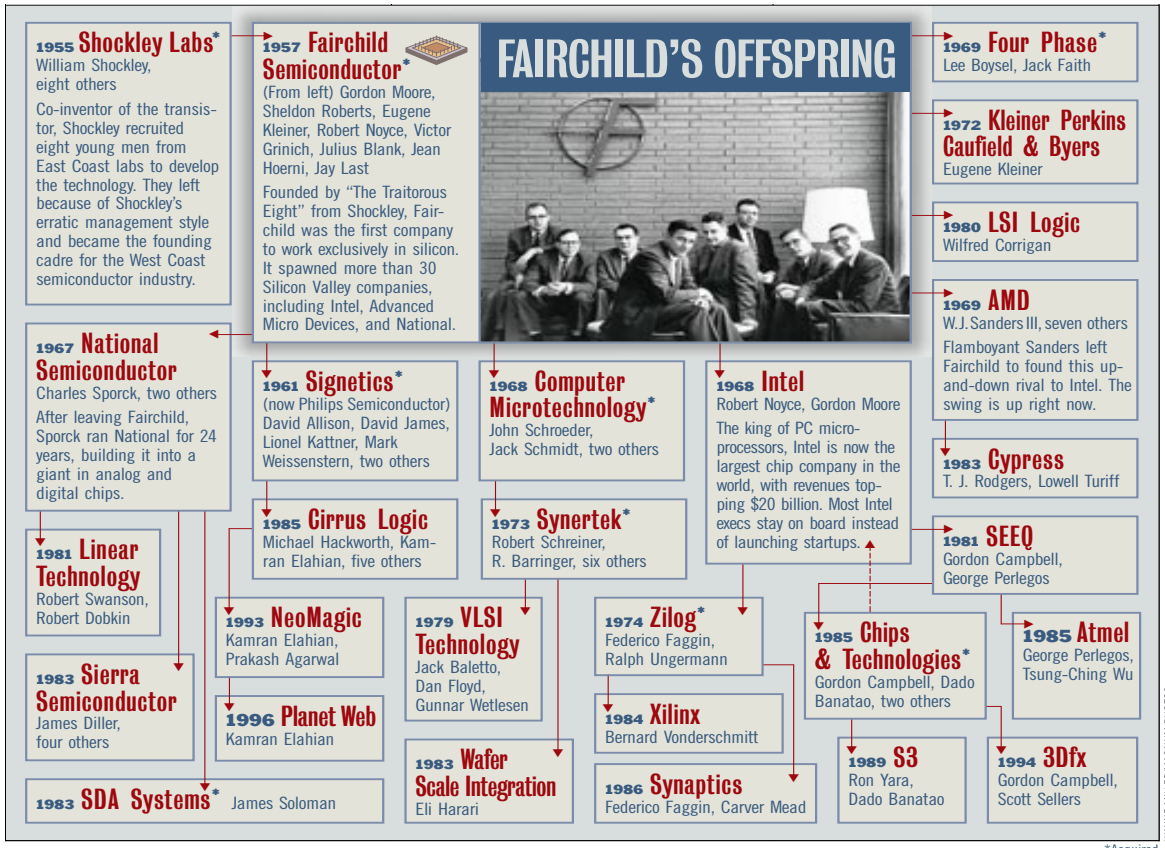


Source: WSTS



Source: IC Insights

From U.S. startups and venture capital to geographic dispersion and consolidation



Country Market share (IC Insights)

US 54%

EU 6%

Taiwan 22%

Japan 6%

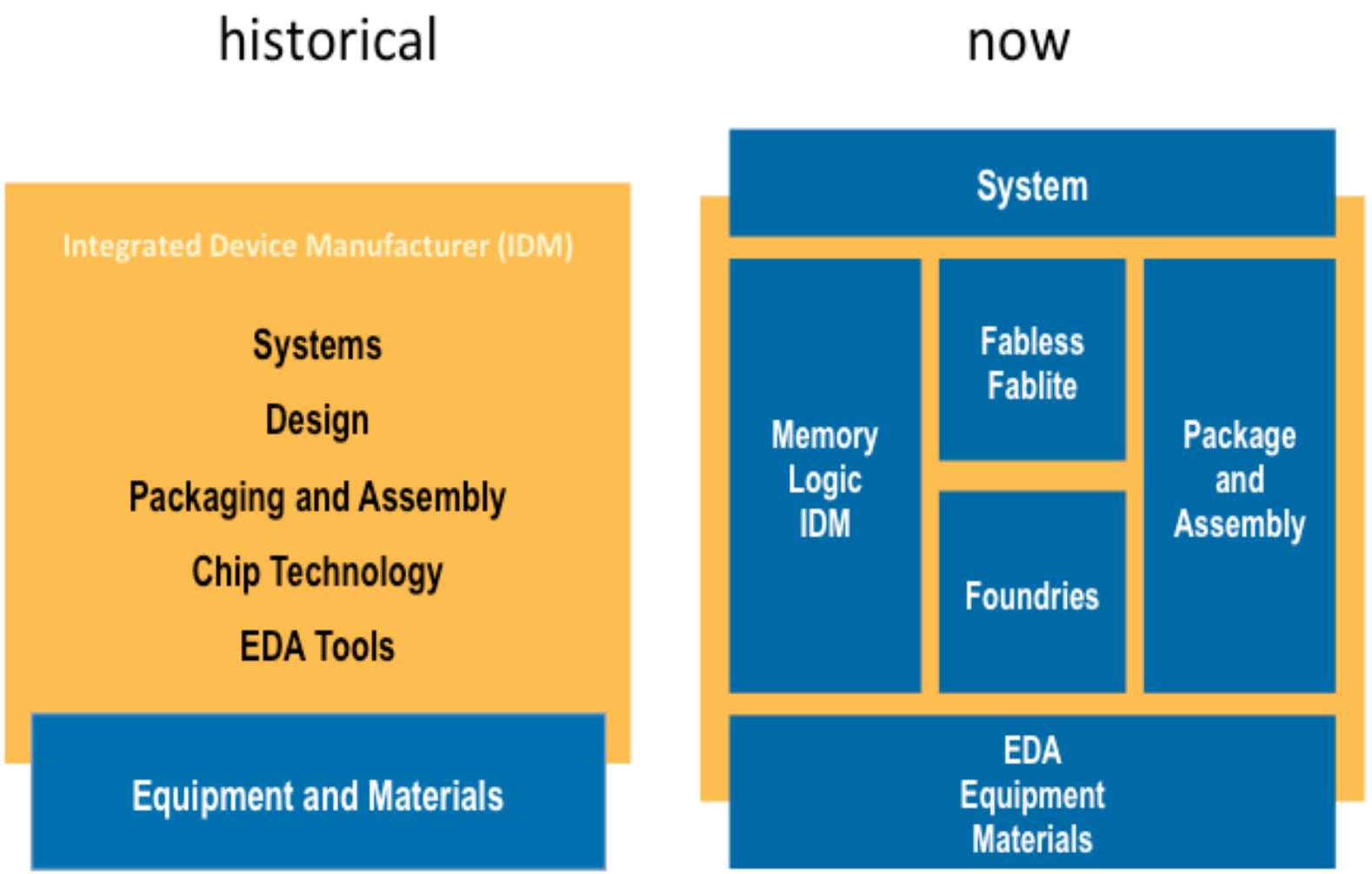
Korea 9%

China 5%

1960's

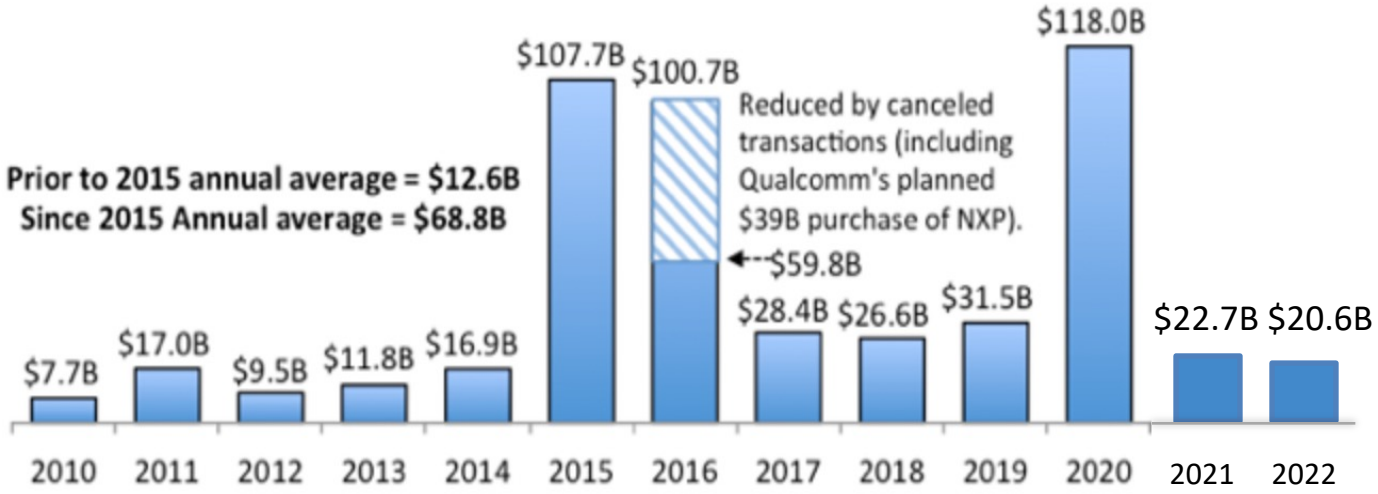
2020's

Evolution of the supply chain and it’s fragmentation



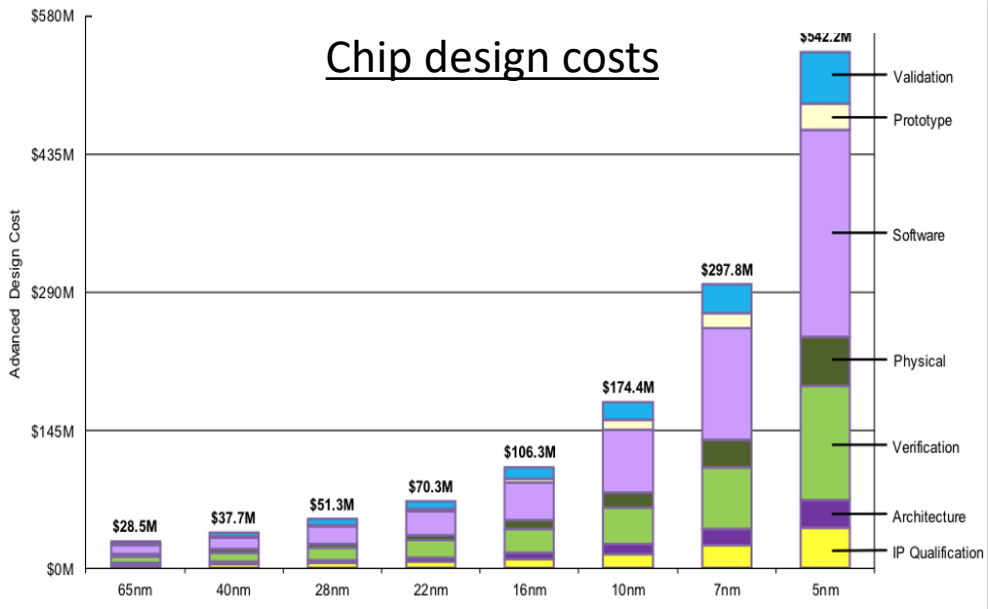
Consolidation and concentration in each segment

Semiconductor M&A Valuation



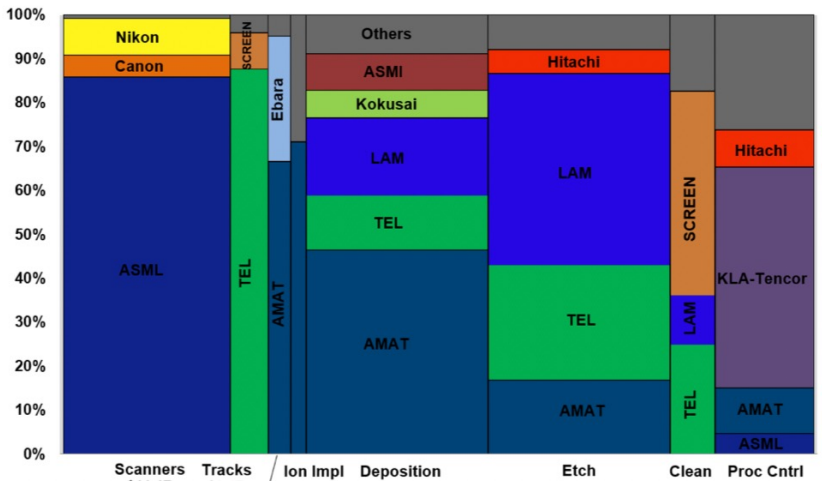
Source: IC Insights

Chip design costs



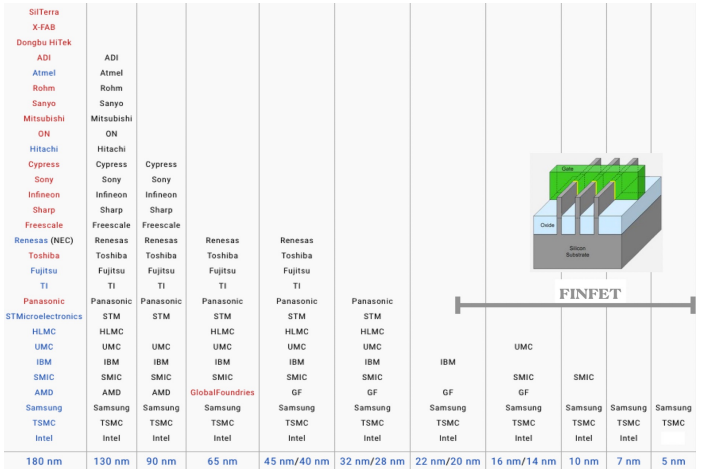
Source: M. Lapadeus, Semi Eng.

Equipment Market Share



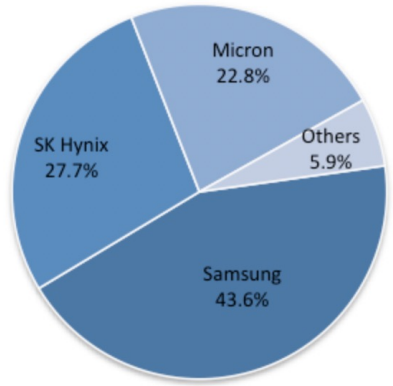
Source: VLSI Research, 2020

Logic/Foundry platforms



Source: Wikipedia

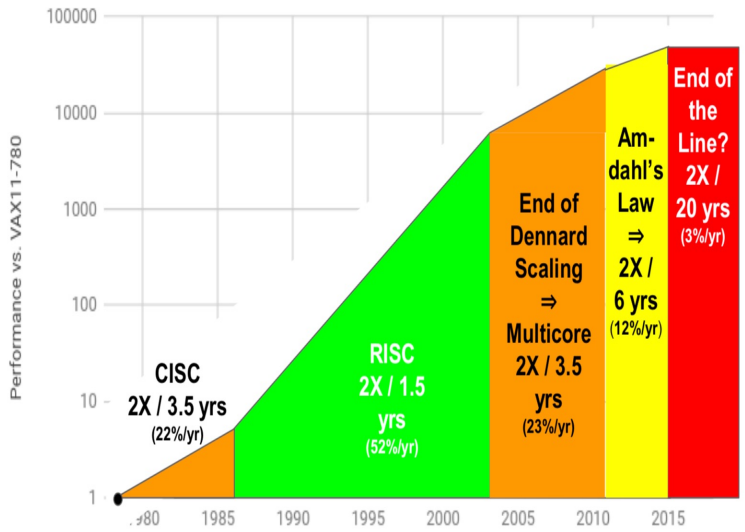
DRAM Market Share



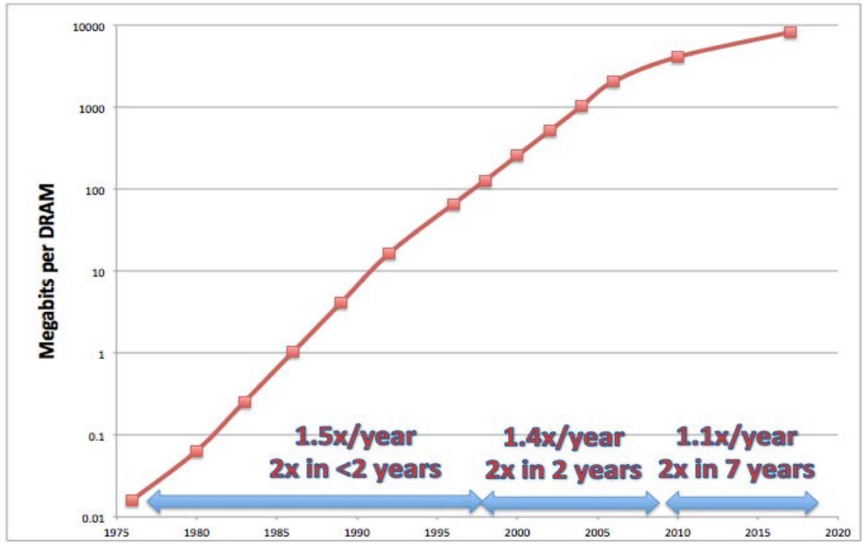
Source: IC Insights

Evidence of Moore's Law slowdown – scaling is in trouble

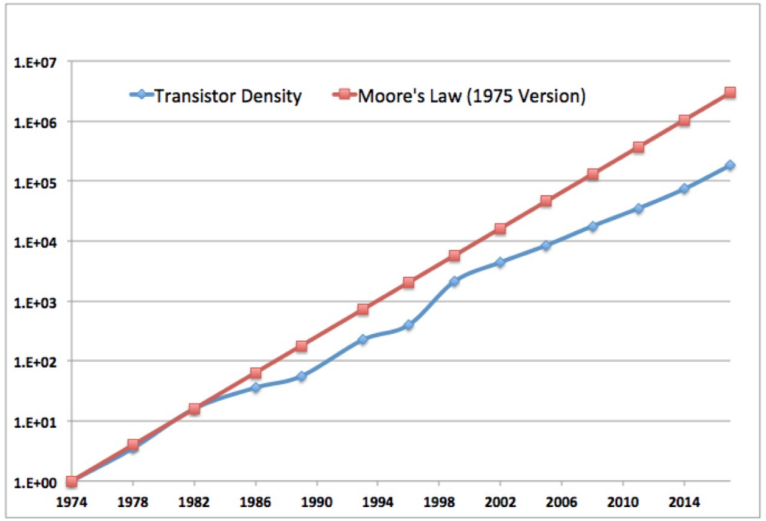
CPU single core performance



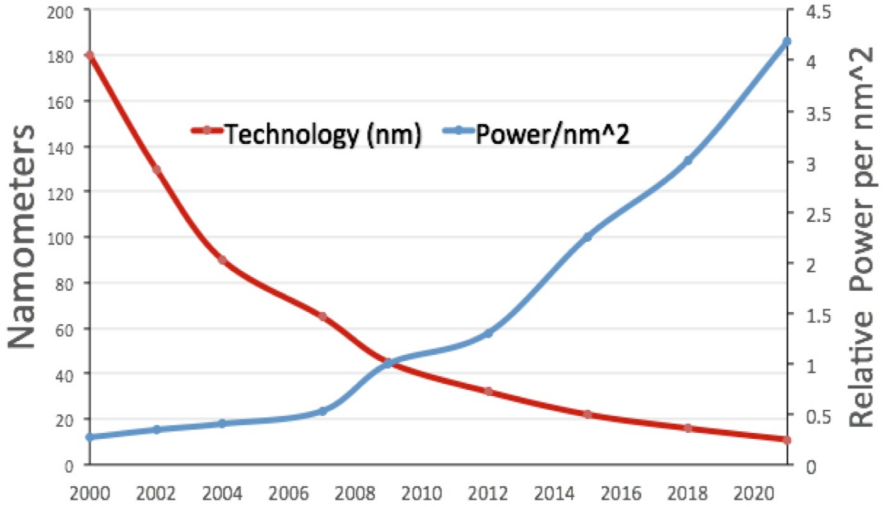
DRAM density roll off



Intel CPU density roll off



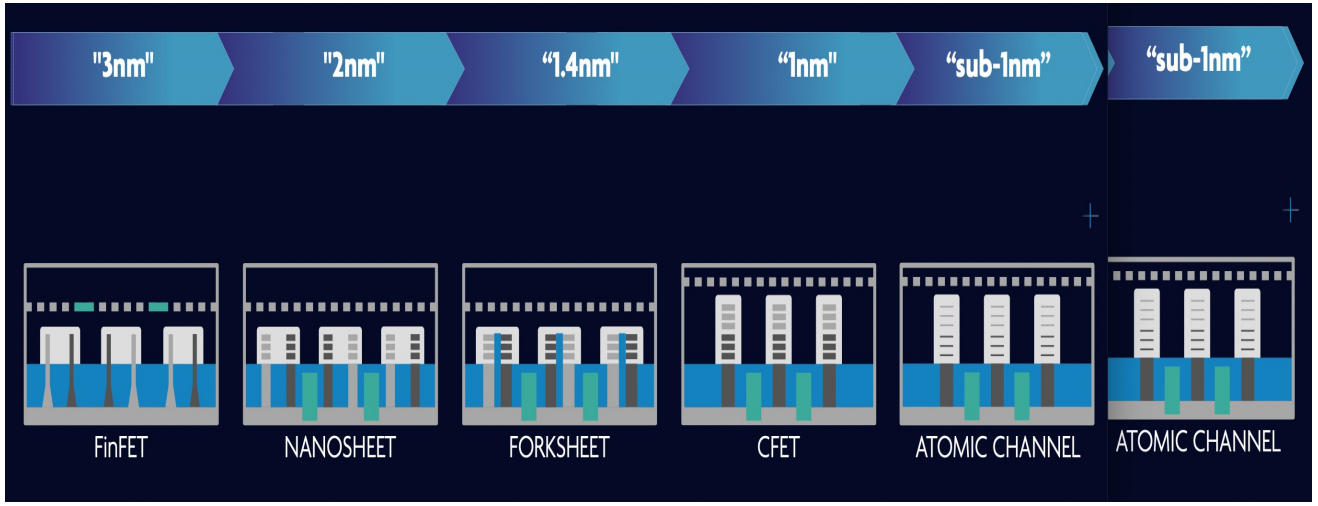
Transistor power takes off



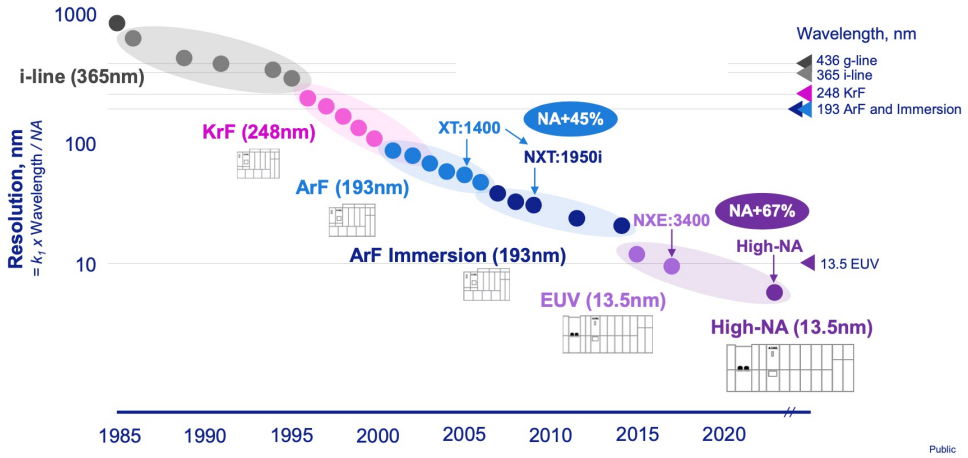
Source: Hennessy/Patterson Turing Award presentation

Some consolation until the next new thing: solid roadmap for next decade

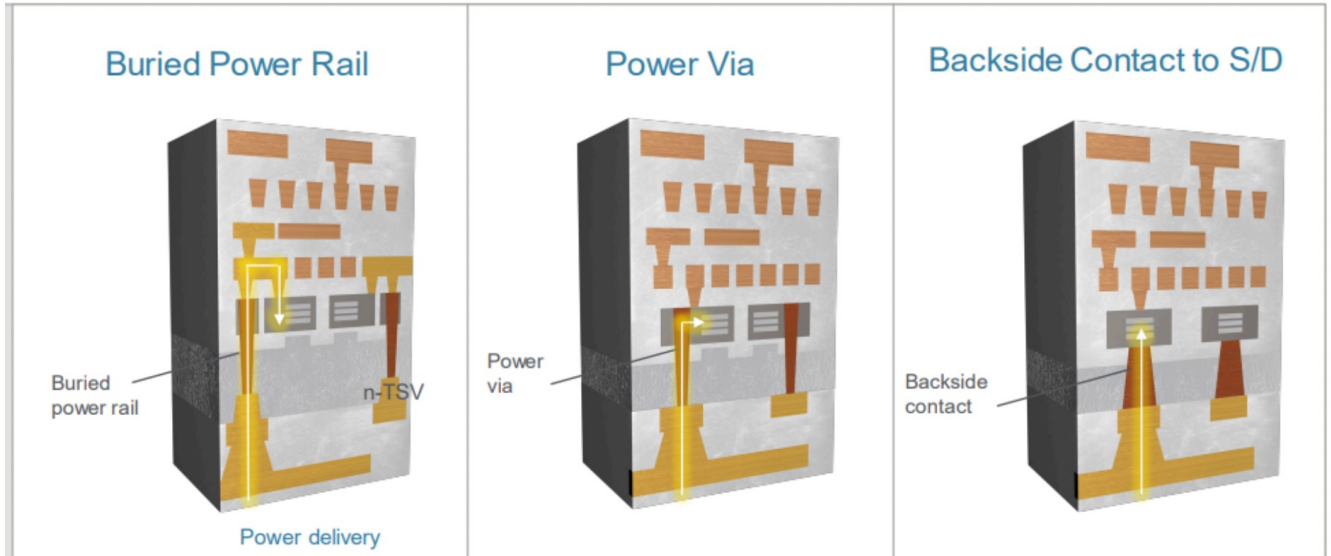
CMOS Roadmap to <1.0 nm



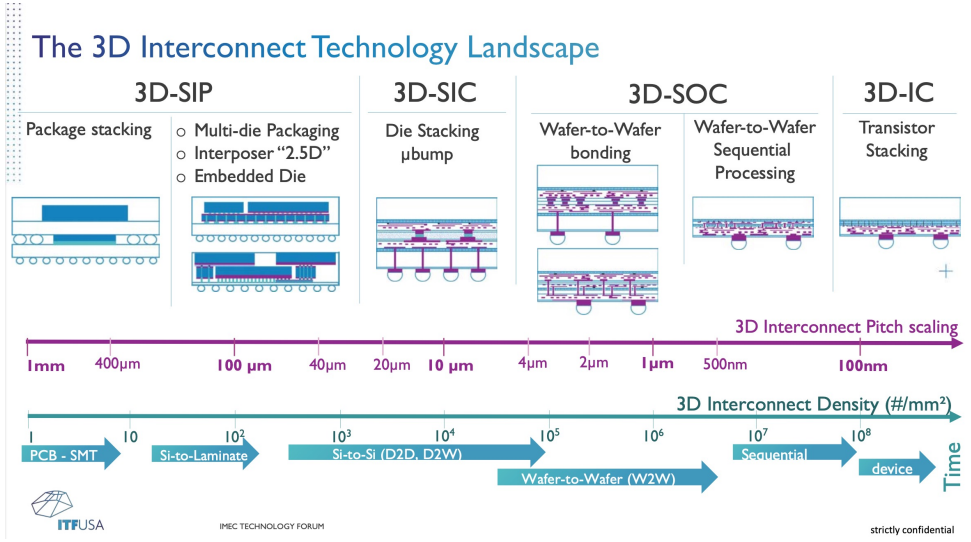
EUV Lithography



Backside Power Distribution

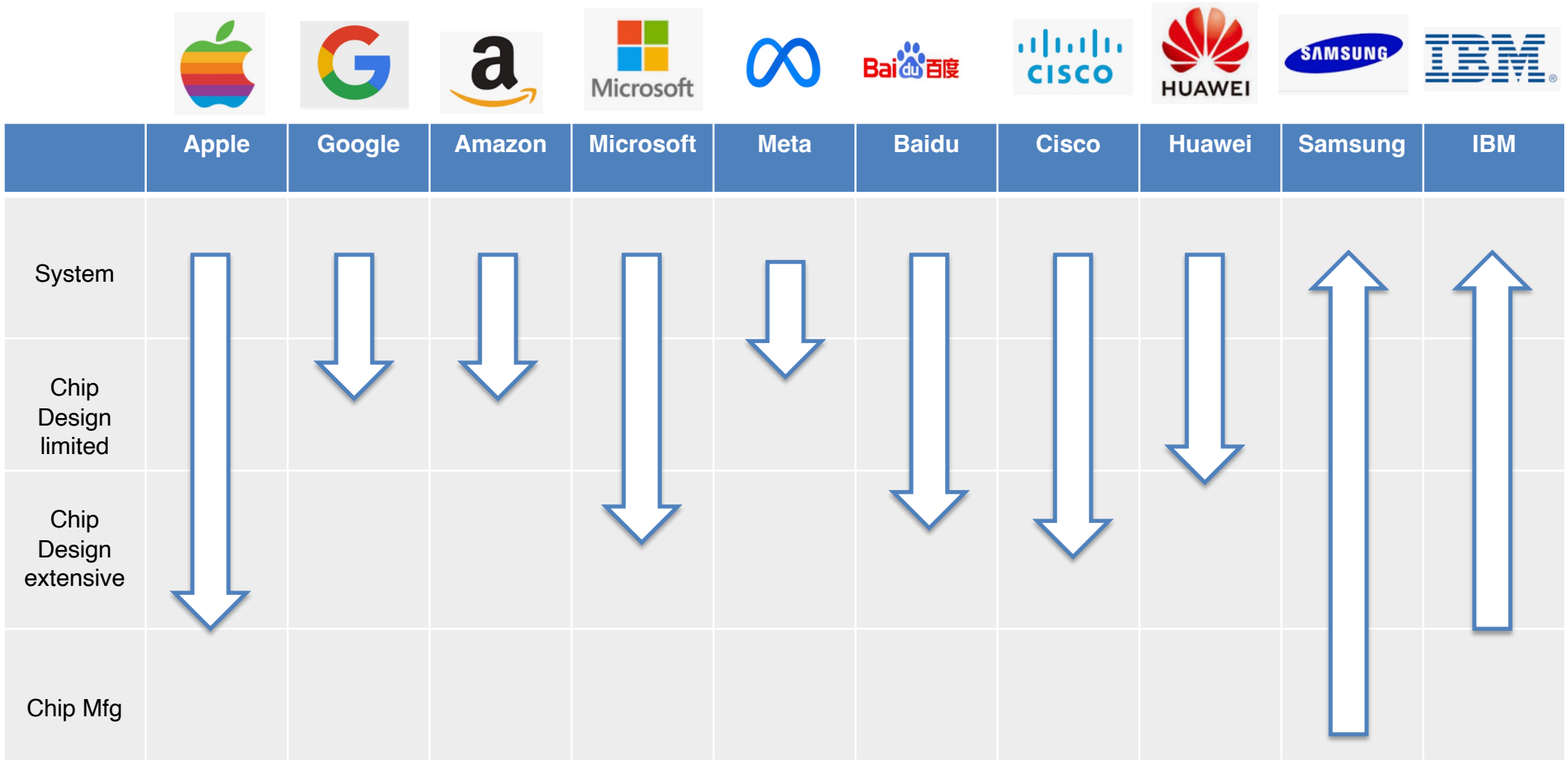


Advanced packaging



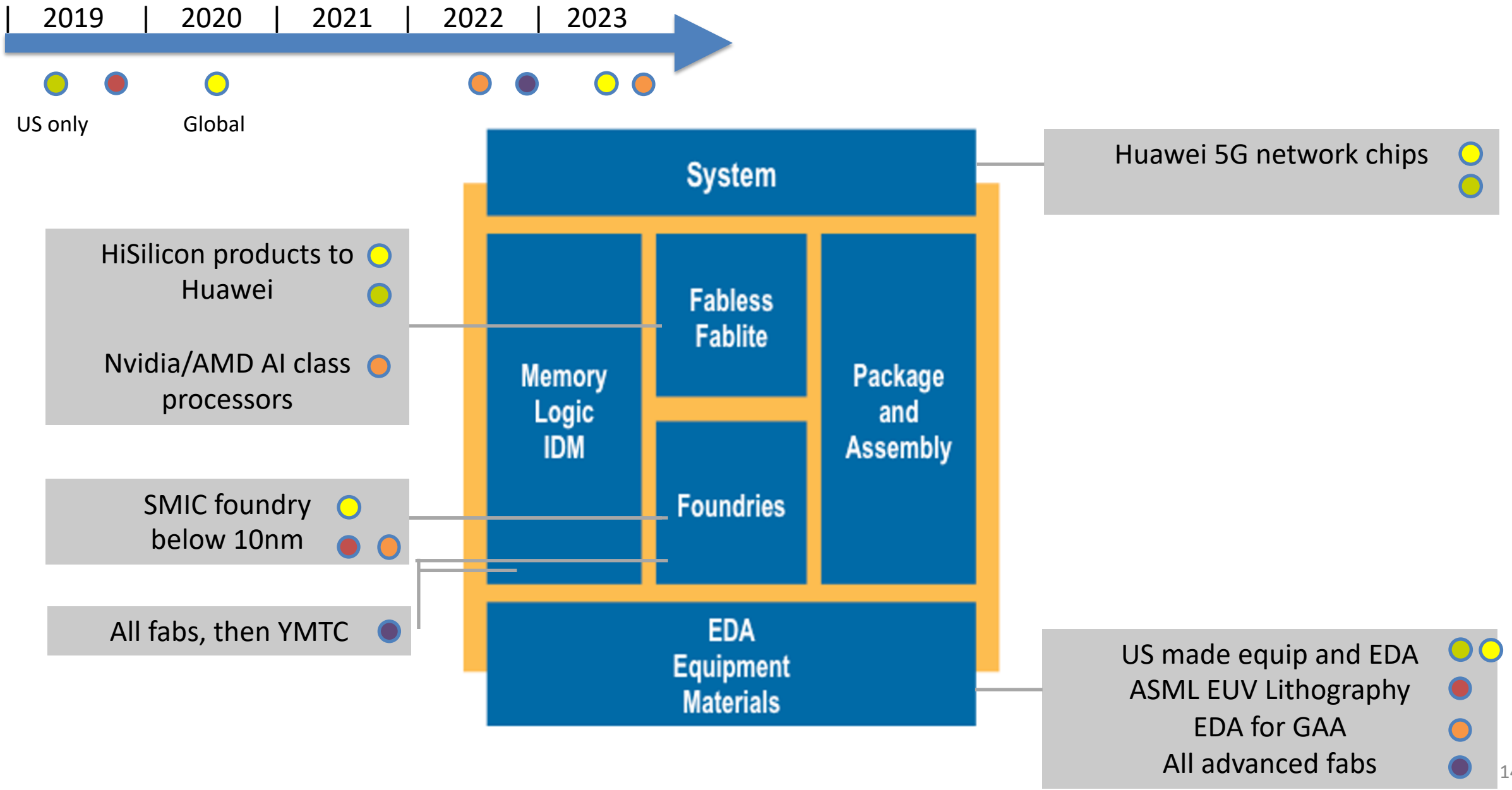
Source: IMEC, ASML, IMEC, Applied Materials (clockwise)

System companies becoming silicon houses

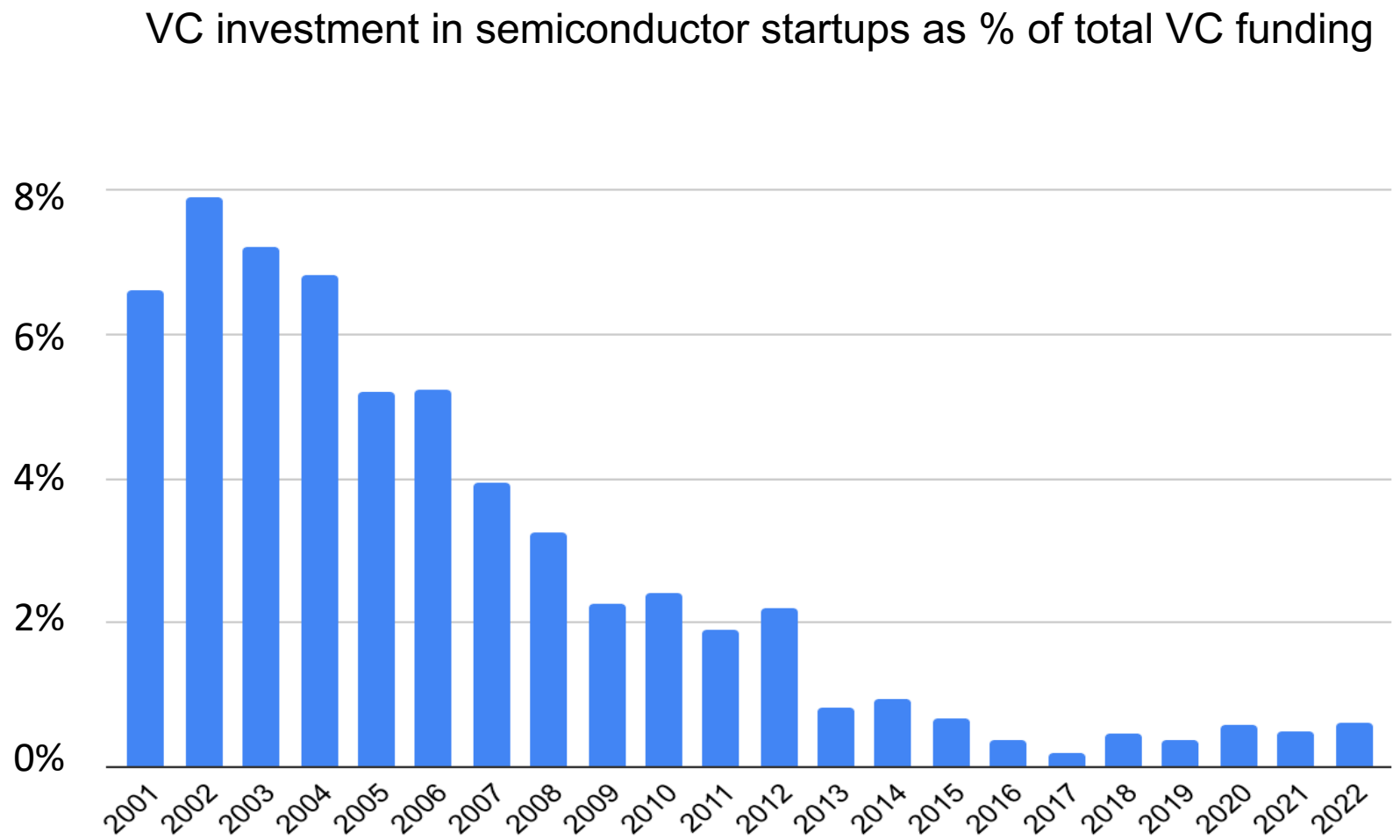


Source: VLSI Research (modified)

China export controls and trade restrictions are stressing globalism

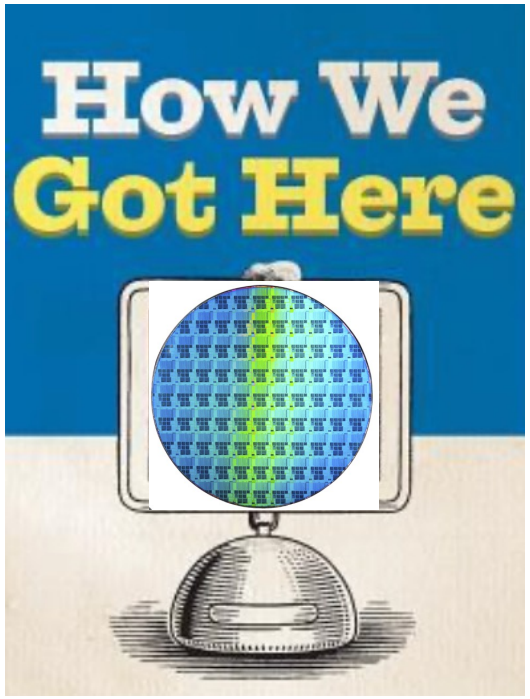


Venture Capital has moved past semiconductors to software and services



Source: Pear Ventures & Crunchbase

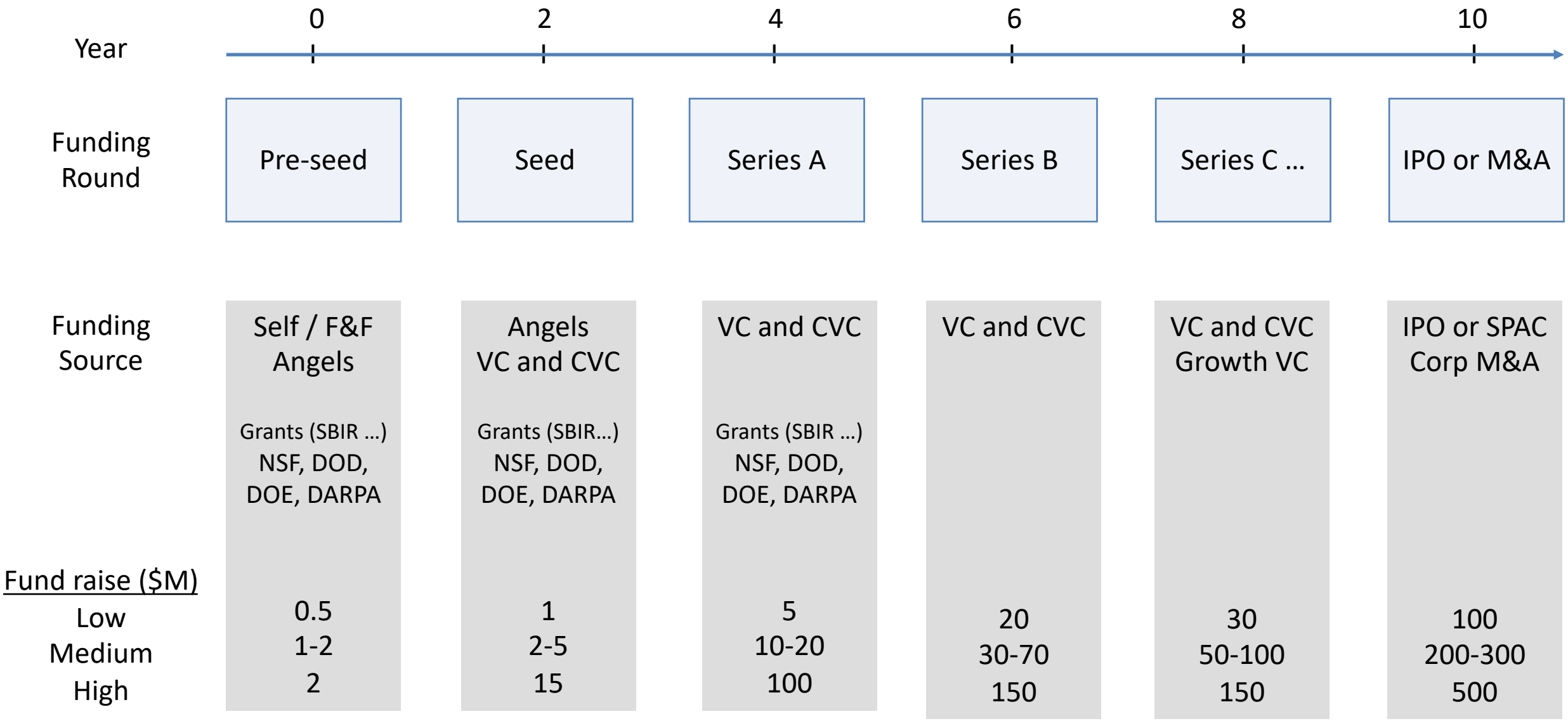
Semiconductor startups and investments



BEHIND THE STARTUP

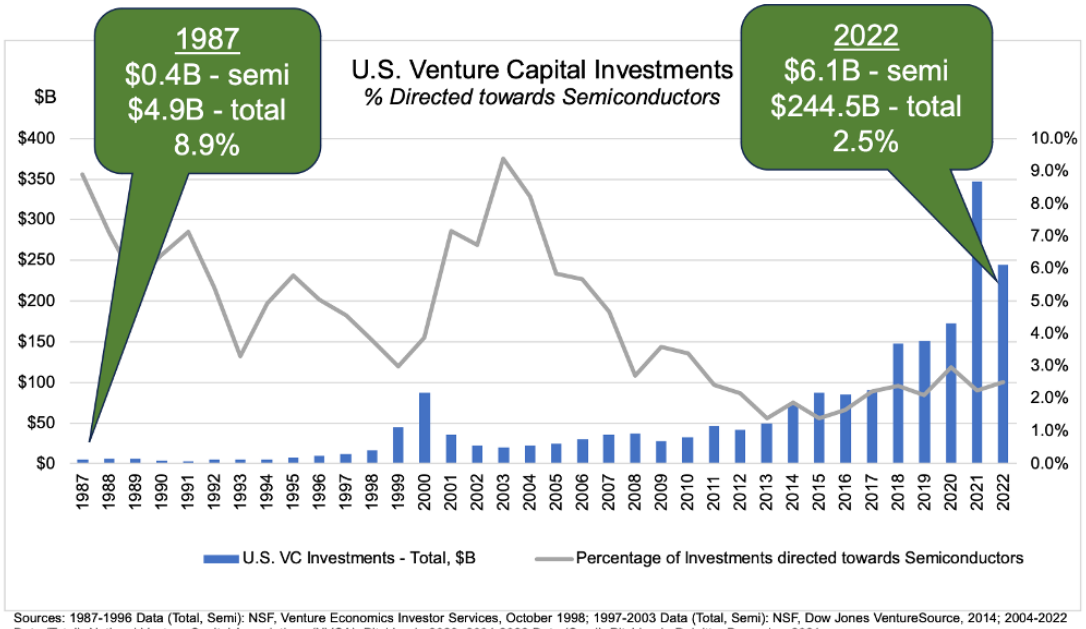
CHIPS for AMERICA

Typical semiconductor startup timeline



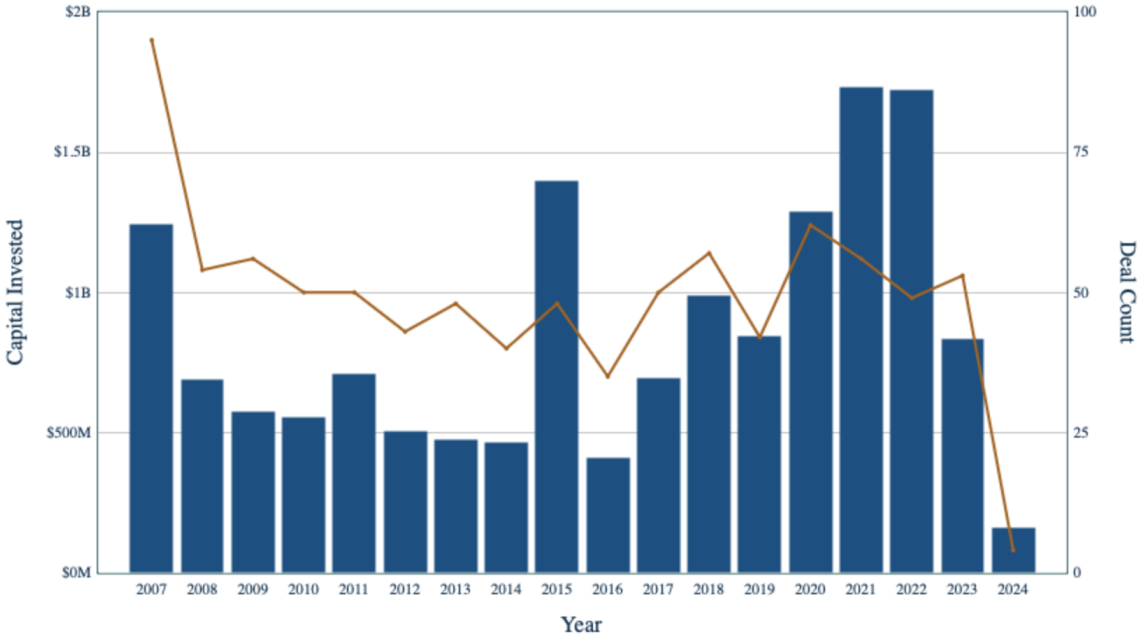
Dramatic ramp of venture investment in the last decade – semis not benefiting

US VC investments (25 years)



Sources: 1987-1996 Data (Total, Semi): NSF, Venture Economics Investor Services, October 1998; 1997-2003 Data (Total, Semi): NSF, Dow Jones VentureSource, 2014; 2004-2022 Data (Total): National Venture Capital Associations (NVCA); Pitchbook, 2023; 2004-2022 Data (Semi): Pitchbook, Deloitte, December 2021

US VC investments in semiconductors (15 years)



Pitchbook

Venture Capital and Corporate VC: who are the major players in semiconductors?

VC by Deal Count

Celesta	26
Walden International	24
A&E Investments	23
Eclipse Ventures	15
Foothill Ventures	15
Sutter Hill Ventures	15
Alumni Ventures	13
GSR Ventures	12
InQTel	12
Cambium	10
DCVC	10
Foundation Capital	10
Kleiner Perkins	10
Lux Capital	10
Bessemer Ventures	9

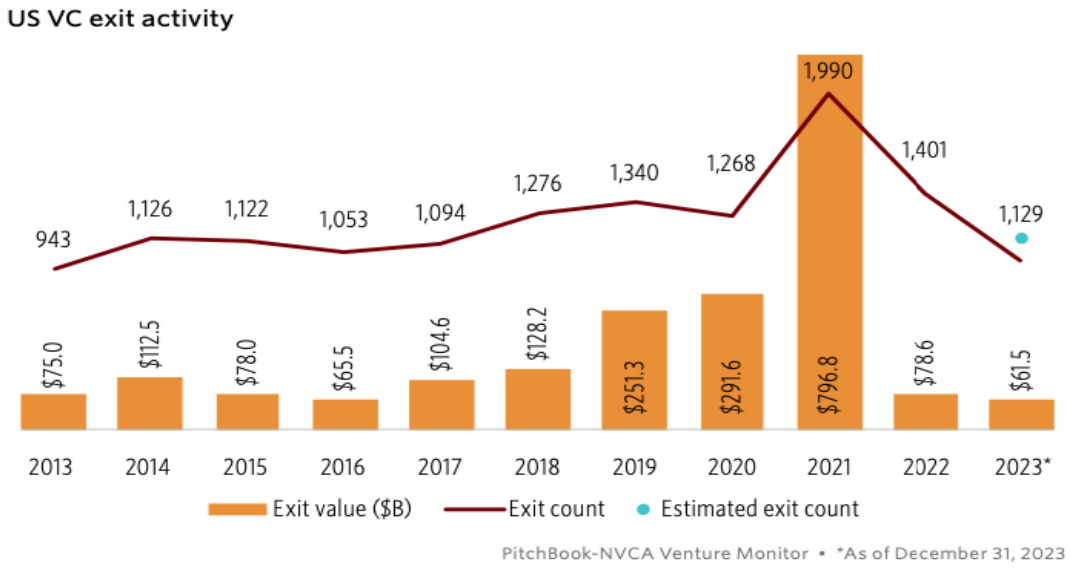
CVC by Deal Count

Intel Capital	74
Applied Ventures	16
Samsung Catalyst Fund	16
TEL Venture Capital	11
Cisco Investments	10
Lockheed Martin Ventures	10
AMD Ventures	9
Dell Tech Capital	9
Western Digital Capital	7
M12	6
Xilinx Ventures	6
TDK Ventures	5
3M Ventures	4
Airbus Ventures	4
Eni Next	4

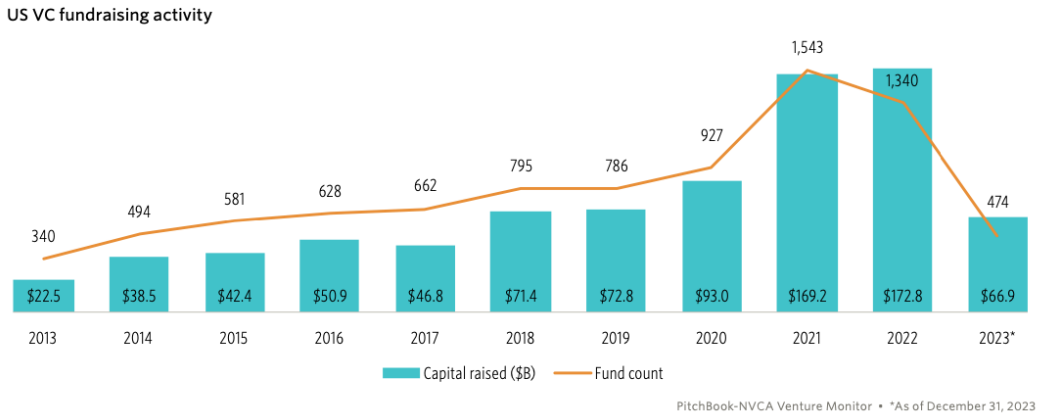
Pitchbook, 2014-2024

Venture Capital exits and funds raised – rapid reversal of positive trends

VC exits (IPO, M&A)

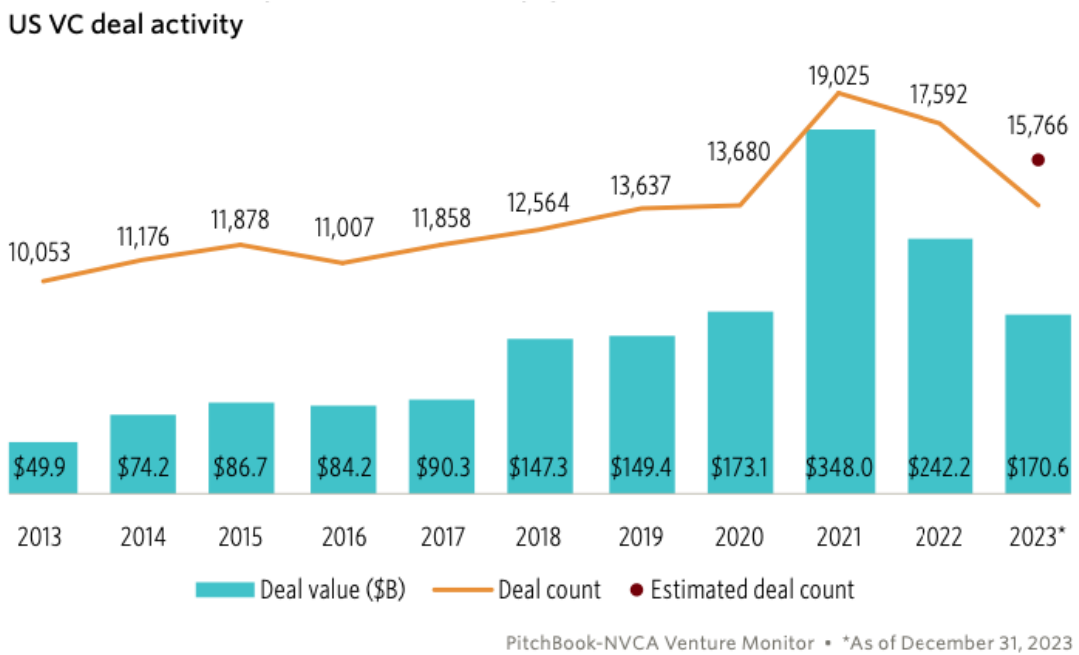


VC capital raised



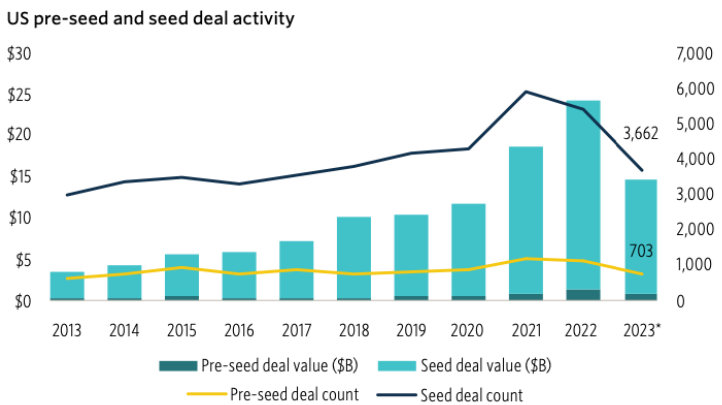
Downturn in Venture Capital startup funding from 2021 peak

US VC investments – All stages



PitchBook-NVCA Venture Monitor • *As of December 31, 2023

Pre-seed and Seed



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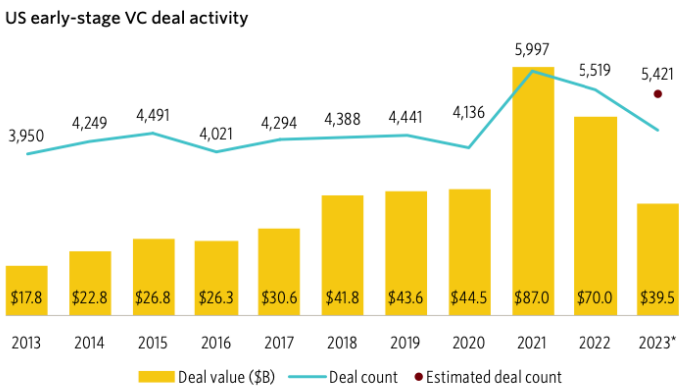
Early Stage (Series A/B)



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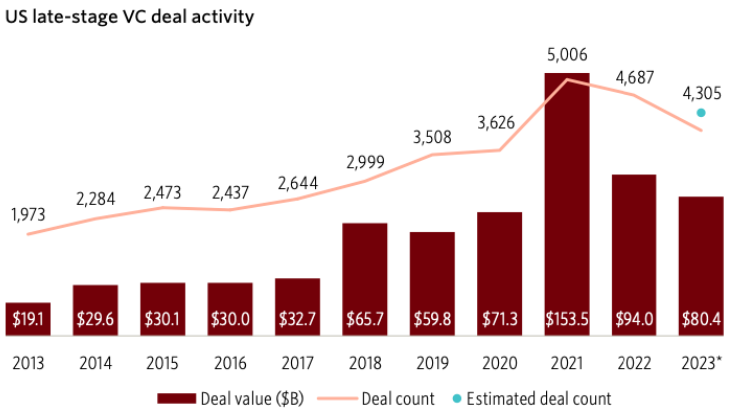
Late Stage (Series C/D)



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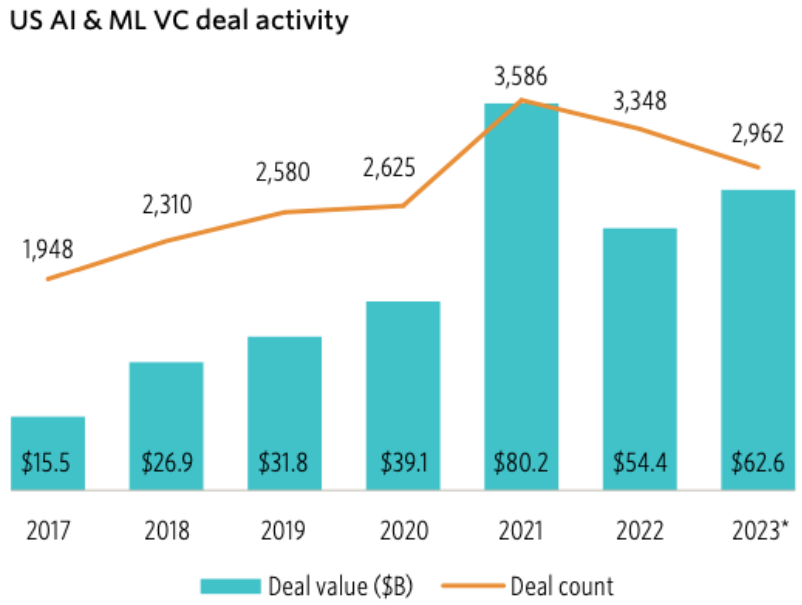
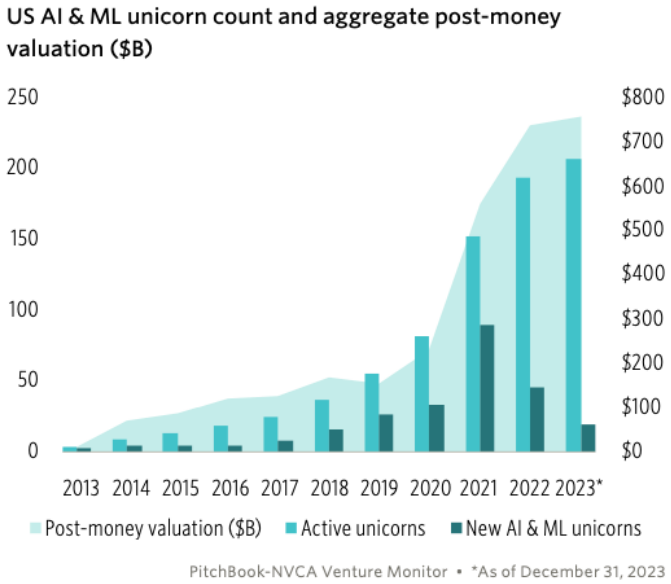
Venture Capital investments in AI/ML have escalated

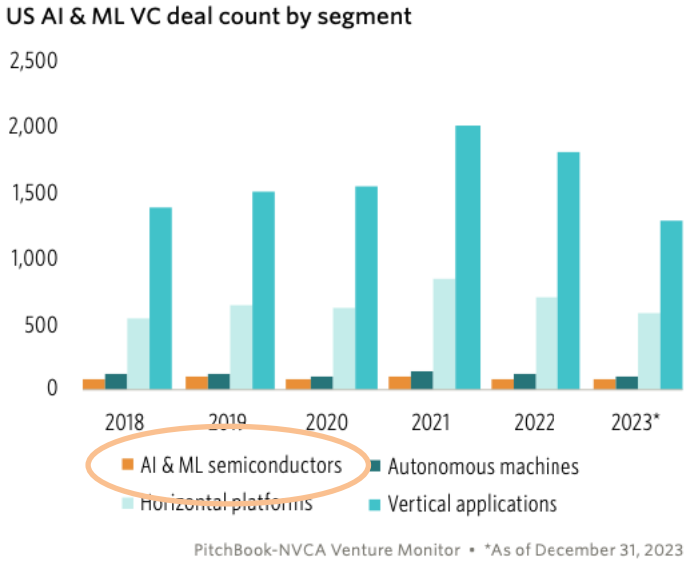
VC funding



AI startup unicorn formation

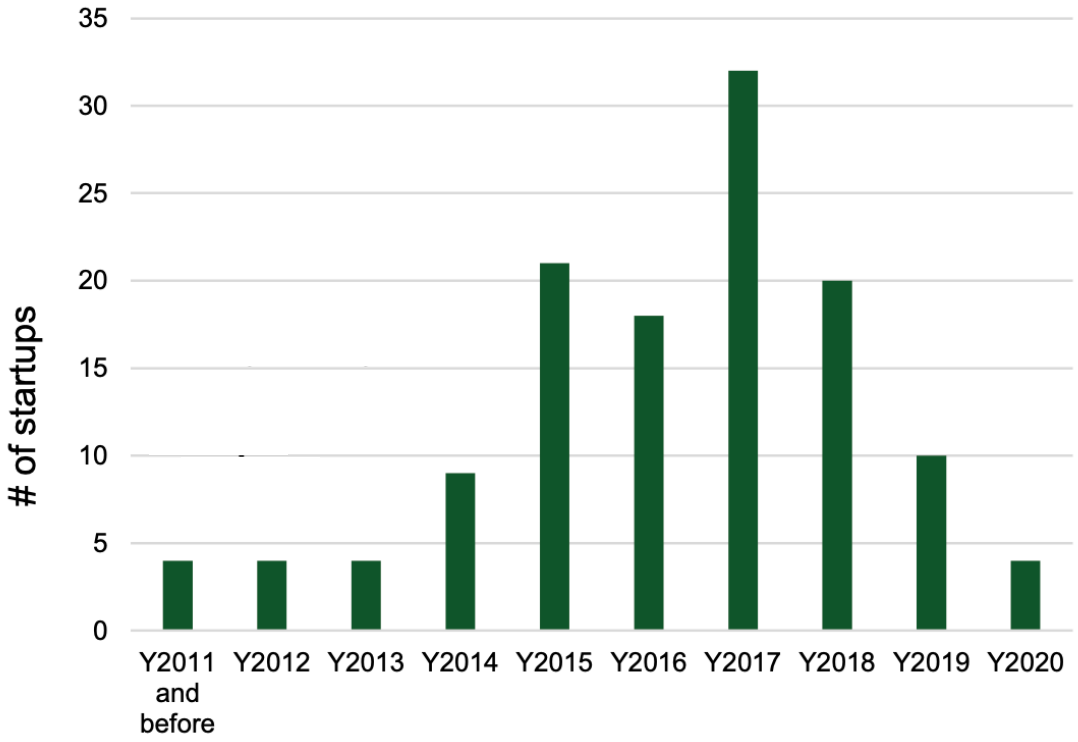


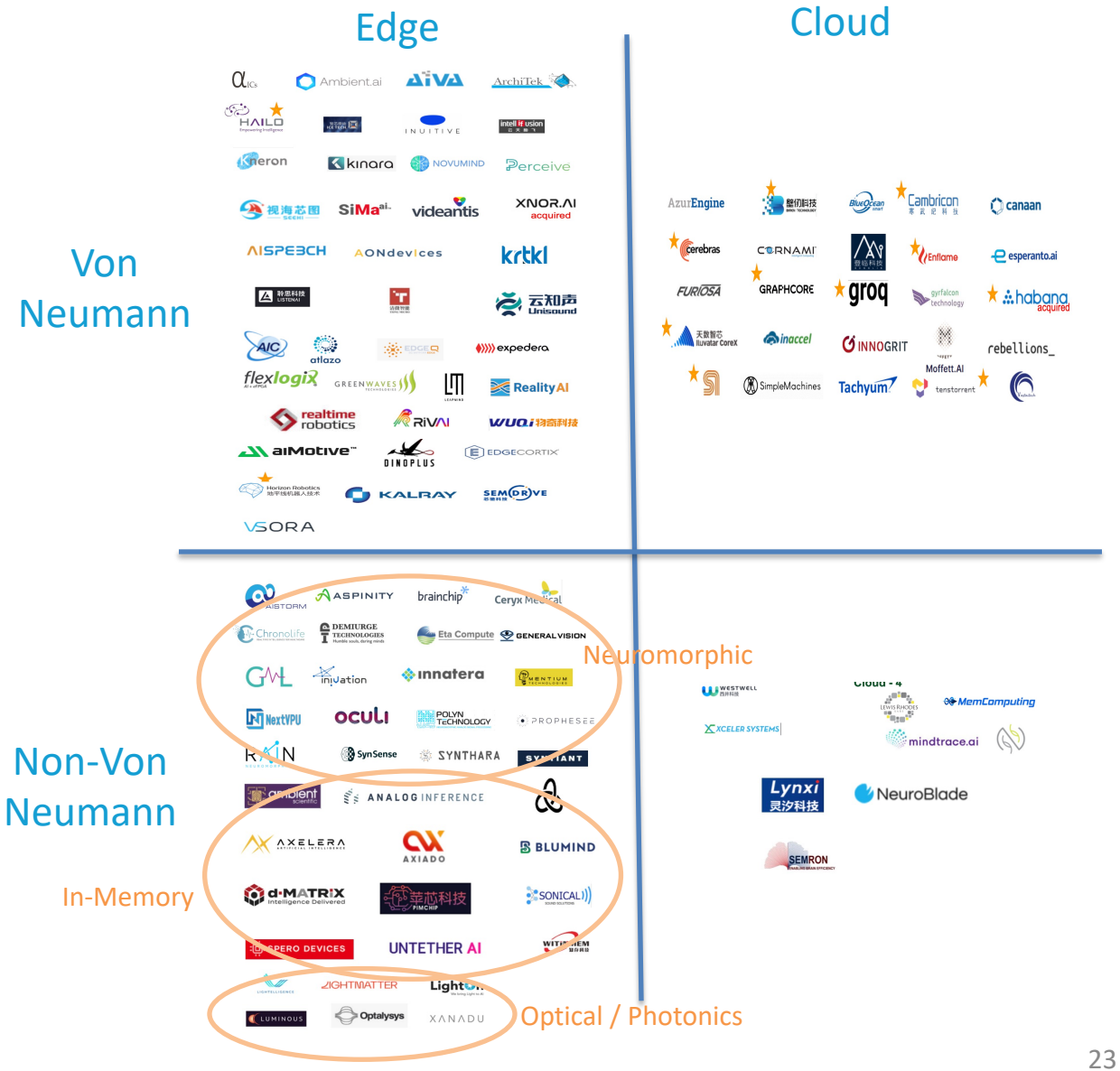
AI funding by sector



The first wave of domain specific accelerators / architectures for AI

AI/ML startups formation





Source: Woodside Capital Partners

VC model at a glance

Goal is return 3-5x or 20-30% annual IRR over the 10-year life of the fund

Invest fund in 20-25 companies which represent 0.1-1% of deal flow

Hits driven business – need 1-3 companies to return 10-100x of investment

VCs are compensated 2% of fund annually for OpEx and retain 20% (carry) of profits

Each startup funding round is lead by a new VC that sets the valuation and investing terms for others, and for existing investors, exercising pro-rata rights is key

VCs raise follow-up funds based upon track record of the prior funds

VC model dictates where investments are made and why semiconductors struggle

Investments in semiconductors are less attractive compared to software and services

- Higher capital required
- Longer time to revenue ramp
- Higher innovation failure rates
- Longer time to liquidity
- Lower returns

Semiconductors requires extensive and specific due diligence, a skill mostly atrophied

Product-market fit is hard to predict based upon early measures of traction and adoption

Challenges facing semiconductor startups

Time, EDA, Prototypes, Test, $'s

Source: 70 startups surveyed in 2014 & > 500 startups 2015 – 2023

Source: Silicon Catalyst

Incubator and accelerator services have helped startups in other arenas

Office space

Infrastructure: HR, Fin, Legal, IP, IT

Curriculum

Events (Demo/Pitch Day)

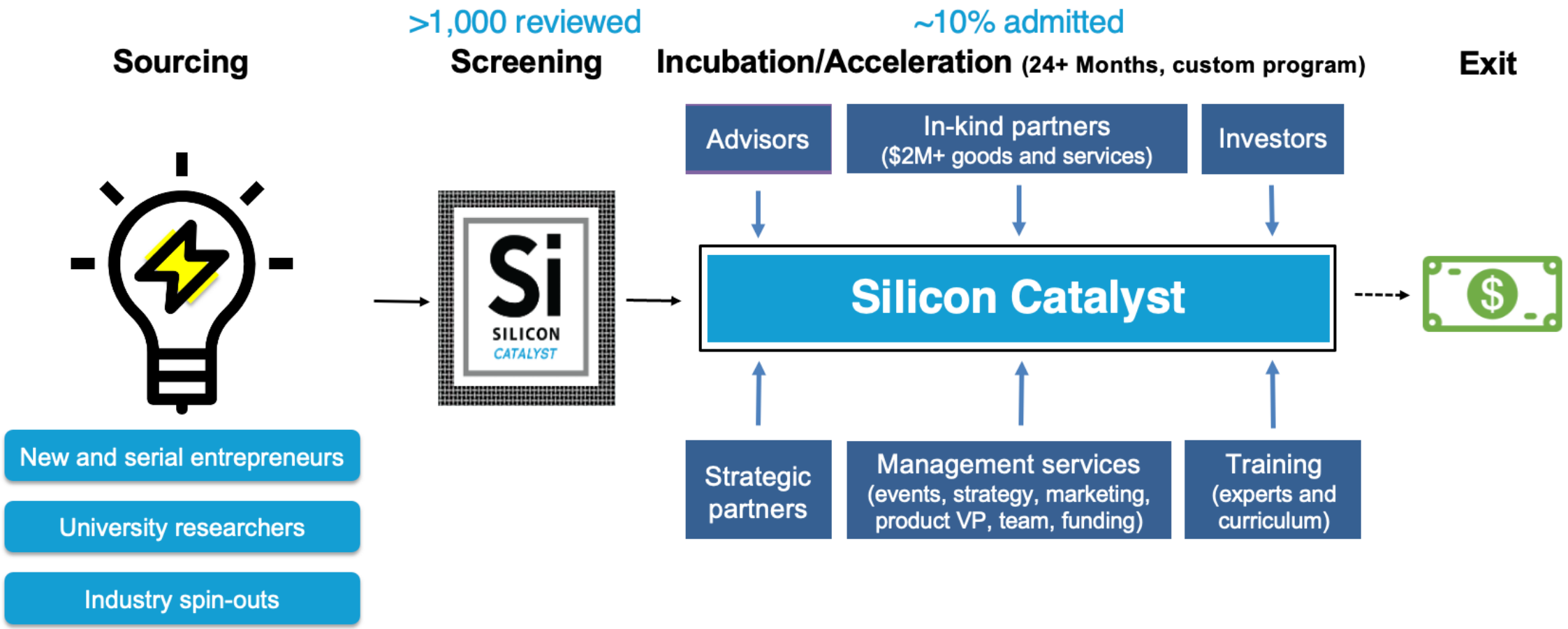
Ecosystem access

Prototyping/software/services

Mentors / Advisors

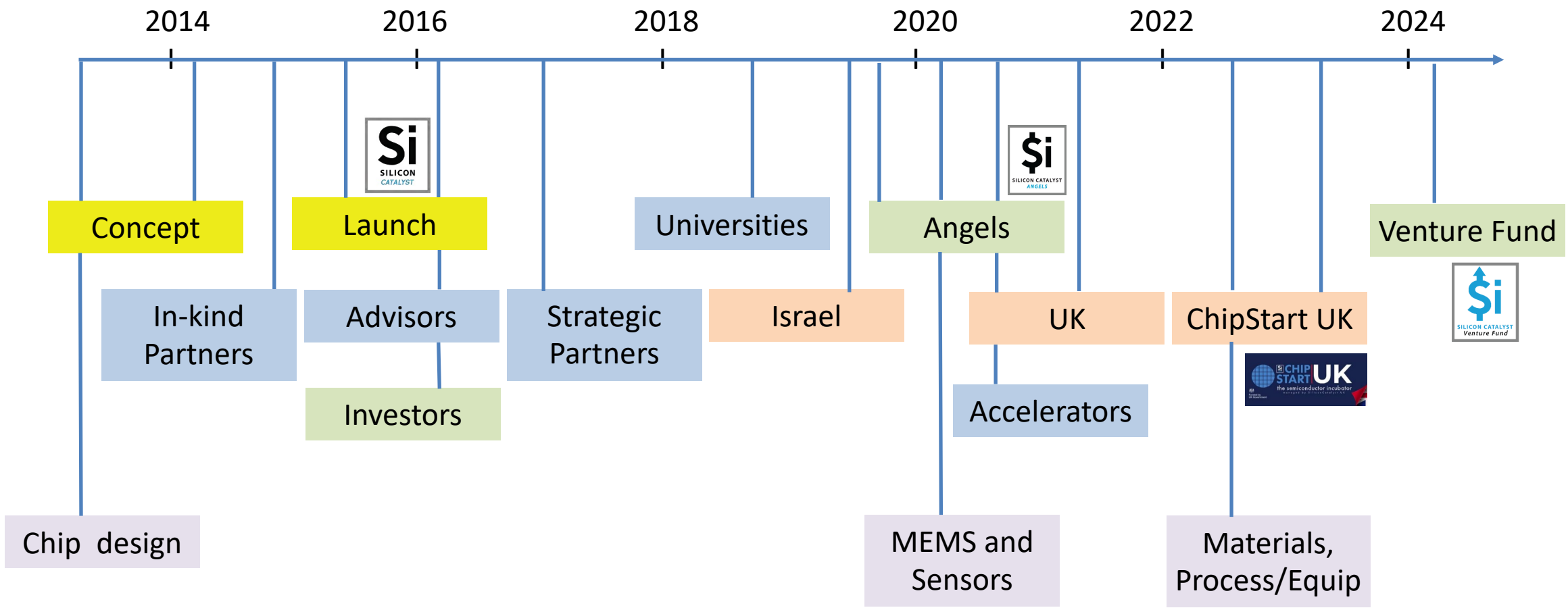
Seed funding

Silicon Catalyst accelerator model is tuned to semiconductor startup needs



Source: Silicon Catalyst

Silicon Catalyst timeline



Silicon Catalyst ecosystem has grown over its first 9 years

Over 90 startups – portfolio >$1.9B valuation, >$500M raised

International
Israel & UK Teams
Advisors worldwide

Industry Partners

35+ Universities

Accelerators

Source: Silicon Catalyst

Silicon Catalyst services are available from the industry's ecosystem

Source: Silicon Catalyst

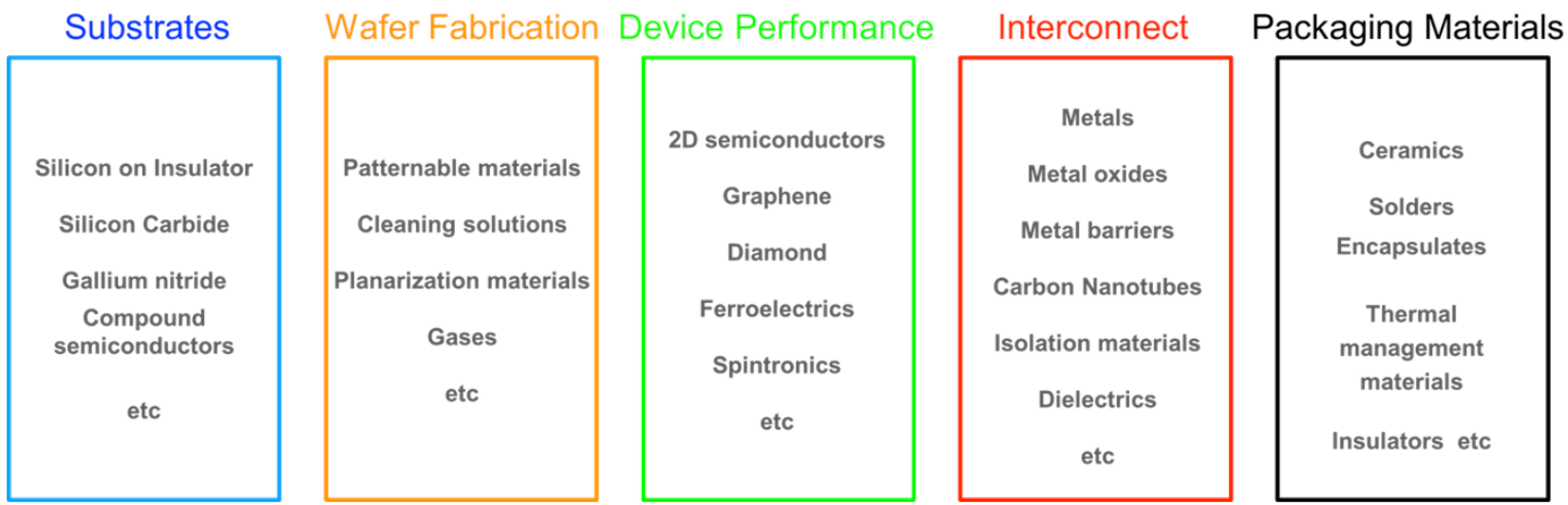
Within semiconductors, what's not receiving its share of love?

Materials/process changes

New materials and devices

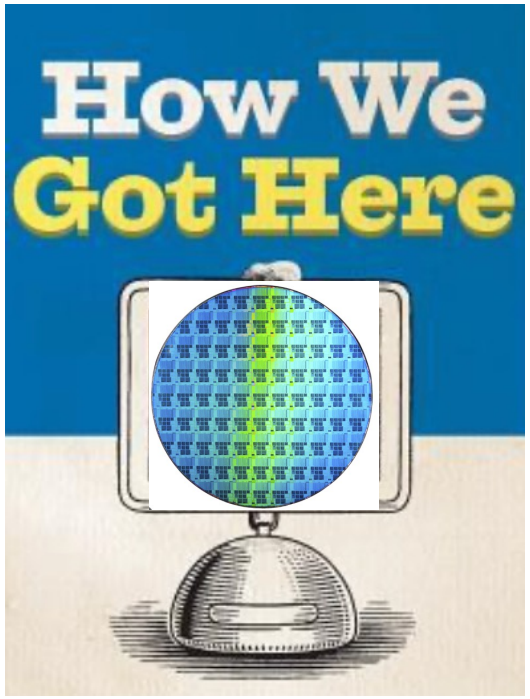
New equipment and processes

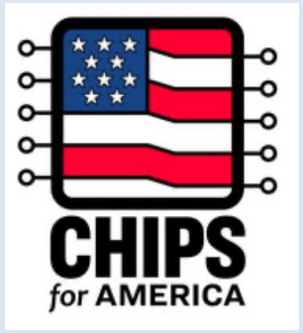
EDA for emerging technologies



Source: Silicon Catalyst

Semiconductor startups and investments

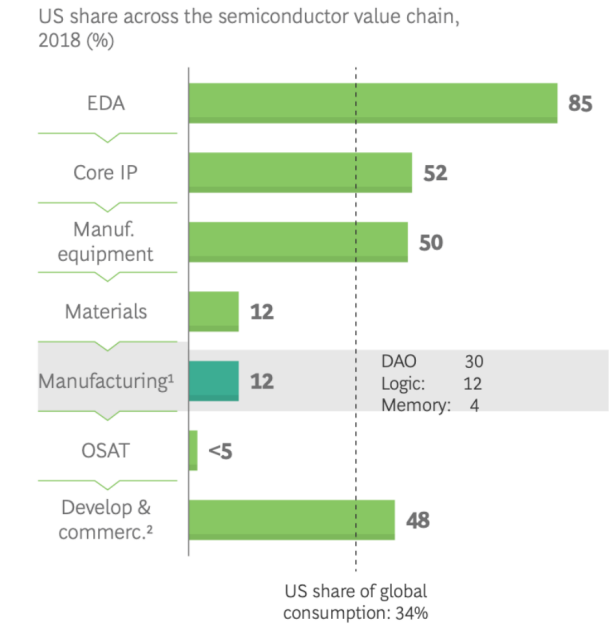




CHIPS and Science Act of 2022 – signed into law in August

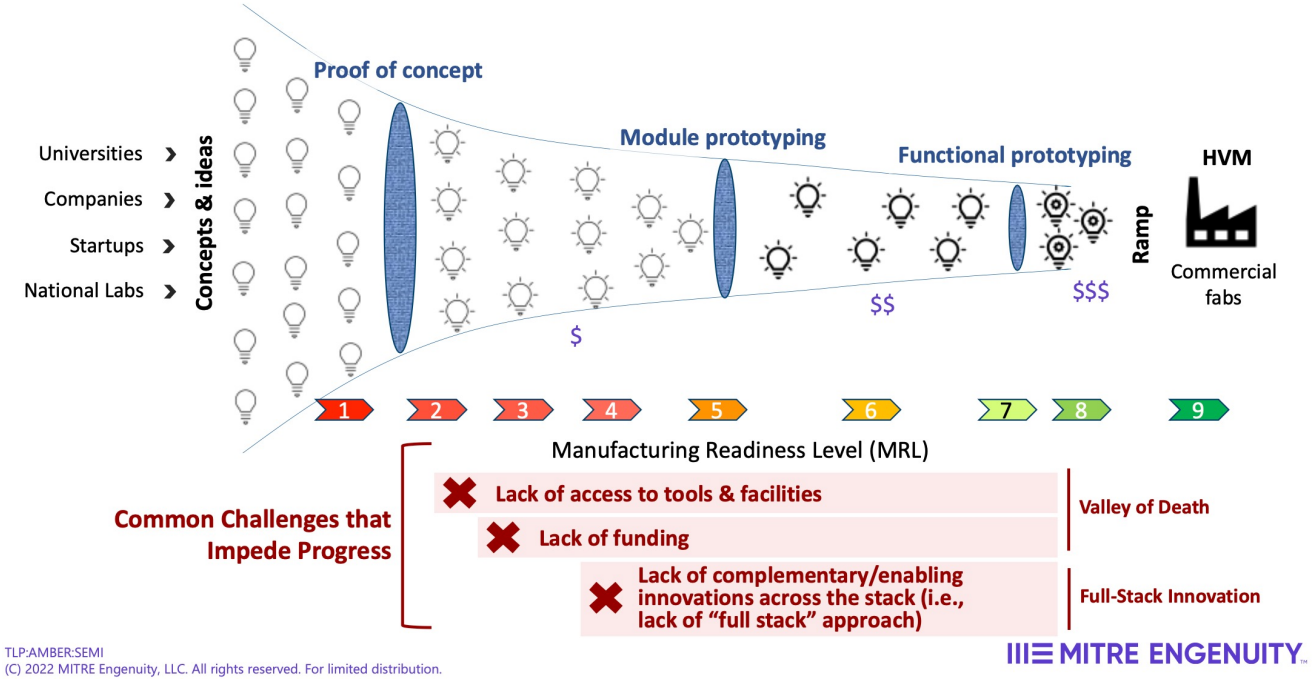
CHIPS Act: $52B funding and $24B tax incentives over 5 years

$39B for manufacturing outcomes



A. Varas, R. Varadarajan, J. Goodrich, and F. Yinug, September 2020, BCG & SIA

$11B for R&D (NSTC) and Advanced Packaging (NAPMP)



MITRE ENGENUITY

$24B (25%) in facility and equipment tax credits

$2B for DOD "Commons" - regional hubs for prototyping

The innovation gap is what the CHIPS Act R&D provisions are about

DARPA ERI

$1.5B – 5 yrs

SRC nCORE JUMP

$200M – 5 yrs

U.S. DEPARTMENT OF ENERGY BES

NSF MRSEC STSC

GAPS

Prototyping at scale

Scale-up business model

Startup funding

Gov. agency coordination

leti cea tech

imec

Colleges of Nanoscale Science and Engineering · SUNY Polytechnic Institute ·

Semiconductor Industry

20 years 15 10 5 0

TRL1 TRL9

CHIPS Act Industrial Advisory Committee (IAC)

IAC Members

Industry

Mike Splinter
Chair
MRS Business and Technology Advisors

Susan Feindt
Vice-Chair
Analog Devices

Susie Armstrong
Qualcomm

Ahmad Bahai
Texas Instruments

Deirdre Hanford
Synopsys

Ken Joyce
Brewer Science

Ann Kelleher
Intel Corporation

Mukesh Khare
IBM Research

Meredith LaBeau
Calumet Electronics

Om Nalamasu
Applied Materials

Debo Olaosebikan
Kepler Computing

Mark Papermaster
AMD

WG member only

Alex Oscilowski
TEL America

Anthony Yer
ASML Technology Center

Scott DeBoer
Micron

WG member only

Ecosystem/ Customers

Daniel Armbrust
Silicon Catalyst

Bill Chappell
Microsoft

Charles Gray
Ford Motor Company

Todd Younkin
SRC

WG member only

Academia/Other Stakeholders

James Ang
Pacific Northwest National Laboratory

Michael Fritze
Potomac Institute for Policy Studies

Carol Handwerker
Purdue University

Rajarao Jammy
MITRE Engenuity

Tsu-Jae King Liu
University of California Berkley

Willy Shih
Harvard Business School

Brandon Tucker
Washtenaw Community College

H.S. Philip Wong
Stanford University

IAC timeline and charges

		R&D GAPS WG	PPP WG	WORKFORCE WG	COMBINED WG
Sep ‘22	Announcement				
Dec ‘22	#1 - Wash DC	R&D Gaps	Organization and PPP	Workforce	x
Feb ‘23	#2 - Virtual	R&D Gaps	Organization and PPP	Workforce	x
Jun ‘23	#3 - Wash DC	Advanced Packaging	IP and NSTC	Workforce	Sequencing of Priorities
Nov ‘23	#4 - Virtual	Metrology and Standards	Investment Fund	x	x

IAC R&D Gaps recommendations

Recommendation 1:

Establish a set of five key capabilities aimed to lower the barriers to entry and success for innovators. These capabilities will rely on a network of physical and virtual facilities with a digital backbone to reduce design and experimentation cycle time. These capabilities should benefit the *entire community of stakeholders and it should be of primary importance to increase access to and reduce the effective cost of accessing these capabilities over time.*

1) Establish easily accessible prototyping capabilities in multiple facilities and enact the ability to rapidly try out CMOS+X at a scale that is relevant to industry

2) Create a semiverse digital twin

3) Establish chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging

4) Build an accessible platform for chip design and enable new EDA tools that treat 3D (monolithic or stacked) as an intrinsic assumption

5) Create a nurturing ecosystem for promising startups

IAC prototyping analysis

300 mm

(1) Late-stage Prototyping
at Advanced Nodes
No Process Changes

(2) Mid/Late-stage Prototyping
CMOS+X
Changes: Mostly BEOL, some FEOL

(3) Pathfinding
New Materials/Process Dev
Process Experimentation

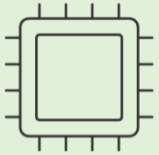
200 mm

(4) Mid/Late-stage Prototyping
CMOS + X
New Materials allowed

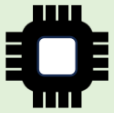
(5) Concept Hardening to Mid-stage
Changes/New Materials allowed

(6) NSTC-enhanced University Facilities
Coupons, 100/200 mm

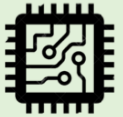
Packaging



(7a) Late-stage Prototyping
Standard Chiplet Interfaces
No or minimal changes



(7b) Pathfinding
Advanced + standard Packaging
Controlled changes allowed



(7c)Early-Stage Proof-of-Concept
Process and tool development
Changes/New Materials allowed

SIA reports (2019 and 2022) call for startup access to advanced prototyping

Prototyping and Piloting Infrastructure

The NSTC and NAPMP must go beyond only funding or coordinating existing research efforts. The two should play an active role in facilitating access to prototyping facilities or to advanced simulation and modeling software. They must also expand access to capabilities that facilitate technology transition from lab-to-fab – such as prototyping and piloting – and ensure the accessibility of these capabilities to researchers and startups. By facilitating access to these capabilities, the NSTC and NAPMP will broaden the pool of potential innovations able to traverse phases from basic research to scaling and reach commercial usefulness.

Source: SIA

PCAST report (2022) calls for a startup investment fund

★★★

REPORT TO THE PRESIDENT

Revitalizing the U.S.

Semiconductor Ecosystem

Executive Office of the President

President's Council of Advisors on Science and Technology

September 2022

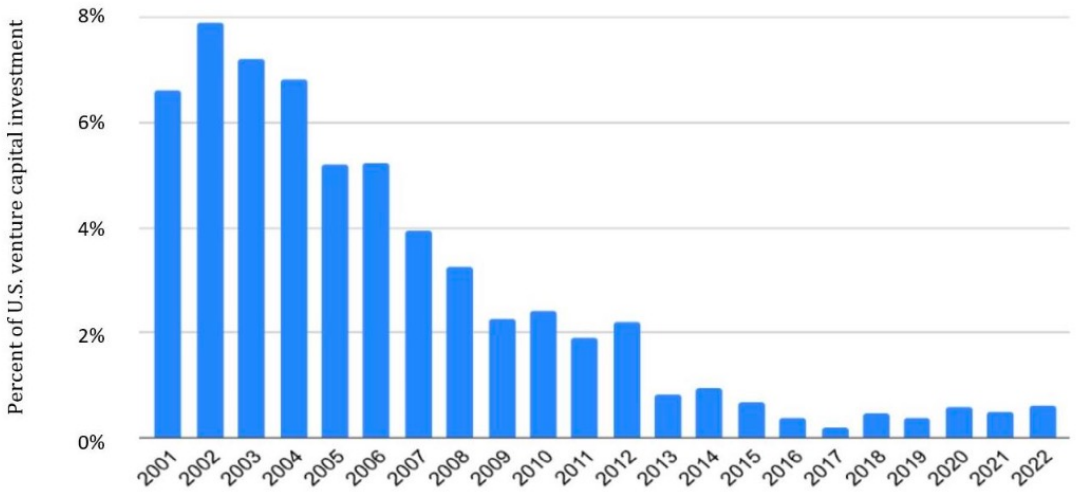
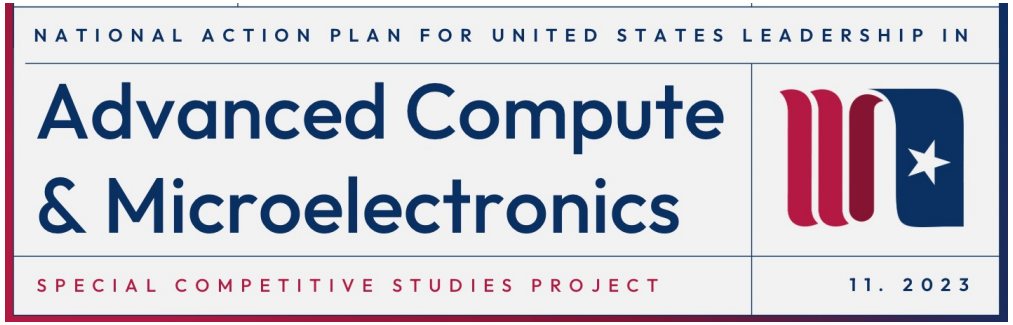


Figure 2: Percent of U.S. venture capital investment in semiconductors since 2001.
Source: Courtesy of Pear Ventures using original data retrieved from Crunchbase in August 2022.

Recommendation 6: The Secretary of Commerce should ensure that by the end of 2023, the NSTC creates an investment fund on the order of $500 million to provide financial support and in-kind access to prototyping and tools for semiconductor startups.

Source: PCAST

SCSP report (2023) recommendations for semiconductors



2.2 Optimize the NSTC Investment Fund to Pursue Disruptive Innovation

The CHIPS & Science Act authorized the NSTC to launch an investment fund that, if implemented effectively, can provide patient capital to scale transformative innovations from across the compute stack. Entrepreneurs working on disruptive technologies in the microelectronics space face daunting challenges, including very high initial costs compared to other industries and an understandable reluctance among many venture capital (VC) firms to invest in hardware technologies with a consolidated market and an uncertain timeline to commercialization.[101] Since bets by even the most accomplished VC funds fail far more often than they succeed, an NSTC fund demands a higher-than-typical tolerance for uncertainty and risk.[102]

Objective: Launch a sufficiently resourced NSTC fund, potentially via an external partner, focused on de-risking seed and early-stage startups aiming to bring disruptive technologies from across the compute stack to market.

Method: Adopt best practices from notable deep tech investment funds, such as In-Q-Tel (IQT) and The Engine, as well as impact investing principles.[103] The fund should be shaped according to the following characteristics:

- **Focus on Seed- and Early-Stage Investments.** The most significant funding gap for disruptive technologies across the microelectronics stack exists earlier in the startup
- **$500 Million Initial Capitalization.**[107] A larger fund will allow for additional shots on goal and offer additional flexibility to support scaling via larger Stage B funding rounds.
- **Capital Allocation Council.** Enabling private sector participation in the fund to provide seasoned technical expertise, evaluative discipline, and the strongest possible diligence. Select VC investors, horizon scanners, and technologists could be convened in an off-the-record, advisory fashion to support NSTC fund managers.

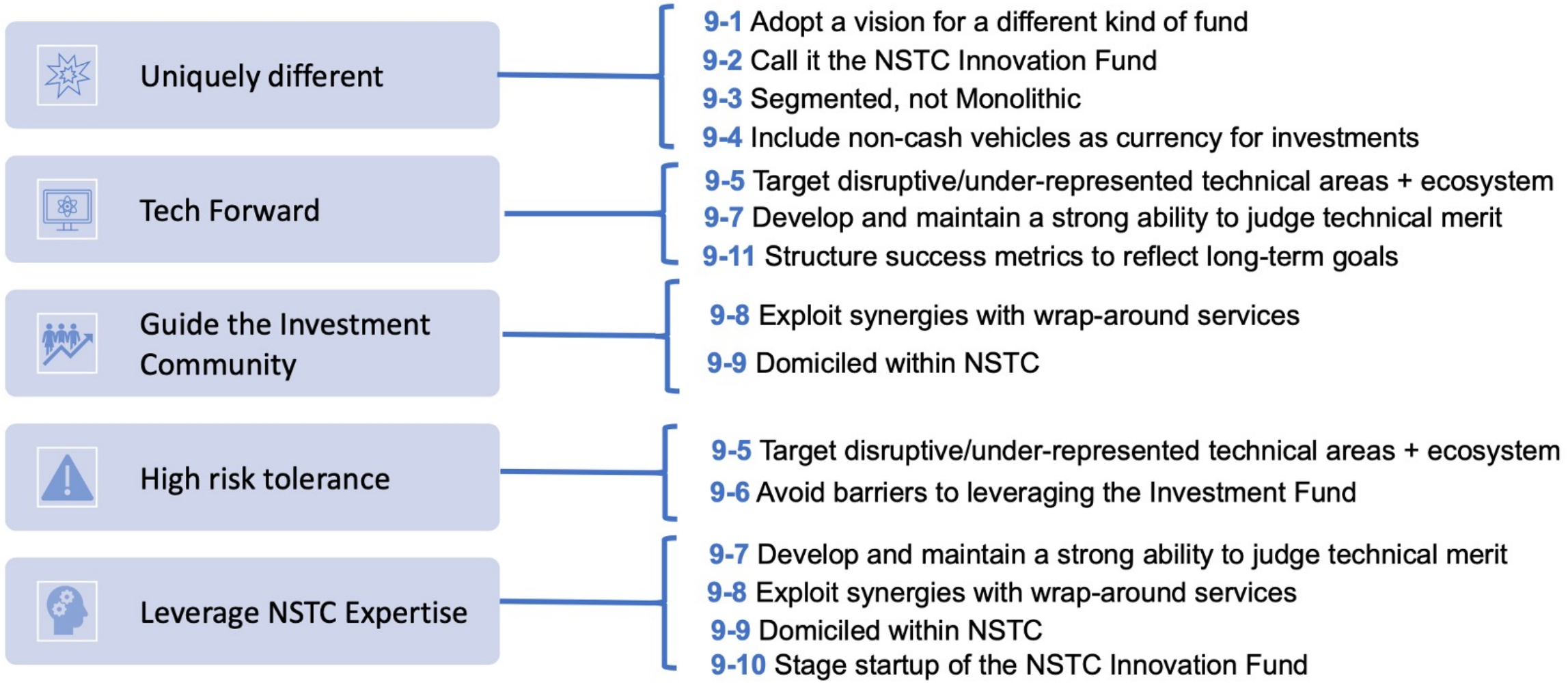
2.3 Augment the NSTC Fund with an Incubator Function

Navigating the microelectronics R&D and funding landscape can be a disorienting experience for innovators. Dozens of federal R&D programs – run seemingly in parallel and with limited connectivity – carry different requirements, grant applications, and government customers, creating hurdles that primarily impact small- and medium-size businesses. Once innovators develop a product, taking their technology to market can be an even more challenging experience. Institutionalized support is needed to increase the odds of successful commercialization.

Objective: Provide a dedicated "help desk" and commercialization support function for microelectronics researchers and innovators to lower barriers to entry.

Method: Establish an "incubator" program linked to the NSTC Investment Fund to offer commercialization support, access to cutting-edge equipment, and mentorship programs for microelectronics innovators. Dedicated commercialization support would increase the odds of success for the NSTC program and startups funded by the investment fund. Such a program should be modeled on approaches taken in recent years by established deep tech investment funds and agile government funders like IQT, DARPA, and the Defense Innovation Unit.[108]

IAC Investment fund recommendations



IAC Investment fund recommendations

Recommendation 9-1

Adopt a vision for a different kind of fund

INCREASE THE NUMBER OF *"SHOTS ON GOAL"*

INVESTMENTS SHOULD BE *TECHNOLOGY-DRIVEN*, NOT GEOGRAPHY DRIVEN

FOSTER MORE NEW *HIGH RISK*, INNOVATIVE, AND POTENTIALLY *DISRUPTIVE* OR *GROUND-BREAKING* TECHNOLOGIES

EXPECT LOWER RETURNS, AND SUSTAINING INVESTMENT WILL BE NEEDED

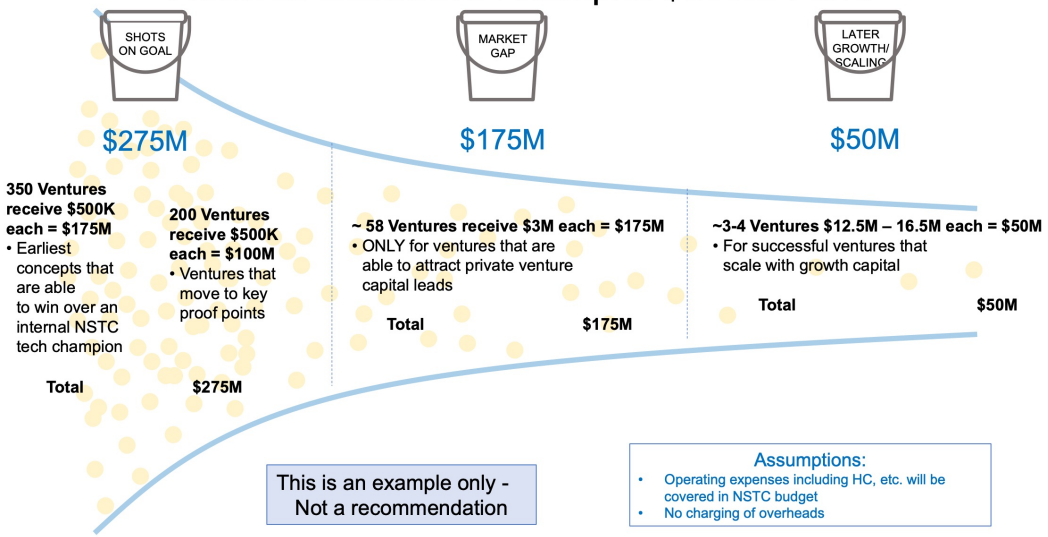
DON'T BE *AFRAID TO FAIL*, OR CUT SUPPORT QUICKLY

FOCUS ON *ACCELERATION*

This is not a profit-driven fund, and also not an evergreen model – it will need ongoing support

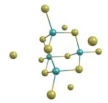
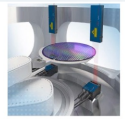
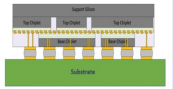
- Increase the number of entrepreneurs willing to step up to hard challenges in microelectronics
- Support firms that take more risk and have a higher failure rate
- These are bets that investors who are focused on maximizing returns would not normally take; guide the investment community by de-risking and signaling
- Ventures might be in important niche areas, and have middling returns, but are strategically vital

Notional Illustrative Example: $500M Fund



Recommendation 9-5

Target under-represented technical areas + ecosystem

Metrology for Next-Generation Microelectronics	Novel Materials	Simulation Modeling Tools	Production Tools	Packaging
				

Maximize deal flow from under-represented technical areas, including those that serve economic and national security interests

The committee specifically calls for the fund to seek high-risk technical challenges that are farther out on the risk/reward frontier than traditional venture investors might be willing to fund at inception

Look at the broader ecosystem and think strategically for the long term

Critical materials, tools, metrology, address 3D scaling challenges

Recommendation 9-10

Stage start-up of the Innovation Fund

May be advantageous to delay startup of the Innovation Fund until a later time, after the NSTC is up and running and has a clearer sense of where technology gaps, shortfalls, disruption opportunities or other priorities have emerged

- With time, the NSTC's infrastructure and in-kind services will take shape and impact how later investments will be structured.
- Sequencing of NSTC capabilities needs to be carefully considered; Innovation Fund is strategic but might not need to be an early priority

NSTC should engage startups early

- NSTC should hire initial staff in Innovation Fund early
- Start projects, grand challenges, and other programs *immediately* to start tech development
- Convene startups and investors
- Institute mentoring
- Start-ups seeking immediate support can avail themselves of NSTC wrap-around services

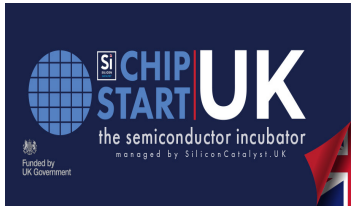
“CHIPStart UK” is an example of a fast-moving Gov’t lead initiative

5/23 UK semiconductor strategy published and funded at £1B

- DSIT responsible for execution
- Intent to create an early-stage startup program

Department for Science, Innovation & Technology

7/23 Silicon Catalyst UK selected to run startup incubator



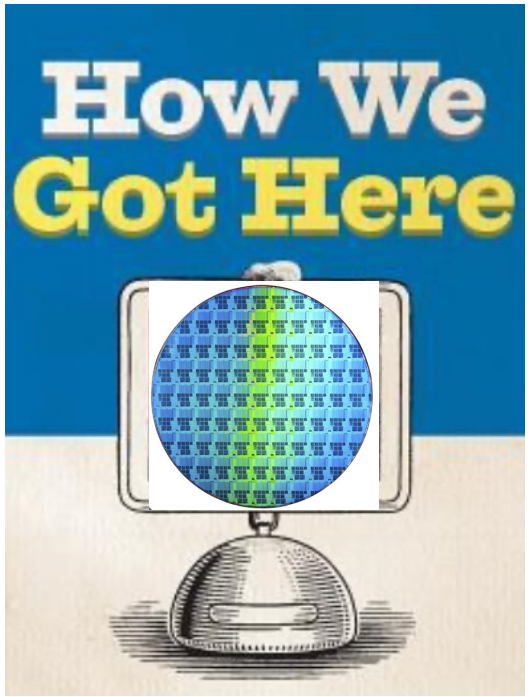
8/23 Call for applications: 27 startups applied

10/23 Final selection: 11 startups admitted for 9-month program

2/24 Call for 2nd cohort applications

3/24 Demo day at UK Semiconductor conference sponsored by DSIT/GSA; 1st in over a decade

Semiconductor startups and investments



BEHIND THE STARTUP

CHIPS for AMERICA

Recommendations

Policy and Partnerships

Recommendations

Execute what's already been authorized and appropriated with the CHIPS Act

1) Accelerate access to affordable prototyping capabilities for startups through the various CHIPS Act initiatives
   - NSTC for silicon, NAPMP for packaging and Mfg. USA for digital twin
   - DOD Commons (Hubs) for "lab to fab" – 8 regional Hubs launched Sept 23

2) Implement NSTC's Innovation fund at a minimum of $0.5B consistent with the IAC and SCSP recommendations

Recommendations

Execute what's already been authorized and appropriated with the CHIPS Act

1) Accelerate access to affordable prototyping capabilities for startups through the various CHIPS Act initiatives
   - NSTC for silicon, NAPMP for packaging and Mfg. USA for digital twin
   - DOD Commons (Hubs) for "lab to fab" – 8 regional Hubs launched Sept 23

2) Implement NSTC's Innovation fund at a minimum of $0.5B consistent with the IAC and SCSP recommendations

Supplement with ongoing government funding streams

3) Enhance existing SBIR/STTR and DIU programs with a "fast-track entrepreneur lane" to 3x funding across NSF/DOE/DARPA/DOD/NIH

4) Leverage ongoing government initiatives by ensuring that startup investment and procurement are included (e.g., DOD NDIS ((National Defense Industrial Strategy) and SBICCT (Small Business Investment Company Critical Technologies)), and DOE Office of Science (BES) and AMO funding and loan programs

Recommendations (Part 2)

Complement by attracting further private investment

5) Increase Corporate VC (CVC) investments by 2x to provide signals to VC for early-stage startups with innovative technologies, especially in materials, metrology, processes and EDA

6) Increase the number of “Hard Tech” and specialty fund VCs by identifying and addressing gaps in incentives and policies via a neutral technology-based organization (e.g., MITRE, SRI, COC – Council on Competitiveness)

7) Commission the OSTP to establish means of collaboration with allied nations’ CHIPS Acts and ensure coordination across government agencies on initiatives that support startups

8) Enhance capital gains provisions for entrepreneurs and investors that have long liquidity timelines (e.g., QSBS - Qualified Small Business Stock for capital gains)

Bottom line up front (BLUF)

Semiconductors are resurgent

Company valuations and profitability
- 8 of the top 20 market caps in tech
- 3rd most profitable industry

AI is profoundly hardware limited -- it's the next gold rush

Essential assets in a geopolitical sea change away from globalism

Semiconductor startups face daunting challenges

Escalating cost of innovation: prototyping access and costs

Sustained decline of venture capital for semiconductors

Achieving product-market fit remains challenging

Diminished customer appetite to award design wins to startups

A surge of investments are underway

CHIPS Act(s) in various countries and regions

VCs are wading back in as there are green shoots in Deep Tech and specialty funds – A contrarian opportunity

Reasonable M&A and IPO opportunities for startups

Chiplets and advanced packaging can advantage startups

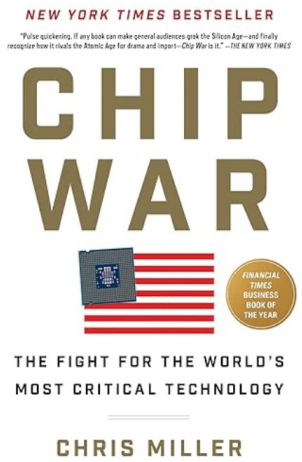
But more research will not lead to commercialization unless we continue to build the startup playbook

Aggressively implement CHIPS Act investments for prototyping and startup funds with a sense of urgency

Supplement with existing government programs and funding streams

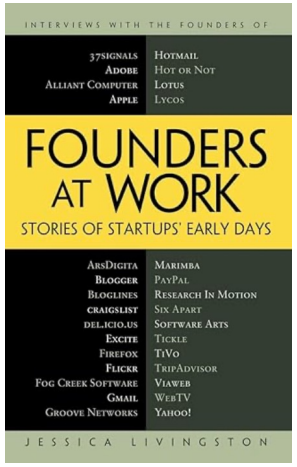
Strengthen startup ecosystem for translation to industry

Where can you learn more?



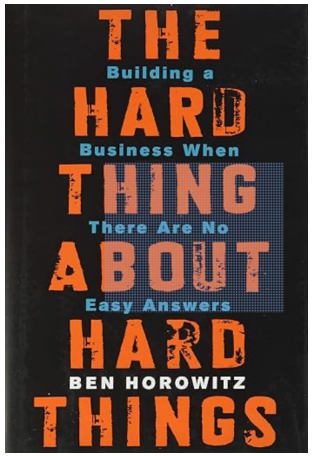
Semi History

Chris Miller



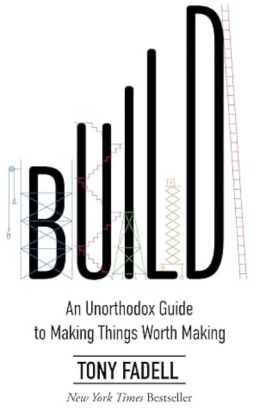
Startup stories
Internet Era

Jessica Livingston



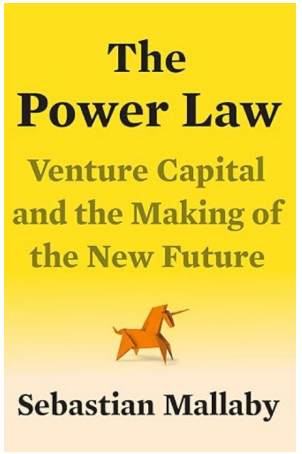
Startup stories
Cloud/SAS era

Ben Horowitz



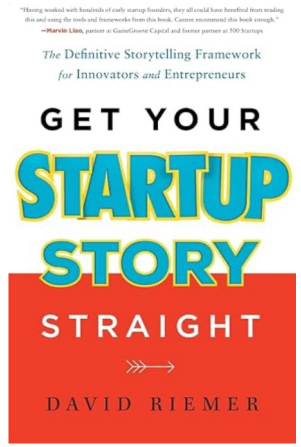
Hardware
Startups

Tony Faddell



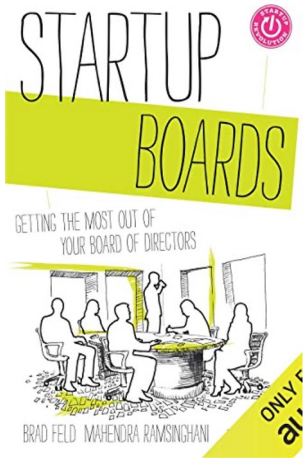
Venture Capital

Sebastian Mallaby



Funding pitchdeck
and storytelling

David Reimer



Startup Boards

Brad Feld

CHIPS Act:

- NATCAST (NSTC operator)
- DOC/NIST (CHIPS.GOV info)
- IAC (Industrial Advisory Committee)

Gov't agencies:

- DOD OSC (Office of Strategic Capital)
- DIANA (DOD Accelerator)
- DARPA ERI
- DOE BES

Thank you – Q&A

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