Encouraging Innovation: The Policies and Partnerships Needed to Support Semiconductor Startups

- Semiconductor startup and investment landscape in 2024 -

Daniel Armbrust

SIA Webinar
– April 4, 2024 –
Encouraging Innovation: The Policies and Partnerships Needed to Support Semiconductor Startups

- Semiconductor startup and investment landscape in 2024 -

Daniel Armbrust

Remarks today are made in his personal capacity, and his remarks should not be attributed to the Department of Commerce, the Industrial Advisory Committee of the CHIPS Act, or the US Government.
Semiconductor startups and investments
**Semiconductors are resurgent**

Company valuations and profitability
- 8 of the top 20 market caps in tech
- 3rd most profitable industry

AI is profoundly hardware limited -- it's the next gold rush

Essential assets in a geopolitical sea change away from globalism

**A surge of investments are underway**

CHIPS Act(s) in various countries and regions

VCs are wading back in as there are green shoots in Deep Tech and specialty funds – A contrarian opportunity

Reasonable M&A and IPO opportunities for startups

Chiplets and advanced packaging can advantage startups

**Semiconductor startups face daunting challenges**

Escalating cost of innovation: prototyping access and costs

Sustained decline of venture capital for semiconductors

Achieving product-market fit remains challenging

Diminished customer appetite to award design wins to startups

**But more research will not lead to commercialization unless we continue to build the startup playbook**

Aggressively implement CHIPS Act investments for prototyping and startup funds with a sense of urgency

Supplement with existing government programs and funding streams

Strengthen startup ecosystem for translation to industry
Semiconductor startups and investments

How We Got Here

Behind the Startup

Recommendations
Policy and Partnerships

CHIPS for AMERICA
How did we get here?

1950’s – Invention of the transistor by Bell Labs and dissemination through licensing core technology

1960’s – Integrated circuits driven by gov’t needs, invention of venture capital and startups in Silicon Valley

1970’s – Invention of microprocessors and DRAM memory

1980’s – Japanese DRAM threat leads to formation of SIA / SRC / SEMATECH to restore US competitiveness

1990’s – Foundry business model lead by TSMC in Taiwan

2000’s – Beginning of industry consolidation; decline in venture capital investment

2010’s – Moore’s Law slowdown, the rise of AI, and emergence of a Chinese threat, pricing power

2020’s – Pandemic chips shortages, CHIPS Act(s), China’s access restrictions, Generative AI
Moore’s Law economic-based prediction

Transistors on a Chip

More R&D (innovation)

Lower cost/function

$’s

Increasing semiconductor revenue

Expanding applications (more silicon)


Source: WSTS

Source: IC Insights
From U.S. startups and venture capital to geographic dispersion and consolidation

**Country Market share (IC Insights)**

- **US**
  - 54%

- **EU**
  - 6%

- **Taiwan**
  - 22%

- **Japan**
  - 6%

- **Korea**
  - 9%

- **China**
  - 5%

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### 1960’s

- **Fairchild Semiconductor**
  - Co-founder Gordon Moore, Sheldon Roberts, Eugene Weizer, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni, Jay Last

- **SIDA Systems**
  - Co-founder Michael R. Harrity, Kamran Elahian, five others

- **Sierra Semiconductor**
  - Co-founder James Diller, four others

- **National Semiconductor**
  - Co-founder Charles Spink, two others

- **Computer Microtechnology**
  - Co-founder John Schmerl, six others

- **VLSI Technology**
  - Co-founder Jack Bokoff, Dan Floyd, Gene Marks

- **NeoMagic**
  - Co-founder Prakash Agarwal

- **Linpack**
  - Co-founder James Solomon

- **Microdevices**
  - Co-founder R. Bollinger, six others

- **Wafers Scale Integration**
  - Co-founder Eli Harari

- **Synertek**
  - Co-founder Robert Schmerl, R. Bollinger, six others

- **Zilog**
  - Co-founder Federico Faggin, Ralph Cordini

- **Xilinx**
  - Co-founder Bernard Vonderschmitt

- **LSI Logic**
  - Co-founder Wilfried Conigian

- **Celoxics**
  - Co-founder James Diller, four others

- **AMD**
  - Co-founder W. L. Sanders II, seven others

- **Cybus**
  - Co-founder T. J. Rodgers, Lowell Tuffi

- **Coventor**
  - Co-founder Michael R. Harrity, Kamran Elahian, five others

- **Synopsys**
  - Co-founder杯 A. B. Pnueli, Ingo Mannhart, Gene Hall

- **Silicon Graphics**
  - Co-founder John Hennessy

- **Synapse**
  - Co-founder Bob Grubbs

- **Four Phase**
  - Co-founder Lee Byrd, Jack Fauch

- **Kleiner Perkins Caufield & Byers**
  - Co-founder Tom Steyer

- **Monsanto**
  - Co-founder Robert Swanson, two others

- **Sierra Systems**
  - Co-founder James Diller, four others

- **CA**
  - Co-founder John Donlon

- **Metron**
  - Co-founder Jack Baletto, seven others

- **S3**
  - Co-founder Dado Banait

- **Fibrelink**
  - Co-founder Michael R. Harrity, Kamran Elahian, five others

- **Cypress**
  - Co-founder T. J. Rodgers, Lowell Tuffi

- **LSI Logic**
  - Co-founder Wilfried Conigian

---

### 2020’s

- **Intel**
  - Co-founder Robert Noyce, Gordon Moore

- **AMD**
  - Co-founder W. L. Sanders II, seven others

- **Apple**
  - Co-founder Steve Jobs

- **Google**
  - Co-founder Larry Page

- **Microsoft**
  - Co-founder Bill Gates

- **Tesla**
  - Co-founder Elon Musk

- **Amazon**
  - Co-founder Jeff Bezos

- **Zappos**
  - Co-founder Tony Hsieh

- **Spotify**
  - Co-founder Daniel Ek

- **Snapchat**
  - Co-founder Evan Spiegel

- **SpaceX**
  - Co-founder Elon Musk

- **Palo Alto Networks**
  - Co-founder Sandeep Chauhan

- **Salesforce**
  - Co-founder Marc Benioff

- **Slack**
  - Co-founder Stewart Butterfield

- **Tesla**
  - Co-founder Elon Musk

- **Uber**
  - Co-founder Travis Kalanick

- **Airbnb**
  - Co-founder Brian Chesky

- **Dropbox**
  - Co-founder Drew Houston

- **Twitter**
  - Co-founder Jack Dorsey

- **Lyft**
  - Co-founder John Zimmer

- **Visa**
  - Co-founder Jim McKee

- **NVIDIA**
  - Co-founder Jensen Huang

- **GoDaddy**
  - Co-founder Robb Scott

- **LinkedIn**
  - Co-founder Reid Hoffman

- **Foursquare**
  - Co-founder Dennis Crowley

- **Quora**
  - Co-founder Adamd D’Angelo
Evolution of the supply chain and its fragmentation

**historical**

- Integrated Device Manufacturer (IDM)
  - Systems
  - Design
  - Packaging and Assembly
  - Chip Technology
  - EDA Tools
- Equipment and Materials

**now**

- System
- Fabless Fablite
- Package and Assembly
- Memory Logic IDM
- Foundries
- EDA Equipment Materials
Consolidation and concentration in each segment

Semiconductor M&A Valuation

Source: IC Insights

$22.7B $20.6B

Chip design costs

Source: M. Lapadeus, Semi Eng.

Equipment Market Share

Source: VLSI Research, 2020

Logic/Foundry platforms


DRAM Market Share

Source: IC Insights
Evidence of Moore’s Law slowdown – scaling is in trouble

Source: Hennessy/Patterson Turing Award presentation
Some consolation until the next new thing: solid roadmap for next decade

CMOS Roadmap to <1.0 nm

EUV Lithography

Backside Power Distribution

Advanced packaging

Source: IMEC, ASML, IMEC, Applied Materials (clockwise)
System companies becoming silicon houses

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<th>Apple</th>
<th>Google</th>
<th>Amazon</th>
<th>Microsoft</th>
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China export controls and trade restrictions are stressing globalism.

- **HiSilicon products to Huawei**
- **Nvidia/AMD AI class processors**
- **SMIC foundry below 10nm**
- **All fabs, then YMTC**
- **US made equip and EDA**
  - ASML EUV Lithography
  - EDA for GAA
  - All advanced fabs
- **Huawei 5G network chips**

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<th>Year</th>
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<th>2021</th>
<th>2022</th>
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<td>Global</td>
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Venture Capital has moved past semiconductors to software and services

Source: Pear Ventures & Crunchbase
Semiconductor startups and investments
Typical semiconductor startup timeline

**Funding Round**
- Pre-seed
- Seed
- Series A
- Series B
- Series C...
- IPO or M&A

**Funding Source**
- Self / F&F
- Angels
- VC and CVC
- Grants (SBIR ...)
- NSF, DOD, DOE, DARPA

**Fund raise ($M)**
- Low
  - 0.5
  - 1-2
  - 2
- Medium
  - 1
  - 2-5
  - 15
- High
  - 5
  - 10-20
  - 100
  - 20
  - 30-70
  - 150
  - 30
  - 50-100
  - 150
  - 100
  - 200-300
  - 500
Dramatic ramp of venture investment in the last decade – semis not benefiting

US VC investments (25 years)

1987
$0.4B - semi
8.9%

2022
$6.1B - semi
$244.5B - total
2.5%

US VC investments in semiconductors (15 years)
**VC by Deal Count**

<table>
<thead>
<tr>
<th>Company</th>
<th>Deal Count</th>
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<td>Celesta</td>
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**CVC by Deal Count**

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Pitchbook, 2014-2024
Venture Capital exits and funds raised – rapid reversal of positive trends

VC exits (IPO, M&A)

US VC exit activity

VC capital raised

US VC fundraising activity
Downturn in Venture Capital startup funding from 2021 peak

US VC investments – All stages

Pre-seed and Seed

Early Stage (Series A/B)

Late Stage (Series C/D)

PitchBook-NVCA Venture Monitor • As of December 31, 2023
Venture Capital investments in AI/ML have escalate
The first wave of domain specific accelerators / architectures for AI

Source: Woodside Capital Partners
VC model at a glance

Goal is return 3-5x or 20-30% annual IRR over the 10-year life of the fund

Invest fund in 20-25 companies which represent 0.1-1% of deal flow

Hits driven business – need 1-3 companies to return 10-100x of investment

VCs are compensated 2% of fund annually for OpEx and retain 20% (carry) of profits

Each startup funding round is lead by a new VC that sets the valuation and investing terms for others, and for existing investors, exercising pro-rata rights is key

VCs raise follow-up funds based upon track record of the prior funds
Investments in semiconductors are less attractive compared to software and services
- Higher capital required
- Longer time to revenue ramp
- Higher innovation failure rates
- Longer time to liquidity
- Lower returns

Semiconductors requires extensive and specific due diligence, a skill mostly atrophied

Product-market fit is hard to predict based upon early measures of traction and adoption
Challenges facing semiconductor startups

Source: Silicon Catalyst

Rank Issues
Rank Expenses
Top Challenges

Time, EDA, Prototypes, Test, $'s

Source: 70 startups surveyed in 2014 & + 500 startups 2015 - 2023
Incubator and accelerator services have helped startups in other arenas

Office space
Infrastructure: HR, Fin, Legal, IP, IT
Curriculum
Events (Demo/Pitch Day)

Ecosystem access
Prototyping/software/services
Mentors / Advisors
Seed funding
Silicon Catalyst accelerator model is tuned to semiconductor startup needs

Sourcing

New and serial entrepreneurs
University researchers
Industry spin-outs

>1,000 reviewed
Screening

Incubation/Acceleration (24+ Months, custom program)

~10% admitted

Silicon Catalyst

Advisors
In-kind partners ($2M+ goods and services)
Investors

Strategic partners
Management services (events, strategy, marketing, product VP, team, funding)
Training (experts and curriculum)

Exit

Source: Silicon Catalyst
Silicon Catalyst timeline

- **2014**
  - Concept
  - In-kind Partners
  - Chip design

- **2016**
  - Launch
  - Advisors
  - Investors

- **2018**
  - Universities
  - Strategic Partners

- **2020**
  - Angels
  - Israel
  - MEMS and Sensors

- **2022**
  - UK
  - Accelerators
  - Materials, Process/Equip

- **2024**
  - Venture Fund
  - ChipStart UK
Silicon Catalyst ecosystem has grown over its first 9 years

Over 90 startups – portfolio >$1.9B valuation, >$500M raised

International
Israel & UK Teams
Advisors worldwide

Industry Partners
GSA
SIIA
semi
PitchBook

Strategic Partners
arm

In-Kind Partners

Advisors
300+

Investors
300+

Accelerators
PRAXIS CENTER

International
Israel & UK Teams
Advisors worldwide

Industry Partners
GSA
SIIA
semi
PitchBook

Strategic Partners
arm

In-Kind Partners

Advisors
300+

Investors
300+

Accelerators
PRAXIS CENTER

Source: Silicon Catalyst
Silicon Catalyst services are available from the industry’s ecosystem

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<tr>
<th>EDA</th>
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In-Kind Partners

1 Low Volume; 2 High Volume Yield Improvement; 3 Israel Only; 4 UK Only

Source: Silicon Catalyst
Within semiconductors, what’s not receiving its share of love?

- Materials/process changes
- New materials and devices
- New equipment and processes
- EDA for emerging technologies

Source: Silicon Catalyst
Semiconductor startups and investments

How We Got Here

BEHIND THE STARTUP

Recommendations Policy and Partnerships

CHIPS for AMERICA
CHIPS and Science Act of 2022 – signed into law in August

**CHIPS Act: $52B funding and $24B tax incentives over 5 years**

- **$39B for manufacturing outcomes**

  - US share across the semiconductor value chain, 2018 (%)
    - EDA: 85
    - Core IP: 52
    - Manuf. equipment: 50
    - Materials: 12 (DAO: 30, Logic: 32, Memory: 4)
    - Manufacturing*: 12
    - OSAT: ≤5
    - Develop & commer.²: 48

- **$11B for R&D (NSTC) and Advanced Packaging (NAPMP)**

- **$24B (25%) in facility and equipment tax credits**

- **$2B for DOD “Commons” - regional hubs for prototyping**

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A. Varas, R. Varadarajan, J. Goodrich, and F. Yihug, September 2020, BCG & SIA

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The innovation gap is what the CHIPS Act R&D provisions are about.

- $1.5B – 5 yrs (DARPA, ERI)
- $200M – 5 yrs (SRC, nCORE, JUMP)
- $200M – 5 yrs (BES, MRSEC, STSC)

GAPS:
- Prototyping at scale
- Scale-up business model
- Startup funding
- Gov. agency coordination

Semiconductor Industry

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35
## IAC timeline and charges

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<th>Date</th>
<th>Event Description</th>
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<th>PPP WG</th>
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<td>Investment Fund</td>
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IAC R&D Gaps recommendations

Recommendation 1:
Establish a set of five key capabilities aimed to lower the barriers to entry and success for innovators. These capabilities will rely on a network of physical and virtual facilities with a digital backbone to reduce design and experimentation cycle time. These capabilities should benefit the entire community of stakeholders and it should be of primary importance to increase access to and reduce the effective cost of accessing these capabilities over time.

1) **Establish easily accessible prototyping capabilities** in multiple facilities and enact the ability to rapidly try out CMOS+X at a scale that is relevant to industry

2) Create a semiverse digital twin

3) **Establish chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging**

4) Build an accessible platform for chip design and enable new EDA tools that treat 3D (monolithic or stacked) as an intrinsic assumption

5) **Create a nurturing ecosystem for promising startups**
IAC prototyping analysis

300 mm

1) Late-stage Prototyping at Advanced Nodes
   No Process Changes

2) Mid/Late-stage Prototyping
   CMOS+X
   Changes: Mostly BEOL, some FEOL

3) Pathfinding
   New Materials/Process Dev
   Process Experimentation

200 mm

4) Mid/Late-stage Prototyping
   CMOS + X
   New Materials allowed

5) Concept Hardening to Mid-stage
   Changes/New Materials allowed

6) NSTC-enhanced University Facilities
   Coupons, 100/200 mm

Packaging

7a) Late-stage Prototyping
    Standard Chiplet Interfaces
    No or minimal changes

7b) Pathfinding
    Advanced + standard Packaging
    Controlled changes allowed

7c) Early-Stage Proof-of-Concept
    Process and tool development
    Changes/New Materials allowed
Prototyping and Piloting Infrastructure

The NSTC and NAPMP must go beyond only funding or coordinating existing research efforts. The two should play an active role in facilitating access to prototyping facilities or to advanced simulation and modeling software. They must also expand access to capabilities that facilitate technology transition from lab-to-fab – such as prototyping and piloting – and ensure the accessibility of these capabilities to researchers and startups. By facilitating access to these capabilities, the NSTC and NAPMP will broaden the pool of potential innovations able to traverse phases from basic research to scaling and reach commercial usefulness.
PCAST report (2022) calls for a startup investment fund

***

REPORT TO THE PRESIDENT
Revitalizing the U.S.
Semiconductor Ecosystem

Executive Office of the President
President’s Council of Advisors on
Science and Technology

September 2022

Recommendation 6: The Secretary of Commerce should ensure that by the end of 2023, the NSTC creates an investment fund on the order of $500 million to provide financial support and in-kind access to prototyping and tools for semiconductor startups.

Source: PCAST
2.2 Optimize the NSTC Investment Fund to Pursue Disruptive Innovation

The CHIPS & Science Act authorized the NSTC to launch an investment fund that, if implemented effectively, can provide patient capital to scale transformative innovations from across the compute stack. Entrepreneurs working on disruptive technologies in the microelectronics space face daunting challenges, including very high initial costs compared to other industries and an understandable reluctance among many venture capital (VC) firms to invest in hardware technologies with a consolidated market and an uncertain timeline to commercialization. Since bets by even the most accomplished VC funds fall far more often than they succeed, an NSTC fund demands a higher-than-typical tolerance for uncertainty and risk.

**Objective:** Launch a sufficiently resourced NSTC fund, potentially via an external partner, focused on de-risking seed and early-stage startups aiming to bring disruptive technologies from across the compute stack to market.

**Method:** Adopt best practices from notable deep tech investment funds, such as In-Q-Tel (IQT) and The Engine, as well as impact investing principles. The fund should be shaped according to the following characteristics:

- **Focus on Seed- and Early-Stage Investments.** The most significant funding gap for disruptive technologies across the microelectronics stack exists earlier in the startup

2.3 Augment the NSTC Fund with an Incubator Function

Navigating the microelectronics R&D and funding landscape can be a disorienting experience for innovators. Dozens of federal R&D programs — run seemingly in parallel and with limited connectivity — carry different requirements, grant applications, and government customers, creating hurdles that primarily impact small- and medium-size businesses. Once innovators develop a product, taking their technology to market can be an even more challenging experience. Institutionalized support is needed to increase the odds of successful commercialization.

**Objective:** Provide a dedicated “help desk” and commercialization support function for microelectronics researchers and innovators to lower barriers to entry.

**Method:** Establish an “incubator” program linked to the NSTC Investment Fund to offer commercialization support, access to cutting-edge equipment, and mentorship programs for microelectronics innovators. Dedicated commercialization support would increase the odds of success for the NSTC program and startups funded by the investment fund. Such a program should be modeled on approaches taken in recent years by established deep tech investment funds and agile government funders like IQT, DARPA, and the Defense Innovation Unit.
IAC Investment fund recommendations

- **Uniquely different**
  - 9-1 Adopt a vision for a different kind of fund
  - 9-2 Call it the NSTC Innovation Fund
  - 9-3 Segmented, not Monolithic
  - 9-4 Include non-cash vehicles as currency for investments

- **Tech Forward**
  - 9-5 Target disruptive/under-represented technical areas + ecosystem
  - 9-7 Develop and maintain a strong ability to judge technical merit
  - 9-11 Structure success metrics to reflect long-term goals

- **Guide the Investment Community**
  - 9-8 Exploit synergies with wrap-around services
  - 9-9 Domiciled within NSTC

- **High risk tolerance**
  - 9-5 Target disruptive/under-represented technical areas + ecosystem
  - 9-6 Avoid barriers to leveraging the Investment Fund

- **Leverage NSTC Expertise**
  - 9-7 Develop and maintain a strong ability to judge technical merit
  - 9-8 Exploit synergies with wrap-around services
  - 9-9 Domiciled within NSTC
  - 9-10 Stage startup of the NSTC Innovation Fund
IAC Investment fund recommendations

Recommendation 9-1

Adopt a vision for a different kind of fund

**This is not a profit-driven fund, and also not an evergreen model – it will need ongoing support**

- Increase the number of entrepreneurs willing to step up to hard challenges in microelectronics
- Support firms that take more risk and have a higher failure rate
- These are bets that investors who are focused on maximizing returns would not normally take; guide the investment community by de-risking and signaling
- Ventures might be in important niche areas, and have middling returns, but are strategically vital

Notional Illustrative Example: $500M Fund

- 350 Ventures receive $500K each = $175M
  - Earliest concepts that are able to win over an internal NSTC tech champion
- 200 Ventures receive $500K each = $100M
  - Ventures that move to key proof points
- 50 Ventures receive $3M each = $150M
  - ONLY for ventures that are able to attract private venture capital leads
- 1-4 Ventures = $12.5M – $16.5M each = $50M
  - For successful ventures that scale with growth capital

Total $500M

Maximize deal flow from under-represented technical areas, including those that serve economic and national security interests

The committee specifically calls for the fund to seek high-risk technical challenges that are farther out on the risk/reward frontier than traditional venture investors might be willing to fund at inception

Look at the broader ecosystem and think strategically for the long term

Critical materials, tools, metrology, address 3D scaling challenges

Recommendation 9-10

Stage start-up of the Innovation Fund

May be advantageous to delay startup of the Innovation Fund until a later time, after the NSTC is up and running and has a clearer sense of where technology gaps, shortfalls, disruption opportunities or other priorities have emerged

- With time, the NSTC’s infrastructure and in-kind services will take shape and impact how later investments will be structured.
- Sequencing of NSTC capabilities needs to be carefully considered; Innovation Fund is strategic but might not need to be an early priority

NSTC should engage startups early

- NSTC should hire initial staff in Innovation Fund early
- Start projects, grand challenges, and other programs immediately to start tech development
- Convene startups and investors
- Institute mentorship
- Start-ups seeking immediate support can avail themselves of NSTC wrap-around services
5/23 UK semiconductor strategy published and funded at £1B
   - DSIT responsible for execution
   - Intent to create an early-stage startup program

7/23 Silicon Catalyst UK selected to run startup incubator

8/23 Call for applications: 27 startups applied

10/23 Final selection: 11 startups admitted for 9-month program

2/24 Call for 2nd cohort applications

3/24 Demo day at UK Semiconductor conference sponsored by DSIT/GSA; 1st in over a decade

“CHIPStart UK” is an example of a fast-moving Gov’t lead initiative
Semiconductor startups and investments
Recommendations

Execute what’s already been authorized and appropriated with the CHIPS Act

1) Accelerate access to affordable prototyping capabilities for startups through the various CHIPS Act initiatives
   - NSTC for silicon, NAPMP for packaging and Mfg. USA for digital twin
   - DOD Commons (Hubs) for “lab to fab” – 8 regional Hubs launched Sept 23

2) Implement NSTC’s Innovation fund at a minimum of $0.5B consistent with the IAC and SCSP recommendations
Recommendations

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Supplement with ongoing government funding streams

3) Enhance existing SBIR/STTR and DIU programs with a “fast-track entrepreneur lane” to 3x funding across NSF/DOE/DARPA/DOD/NIH

4) Leverage ongoing government initiatives by ensuring that startup investment and procurement are included (e.g., DOD NDIS ((National Defense Industrial Strategy) and SBICCT (Small Business Investment Company Critical Technologies)), and DOE Office of Science (BES) and AMO funding and loan programs
**Recommendations (Part 2)**

Complement by attracting further private investment

1. Increase Corporate VC (CVC) investments by 2x to provide signals to VC for early-stage startups with innovative technologies, especially in materials, metrology, processes and EDA

2. Increase the number of “Hard Tech” and specialty fund VCs by identifying and addressing gaps in incentives and policies via a neutral technology-based organization (e.g., MITRE, SRI, COC – Council on Competitiveness)

3. Commission the OSTP to establish means of collaboration with allied nations’ CHIPS Acts and ensure coordination across government agencies on initiatives that support startups

4. Enhance capital gains provisions for entrepreneurs and investors that have long liquidity timelines (e.g., QSBS - Qualified Small Business Stock for capital gains)
**Semiconductors are resurgent**

Company valuations and profitability
- 8 of the top 20 market caps in tech
- 3rd most profitable industry

AI is profoundly hardware limited -- it’s the next gold rush

Essential assets in a geopolitical sea change away from globalism

**A surge of investments are underway**

CHIPS Act(s) in various countries and regions

VCs are wading back in as there are green shoots in Deep Tech and specialty funds – A contrarian opportunity

Reasonable M&A and IPO opportunities for startups

Chiplets and advanced packaging can advantage startups

**Semiconductor startups face daunting challenges**

Escalating cost of innovation: prototyping access and costs

Sustained decline of venture capital for semiconductors

Achieving product-market fit remains challenging

Diminished customer appetite to award design wins to startups

**But more research will not lead to commercialization unless we continue to build the startup playbook**

Aggressively implement CHIPS Act investments for prototyping and startup funds with a sense of urgency

Supplement with existing government programs and funding streams

Strengthen startup ecosystem for translation to industry
Where can you learn more?

- **CHIP WARS**
  - Chris Miller

- **FOUNDEES AT WORK**
  - Jessica Livingston

- **BUILD**
  - Ben Horowitz

- **The Power Law**
  - Sebastian Mallaby

- **GET YOUR STARTUP STORY STRAIGHT**
  - David Reimer

- **Hardware Startups**
  - Tony Faddell

- **Venture Capital**
  - Sebastian Mallaby

- **Funding pitchdeck and storytelling**
  - David Reimer

- **Startup Boards**
  - Brad Feld

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**CHIPs Act:**
- **NATCAST** (NSTC operator)
- **DOC/NIST** (CHIPS.GOV info)
- **IAC** (Industrial Advisory Committee)

**Gov’t agencies:**
- **DOD OSC** (Office of Strategic Capital)
- **DIANA** (DOD Accelerator)
- **DARPA ERI**
- **DOE BES**
Thank you – Q&A

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