Recommendations for the National Semiconductor Technology Center (NSTC)

May 2024

SIA SEMICONDUCTOR INDUSTRY ASSOCIATION

CONTENTS

INTRODUCTION

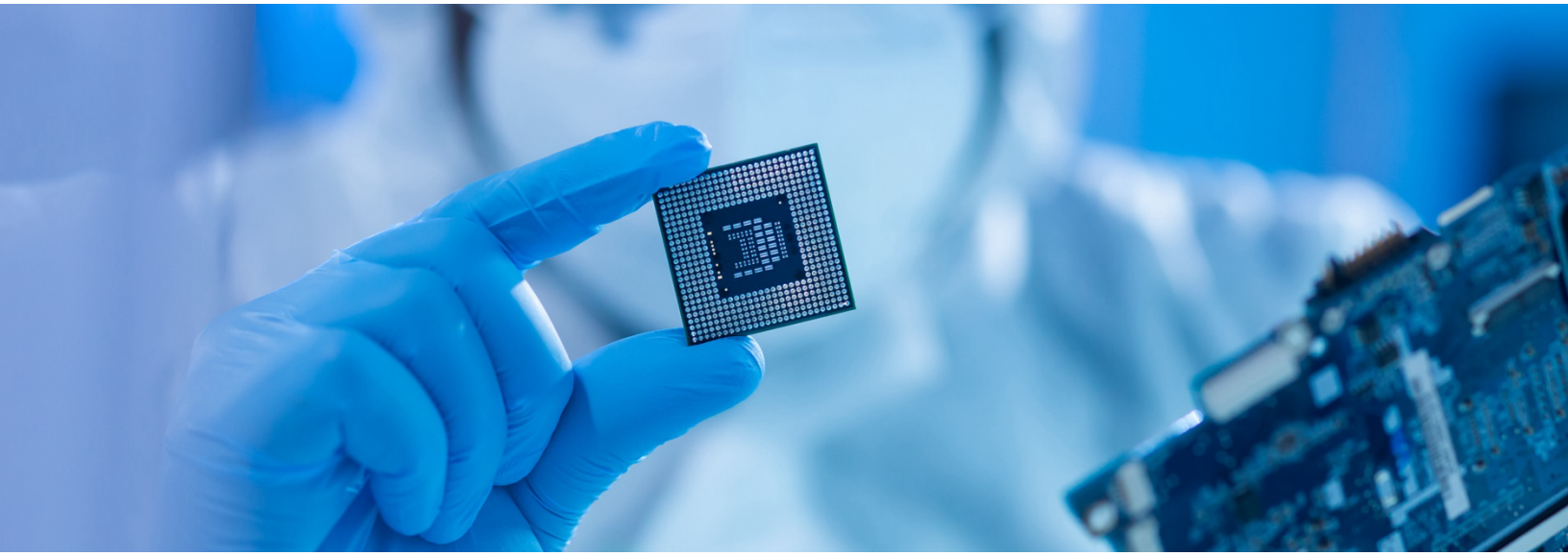
The CHIPS Act represents the most significant federal investment ever made in the U.S. semiconductor industry, including a substantial $13 billion investment in chip research and development (R&D) programs. To promote U.S. global leadership, maximize impact of these investments, and ensure the next generations of transformative technologies are developed domestically, it is essential that the CHIPS R&D program is driven by the priorities of the U.S. semiconductor industry and fosters effective collaboration across companies, government agencies, institutions of higher education, and other key stakeholders.

The cornerstone of the CHIPS R&D program is the National Semiconductor Technology Center (NSTC), a $5 billion public-private consortium that is tasked to "conduct research and prototyping of advanced semiconductor technology and grow the domestic semiconductor workforce to strengthen the economic competitiveness and security of the domestic supply chain."[1] The NSTC Consortium was formally established in February 2024 as a partnership between the Departments of Commerce, Energy, and Defense; the White House Office of Science and Technology Policy; the National Science Foundation; and the National Center for the Advancement of Semiconductor Technology (Natcast).[2] Natcast is the new, purpose-built, non-profit entity created to operate the NSTC Consortium.[3] Other CHIPS R&D programs include the National Advanced Packaging Manufacturing Program (NAPMP), a new Manufacturing USA Institute, the CHIPS Metrology Program, and the DOD Microelectronics Commons.

[1] 15 U.S.C. §4656(c)(1).

[2] White House, "Fact Sheet: Biden-Harris Administration Announces Over $5 Billion from the CHIPS and Science Act for Research, Development, and Workforce", February 9, 2024. Available at: https://www.whitehouse.gov/briefing-room/statements-releases/2024/02/09/fact-sheet-biden-harris-administration-announces-over-5-billion-from-the-chips-and-science-act-for-research-development-and-workforce/

[3] For more information on Natcast, see: https://natcast.org/.



Over the past few years, leading stakeholders have issued a number of valuable documents detailing recommendations and priorities for the initiation and operation of the NSTC. These reports include:

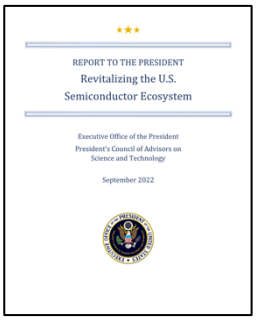
- President's Council of Advisors on Science and Technology (PCAST), "Report to the President: Revitalizing the U.S. Semiconductor Ecosystem," September 2022[4]

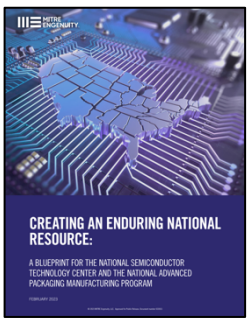
- American Semiconductor Innovation Coalition (ASIC), "Accelerating Semiconductor Research, Accelerating America: Bringing the Best Research and Development to The NSTC and NAPMP," February 2022[5]

- MITRE Engenuity (MITRE), "American Innovation, American Growth: A Vision for the National Semiconductor Technology Center," November 2021,[6] and "Creating an Enduring National Resource: A Blueprint for the NSTC and the NAPMP," February 2023[7]

- Semiconductor Industry Association (SIA), "American Semiconductor Research: Leadership Through Innovation," October 2022[8]

The CHIPS Research and Development Office (CRDO) also issued their own white paper, "A Vision and Strategy for the NSTC,"[9] in April 2023, and the CHIPS Industrial Advisory Committee (IAC) issued a series of recommendations on the CHIPS R&D programs from February to November 2023.[10]





[4] PCAST report available at: https://www.whitehouse.gov/wp-content/uploads/2022/09/PCAST_Semiconductors-Report_Sep2022.pdf
[5] ASIC white paper available at: https://asicoalition.org/vision-for-nstc
[6] MITRE (2021) report available at: https://mitre-engenuity.org/news-insights/news-release/semiconductor-alliance-vision-for-nstc/
[7] MITRE (2023) report available at: https://www.mitre.org/news-insights/news-release/mitre-engenuity-semiconductor-alliance-outline-guidance-national
[8] SIA report available at: https://www.semiconductors.org/american-semiconductor-research-leadership-through-innovation/
[9] CRDO vision document available at: https://www.nist.gov/chips/vision-and-strategy-national-semiconductor-technology-center
[10] CHIPS IAC presentations available at: https://www.nist.gov/chips/industrial-advisory-committee/industrial-advisory-committee-meetings

This body of work represents an emerging industry consensus that should form the guiding basis for CRDO and Natcast in the establishment and operation of the NSTC. This document synthesizes industry consensus and presents the most updated guidance, principles, and priorities of the SIA membership in order to promote the success of the NSTC. These key recommendations include:

1. **Industry-Driven Public-Private Partnership:** The NSTC should reflect industry technology priorities and ensure alignment with the technology agenda and roadmaps of the U.S. semiconductor industry.

2. **Objectives and Focus:** The NSTC research agenda should pursue full-stack innovation, and associated infrastructure should aim to meet piloting, prototyping, and commercial scaling needs. Research ought to engage full-system characteristics, enabling hardware/software/technology co-design across a variety of priority applications (e.g., AI inference/training, advanced driver assistance systems, extended reality, etc.) and systems (e.g., data center accelerators, smart vehicles, handhelds, wearables, etc.).

3. **Operating Structure:** The NSTC should be comprised of technology centers focused on industry subsectors (e.g., advanced logic, advanced memory, analog and mixed signal, etc.), cross-cutting R&D priorities (e.g., energy efficiency, security, etc.), and end-market working groups (e.g., auto, edge, emerging tech, etc.). The NSTC should maximize the use of existing facilities to the extent feasible and only construct new facilities where needed to achieve programmatic goals.

4. **Participation Structure:** The NSTC should primarily operate on a membership model for participation in R&D projects and facilities access, and a variety of funding mechanisms should be used to provide adequate and sustained support for a diverse set of stakeholders.

5. **Policy Considerations:** Where possible, the NSTC should leverage existing, industry-accepted protocols, and when new policies or guidance are needed (e.g., domestic production requirements, research security, and intellectual property rights), it is critical that the NSTC and all CRDO programs provide clear guidance that has been informed from industry engagement.

I. Industry-Driven Public-Private Partnership (PPP)

To achieve the innovation and commercialization goals of the CHIPS Act— "to conduct advanced semiconductor manufacturing, design, and packaging research, and prototyping that strengthens the entire domestic ecosystem"[11]—it is critical that the NSTC maintains an industry-centric focus. To this end, the CHIPS Act calls for the NSTC to be "operated as a public private-sector consortium with participation from the private sector" and key federal science agencies.[12] Effectively executing this mandate will require the NSTC to establish tight integration with industry. To meet this statutory requirement, mechanisms for regular and meaningful engagement between industry and government should be established in developing the strategy, structure, and plan of action for the NSTC.[13] As a PPP, NSTC priorities and project scope should be identified jointly across industry, government, and academia with the goals of accelerating R&D, securing American semiconductor leadership, and boosting domestic manufacturing capabilities in critical semiconductor end markets.

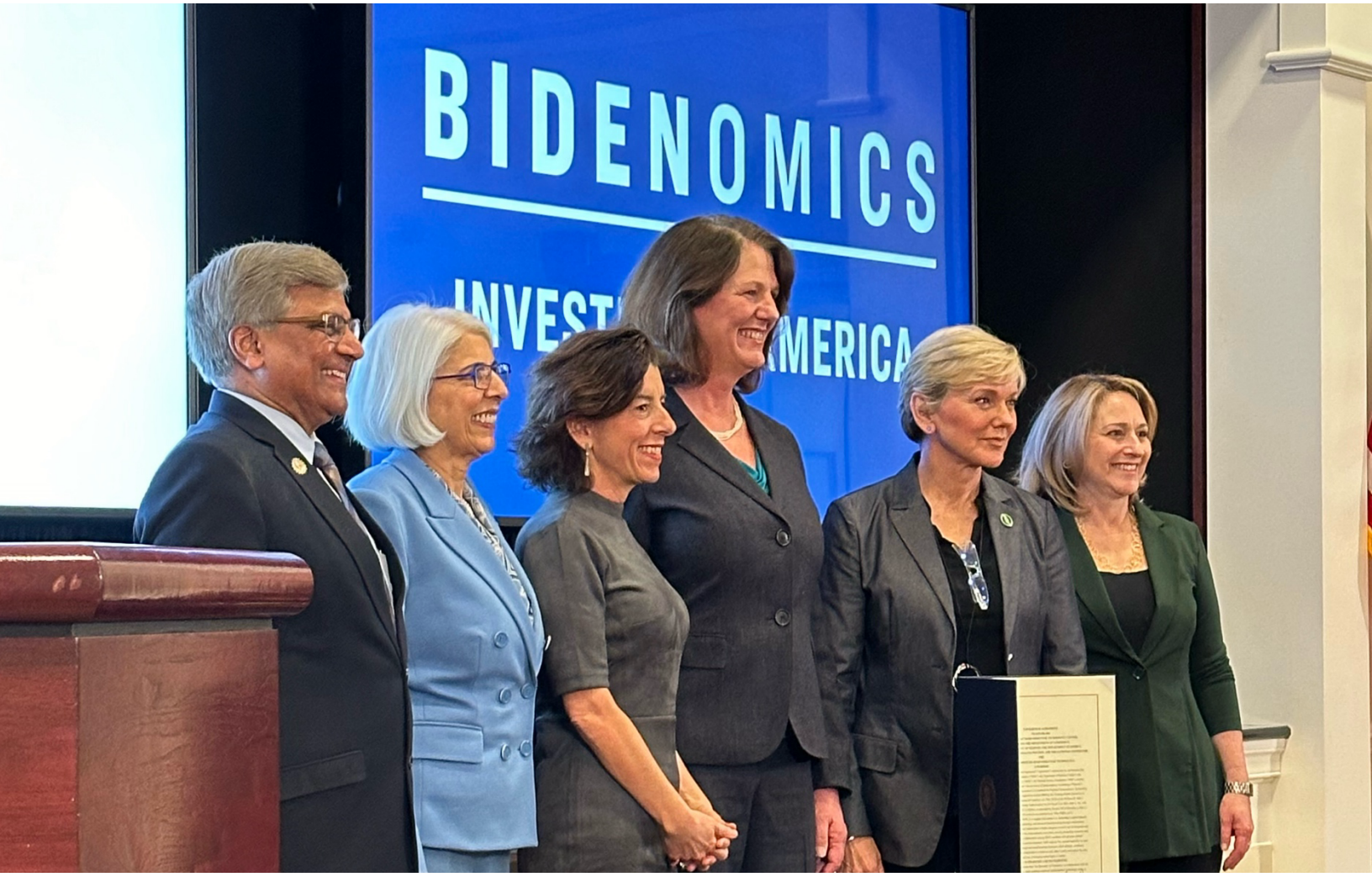
The semiconductor industry should provide ongoing guidance on strategy and operational matters. The CHIPS Act established the IAC to advise NIST on the semiconductor research programs established under the Act, and this function should be replicated to guide Natcast and the work of the NSTC. Currently, the IAC is convened by the Department of Commerce and provides guidance only on topics for which Commerce requests their input. As recommended by ASIC and MITRE, industry input should be institutionalized at multiple levels within the CHIPS R&D programs and Natcast. The IAC should continue its mission to advise at the CRDO leadership level, but the IAC (or a similar entity) should have an expanded role in advising Natcast on a broader range of activities beyond strictly what is requested. To ensure industry priorities are reflected in the operation of the NSTC, the Natcast Board of Trustees should maintain a majority of industry representatives to keep the NSTC focused on project evolution that meets industry priorities.

The NSTC should also secure program leadership with considerable experience in the private sector to facilitate an agenda that aligns with industry needs. Natcast leadership announced so far has extensive industry experience and expertise, and this dynamic should persist as Natcast continues building out its capabilities. Compensation differentials between the public and private sectors present a challenge for recruiting high-level NSTC leadership with significant

[11] 15 U.S.C. § 4656(c)(2)(A).
[12] 15 U.S.C. § 4656(c)(1). The NAPMP was established as a program within the National Institute of Standards and Technology (NIST), but it should also be operated with considerable input from industry and in close coordination with the NSTC.
[13] ASIC Coalition White Paper, at 7: "This requires a technology network led by industry in close collaboration with government and academia."

industry acumen. NSTC should make use of its other transaction authority (OTA)[14] in statute to offer compensation packages that assist in attracting industry leadership.

The CHIPS R&D Office will continue to play a vital ongoing role in monitoring progress of the NSTC with respect to advancing the national interest, especially as it relates to advancing semiconductor technologies of particular importance to the country's economic and national security. As the NSTC works to facilitate technology advancements that meet the commercial needs of the U.S. semiconductor industry, CRDO should work to ensure that R&D advancements are translating to marketplace solutions that meet the national goals of the CHIPS Act.



Above: Signing ceremony at the White House celebrating the establishment of the NSTC Consortium of the Departments of Commerce, Energy and Defense; NSF, OSTP, and Natcast.

[14] IAC Org/PPP WG (Feb., Rec. 1-1): "Structure the NSTC as a new and independent non-profit utilizing the Department's Other Transaction Authority (OTA)."

II. Objectives and Focus

A. Goals of the NSTC

Consistent with the requirements of the CHIPS Act, the NSTC agenda and investments should be targeted to provide the greatest value possible to the U.S. economy, national security, and the U.S. semiconductor industry. Some key objectives of the program should include the below:

- **Advance semiconductor science and technology across the supply chain in key R&D areas** (e.g., performance, reliability, device architectures, package design, advanced computing architectures).
- **Address technology and cost barriers to domestic production of advanced semiconductor technologies.**[15] In order to deploy new technologies domestically, companies must determine that they can do so profitably. Understanding the domestic cost drivers will help those determining a research portfolio to identify projects with the greatest potential to build domestic capacity. For example, if manufacturing a given technology is determined to have a disproportionately high labor cost in the U.S., the NSTC should work to reduce human intervention through augmented automated processes.
- **Reduce the time and cost of bringing technologies to manufacturing at scale.** A focus on accelerating these innovations and their commercial implementation will help to maintain and extend U.S. company leadership.

B. Metrics for Success

The NSTC leadership should identify a set of metrics early on by which they will assess the NSTC's impact and overall success. Industry input to identify appropriate metrics will be important, though ultimately these metrics should be agreed upon by both industry and government partners.

At the NSTC level, given the importance of private sector contribution for solidifying a sustained, long-term funding model, SIA recommends that one of the main metrics of success is the influx of private sector funding streams. The value the NSTC provides to companies will likely correlate to their willingness to contribute to research projects. The NSTC will be successful if it has a steady and growing membership, in addition to full utilization of "fee for access" services.

In the long-run, a key metric of success will be the patents that come out of NSTC projects (as well as licenses issued for those patents, both domestically and internationally).

[15] ASIC Coalition White Paper, at 5: "…functions resulting in benefits including lower costs, increased functionality…"

Robust participation and support for start-ups will also be a key measure, including the ability of start-ups to secure follow-on funding or progress to lower levels of support following NSTC projects. As directed by Executive Order 14110, the NSTC should promote competition by "implementing a flexible membership structure for the National Semiconductor Technology Center that attracts all parts of the semiconductor and microelectronics ecosystem, including startups and small firms."[16]

In addition to success metrics across the entire NSTC program, it will be important to establish and measure against goals at more program-specific levels, including at the technical centers and for cross-cutting and end-market priorities. These metrics should be utilized to track the impact of the various workstreams and technology areas under NSTC stewardship. For example:

- *Workforce development:* SIA recommends tracking the number of students that partake in NSTC activities, broken out by level of education, major, regional affiliation, demographic identifiers, etc.

- *Enabling Energy Efficiency:* Given the increasing demand for compute and the sensitivity to increased energy consumption, it is important for this cross-cutting R&D working group to develop a set of normalized metrics for success that allow for comparison across different device architectures, computing modalities, data transfer solutions, etc.

C. Focus on Prototyping and Piloting ("Lab to Fab")

The NSTC and its associated infrastructure should skew toward later technology readiness level (TRL) development and aim to meet piloting, prototyping, and commercial scaling needs, including capacity for proprietary research.[17,18,19] This will ensure that the NSTC fills a unique role in the U.S. semiconductor research ecosystem in the transition from government and

[16] White House, "Executive Order on the Safe, Secure, and Trustworthy Development and Use of Artificial Intelligence," October 2023. Available at: https://www.whitehouse.gov/briefing-room/presidential-actions/2023/10/30/executive-order-on-the-safe-secure-and-trustworthy-development-and-use-of-artificial-intelligence/

[17] ASIC Coalition White Paper, at 9: "The NSTC and NAPMP can address this critical gap by conducting research, development and prototyping in semiconductor manufacturing, packaging, and design…"

[18] IAC R&D WG (Feb., Rec. 1-1): Establish easily accessible prototyping capabilities in multiple facilities and enact the ability to rapidly try out CMOS+X at a scale that is relevant to industry.
IAC Org/PPC WG (Feb., Rec. 4-3): The NSTC should offer prototyping enablement with a translation path to multiple domestic volume production sources, encompassing the spectrum from pre-competitive to private research program types. It should lower barriers to innovation and enable smaller entities to participate.
IAC R&D WG (June, Rec. 2): Incentivize (9902) an existing wafer- and panel-based manufacturer to create prototyping capabilities in the US by establishing a pilot and initial manufacturing line, including expansion capabilities (annex) for R&D

[19] IAC Sequencing WG (June, Rec. 1-1): The working group recommends that the NSTC focus investments on two critical stages of the R&D pipeline that represent significant gaps in U.S. capabilities: 1. Mid- to late-stage prototyping beyond pathfinding. 2. Early-stage concept hardening beyond university-type research.
IAC R&D WG (June, Rec. 2): Incentivize (9902) an existing wafer- and panel-based manufacturer to create prototyping capabilities in the US by establishing a pilot and initial manufacturing line, including expansion capabilities (annex) for R&D

academic research programs to private sector entities (Figure 1). It will also address some of the most costly and operationally risky elements of private sector product development.

Existing federal research programs fund basic research in universities and national labs, and organizations like imec and the Semiconductor Research Corporation (SRC) supplement these research programs through successful partnerships with industry for earlier stage research. Industry partners have dedicated annual budgets to support these research initiatives. If the NSTC initiates activities for low-to-mid TRL projects, there is potential for it to become a de facto competitor to organizations that are already successful within their mission. At the same time, the U.S. semiconductor industry makes significant investments in product development to advance commercial technology.[20] Given this landscape, the vital contribution for the NSTC is to bridge the "lab to fab" gap and enable innovations to be developed and reach large-scale commercial production. As noted by ASIC and MITRE, underinvestment in piloting, prototyping, and commercial scaling risks not only a failure to realize the return on investment from upstream research programs, but also the possibility that other (competitor or adversarial) countries will make the investments and seize an opportunity to capitalize on U.S. innovation.

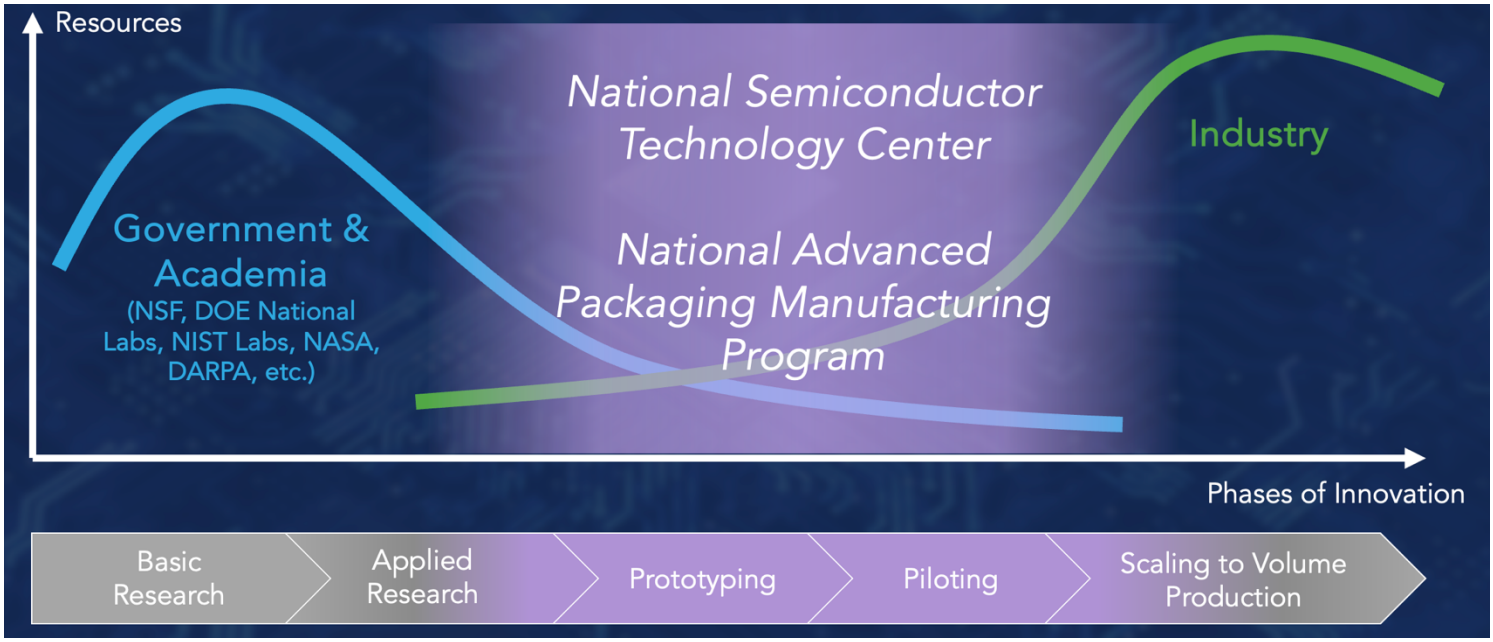


Figure 1. The NSTC and the NAPMP should aim to fill a current semiconductor ecosystem gap (i.e., the "lab-to-fab" transition) in piloting, prototyping, and scaling.

[20] Semiconductor Industry Association, "2023 State of the Industry," August 2023, at 21: "In 2022, total U.S. semiconductor industry investment in R&D totaled $58.8 billion."

D. Pursuing Full-Stack Innovation Across the U.S. R&D Ecosystem

Innovations in the semiconductor industry are interdependent, and the most impactful developments will encompass fundamental materials and device innovations, IP and design advances, manufacturing and processing technologies, and all the way up to new algorithms and software. The U.S. government science and technology enterprise will be most effective in its mission to spur continued domestic industry leadership by engaging programs all levels throughout the "stack." No one entity can or should seek to generate innovations at all levels of the stack. Rather, leadership of the CHIPS R&D programs – the CHIPS R&D Office director, the Natcast CEO and NSTC director, the NAPMP director, the CHIPS Metrology director, the DOD Microelectronics Commons director, and the CHIPS Manufacturing USA Institute director -- should all coordinate their research agendas to pursue full-stack innovation that supports and utilizes insights and successes from one program to inform research objectives in the other programs.[21, 22]

Further, outside of the CHIPS R&D initiatives, there are numerous other programs within the federal government that have equities in driving full-stack innovation for semiconductors—from funders of early science (e.g., NSF and the DOE Office of Science) to applied research programs (e.g., the DOE Advanced Materials & Manufacturing Technologies Office and the NIST Office of Advanced Manufacturing), to programs that make strategic investments in early businesses (e.g., DARPA and ARPA-E). Additionally, there are other non-governmental programs that have a decades-long histories of significant contribution in semiconductor science evolution (e.g., Semiconductor Research Corp., imec, NY CREATES, CEA Leti, etc.). In order to facilitate a whole-of-government approach that enables full-stack innovation, it is important that these programs continue with robust programming, innovation, and funding. Meanwhile, as suggested by the IAC[23] and MITRE, the NSTC should carve out a complementary, coordinated, and targeted focus so as not to become a one-stop-shop in the federal government for semiconductor research support at all TRLs.

[21] IAC R&D WG (Feb, Rec. 2): Identify a small number of application driven grand challenges to inspire innovation across the computing stack and spans fundamental materials, equipment and process R&D; design and manufacturing. The grand challenges should be at the system level, integrating hardware and software considerations, and necessarily require contributions across several layers of the compute and system hierarchy.

[22] ASIC Coalition White Paper, at 9: "For the full potential of future technologies to be reached, coordination across the "full stack" must be orchestrated…"

[23] IAC Org/PPP WG (Feb., Rec. 4-5): NSTC should partner with and be complementary to existing centers, and emphasize build-out of the ecosystem and enabling infrastructure.

In order to maintain its mission and focus within the federal government, the CRDO and NSTC should be regular participants in the National Science and Technology Council's Subcommittee on Microelectronics Leadership (SML) to ensure synergy between cross-governmental program portfolios and mechanisms for successful projects to transition through the innovation pipeline. Under the CHIPS Act, the NSTC must be aligned[24] with the National Strategy on Microelectronics Research, which was recently released by the SML.[25]

Among non-governmental operations, the NSTC should take care to create complementary facilities and operations and avoid redundancy (unless a capacity is found to be insufficient for demand). The NSTC should seek cooperative agendas with other research facilities (including in allied countries) to the maximum extent practicable. Avoiding duplicative programs and facilities will also allow companies to realize unique value from each research facility. This will stem the possibility for competition among research facilities that could result in diluting budgets or companies reallocating budget for R&D from one operation to a different one.

Companies and research entities have invested considerable time and energy in collaborating to develop documents that describe industry-wide grand challenges, key technology gaps, and research roadmaps (i.e., Semiconductor Research Corporation's Decadal Plan, Microelectronics and Advanced Packaging Technologies Roadmap, etc.). CHIPS R&D programs, including the NSTC, should maximize use of these resources to determine research agendas.

Finally, it is also important to emphasize that the NSTC is not intended to supplant proprietary R&D that companies will continue running out of their corporate facilities. Industry and the NSTC should identify working arrangements that would allow companies to run portions of an experiment at their corporate facilities and then run a different part of the experiment at an NSTC facility. This sort of working arrangement would allow NSTC to limit its capital expenditures and focus them on the elements where there is greatest need.

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[24] 15 U.S.C. § 4656(c)(2)(A)

[25] Subcommittee on Microelectronics Leadership, Committee on Homeland and National Security of the National Science and Technology Council, "National Strategy On Microelectronics Research," March 2024. Available at: https://www.whitehouse.gov/wp-content/uploads/2024/03/National-Strategy-on-Microelectronics-Research-March-2024.pdf

III. Operating Structure

Consistent with the recommendations from prior reports, including those from PCAST,[26] ASIC, and MITRE, SIA recommends that the NSTC be organized around a number of "technical centers" (TCs) focused on key technology segments (Section 3.A below). We further recommend these TCs be directed to address a set of cross-cutting R&D priorities (Section 3.B below) and strategic end markets (Section 3.C below). These cross-cutting priorities and end markets should be allocated dedicated budgets and tool time across the technical centers. This matrix structure should also employ robust mechanisms for coordination with all other CHIPS R&D programs, such as the NAPMP, to ensure the different R&D elements are working in concert with one another and driving toward common goals.

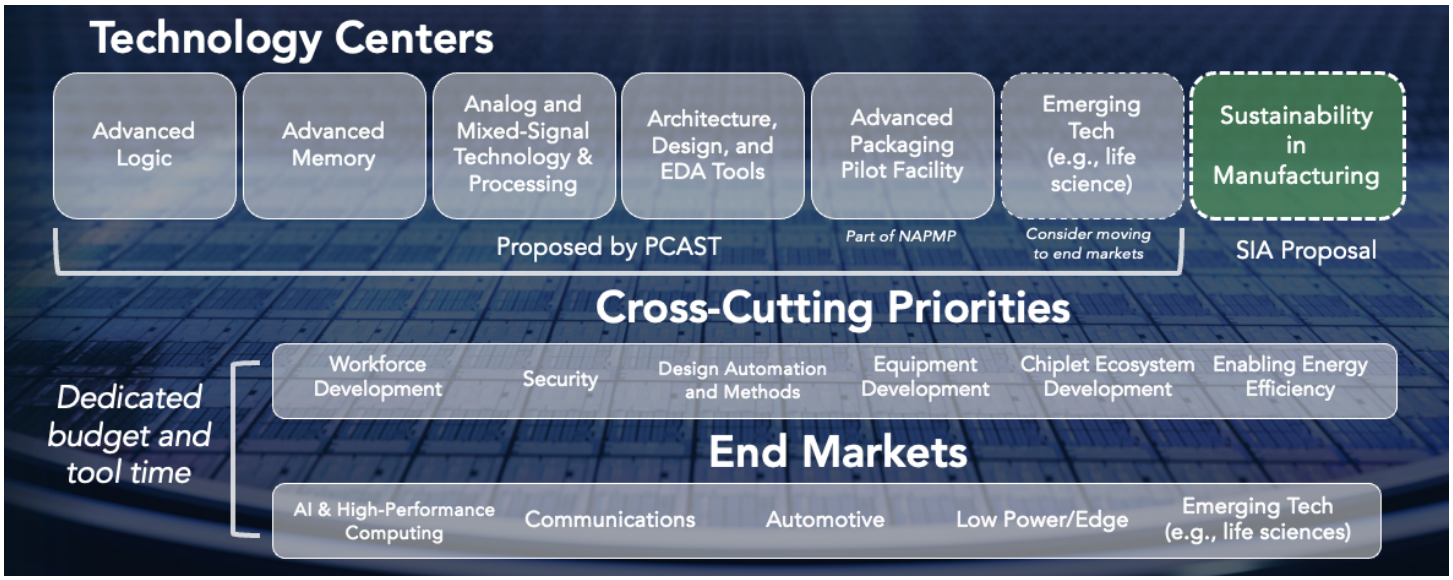

Figure 2. Proposed organizational structure of the NSTC (and the Advanced Packaging Piloting Facility), consisting of discrete technical centers along with cross-cutting and end market R&D priorities.

It is important to emphasize that the categorization within the organizational framework of "Technical Centers," "Cross-Cutting Priorities," or "End Markets" does not indicate a higher or lower level of prioritization, and progress on cross-cutting R&D priorities and translational research for end markets should be pursued just as aggressively as progress on the subject of a given technical center. Durable mechanisms should be instituted to balance research at all levels of the organizational structure.

Activities of the NSTC should be determined by boards and committees that contain significant industry representation. Members from industry should represent a broad diversity from across the semiconductor ecosystem. Moreover, in the early stages of establishing each of these

[26] PCAST Report, at 9: "…in a geographically distributed model encompassing up to six coalitions of excellence (COEs)."

programs, these advisory boards and working groups should identify critical metrics for success and build in means of tracking these throughout their programming. These advisory groups should be structured as follows:

- Each NSTC Technology Center should assemble a Technology Advisory Board (TAB) comprised of industry personnel who are subject matter experts for the purview of that TC.[27] The TAB will develop the overall strategy, research and technology, and budget priorities for their TC.
- Each cross-cutting R&D priority should have a body of experts focused on ensuring progress in that focus area to guide research directives on these categories.
- Each end market should have a body of experts focused on coordinating innovations (from across all TCs and other CRDO research programs) in that sector that are critical to national and economic security. End Market Working Groups should be established to ensure this collaboration.

A. Technical Centers

Technology development and research requires a suite of processing tools and other associated infrastructure needs, and these needs will vary by technology segment (e.g., the requirements for analog and mixed-signal research are distinct from those of advanced logic). Based on the required research infrastructure for different sectors of the semiconductor ecosystem, we recommend organizing research operations around several focused TCs that are outfitted to suit technology development for that sector. The PCAST recommended six TCs, and SIA endorses a somewhat modified proposed approach as a means of advancing innovation in key technology segments.

Given the timing and expense of greenfield construction, SIA recommends leveraging existing infrastructure to support a rapid start to NSTC and Advanced Packaging Pilot Facility (APPF) activities.[28,29] There are significant industry, academic, and other facilities and assets within the U.S. that could be marshalled for the NSTC's Technical Centers and the NAPMP's APPF. Bolstering use of these facilities will be the fastest way to start producing outputs for businesses. It will also maximize the value of appropriated CHIPS R&D funds and reduce potential for duplicative facilities.[30]

In addition to the TCs recommended by the PCAST, SIA further recommends the addition of a center on "Sustainability in Manufacturing." SIA believes it would be beneficial to establish a stand-alone center to address sustainability issues that, if left unaddressed, could prove to be

[27] MITRE (2021), at 17. PCAST, at 15
[28] ASIC Coalition White Paper, at 6: "It also must expand existing large piloting and prototype integration centers – leveraging prior investment – since entirely new centers would take years to become fully-operational – too late to impact the current battle."
[29] IAC Org/PPC WG (June, Rec. 1-3): To expedite the start-up of operations and minimize duplication, leveraging existing facilities worldwide for other critical capabilities, as well as leveraging 9902 funding to support NSTC needs.
[30] MITRE (2021), at 14. MITRE (2023), at 26.

an obstacle to technology development and prevent the industry from complying with increasingly stringent environmental requirements. The mission of this center would include the development of process gases with reduced global warming potential, chemicals with improved environmental profile (e.g., reduced bioaccumulation, persistence, and toxicity), manufacturing processes with reduced water consumption, and other priorities relating to the environmental sustainability, health and safety of the fabrication process. A dedicated center would accelerate the development and initial evaluation of more environmentally neutral processes and materials. That said, it is also important to note that after initial development work, other technical centers may play a critical role in integrating the outputs of this sustainability work.

Natcast will be responsible for establishing all of these TCs, with the exception of the Advanced Packaging Piloting Facility, which will be developed by the NAPMP. While advanced packaging has its own set of R&D priorities, it is also the platform on which heterogeneous technologies are brought together to execute complex workloads. Coordination and collaboration between the NSTC and the NAPMP are essential to ensure diverse technology advancement enabled by advanced packaging. We recommend that Natcast also acts as the operator of the Advanced Packaging Piloting Facility to facilitate integration with NSTC programs across TCs.[31,32]

B. Cross-Cutting R&D Priorities

In addition to the TCs organized around specific technology segments, collaboration between different TCs is important to generate cross-functional solutions rather than siloed point solutions. Put differently, some technology developments (i.e., security) require a broader set of stakeholders from all across the ecosystem. We recommend that Natcast establish a structure for cross-TC technology priority alignment on R&D objectives that cut across multiple sectors of the industry. Each cross-cutting working group should rigorously pursue progress on these priorities within their domain space. Accordingly, resources, tool time, and other assets should be allocated to address important cross-cutting priorities. For example, workforce development and the pursuit of more energy efficient devices/architectures and secure designs should be engaged at all technical centers. In alignment with PCAST, SIA recommends the following cross-cutting priorities be integrated into the work of the TCs:

- ***Workforce Development***: Maximum access to facilities will be critical to training the workforce needed for the industry, and this can effectively serve as a form of "on-the-job" training. Additionally, certain sectors of the industry entail skills or knowledge base that are distinct from other parts of the industry. Incorporating workforce development across all TCs will ensure that all sectors are able to develop workforce suited to their

[31] ASIC Coalition White Paper, at 5: "Co-location of NAPMP and NSTC technical activity will accelerate innovation across the full technology stack."
[32] PCAST Report, at 14: "The Secretary of Commerce should merge the governance of the NSTC and the NAPMP to increase the synergy of investments and reduce the potential for duplication of infrastructure."

needs.[33] CRDO and Natcast have already indicated intent to establish a Semiconductor Workforce Center of Excellence (CoE) under the NSTC,[34] and we believe a decentralized approach to establishing this CoE will maximize opportunities for workforce development. Some efforts of the CoE would benefit from a coordinated approach, such as efforts to standardize curricula, establish a clearinghouse of educational resources, share best practices, and promote industry awareness to students and workers.

- ***Security***: Systems are only as secure as their least secure component, and as the industry moves toward heterogeneous integration and chiplet ecosystems, it is essential to ensure that security innovation is a priority across all TCs.

- ***Energy Efficiency***: The SRC Decadal Plan[35] highlighted the pressing need for devices and architectures with significantly improved energy efficiency to meet growing societal data needs and corresponding demand for computing and storage. Accordingly, energy efficiency should be pursued at the device level, the architecture/system level, the tool module level, and at the fab level.[36,37]

- ***Chiplet Ecosystem Development***: The industry's move toward heterogeneous integration and chiplet ecosystems will involve technology segments across the semiconductor industry.[38] Diverse sets of components must be interoperable with one another, and technology developments in one group of chiplets will likely inform developments for other chiplet providers. Given the wide reach of this move in the industry, it is important that chiplet ecosystem development occur across all TCs.

- ***Design Automation and Methods***: Design automation software must be optimized for each different industry segment, and so it is important that this takes place across all TCs.

- ***Equipment Development***: Equipment providers develop specialized tooling for all sectors of the industry—each with different tooling priorities to enable their technology

[33] CRDO Vision Document, at 17.
[34] CHIPS R&D Office, "Building the U.S. Semiconductor Workforce: Progress Report," Nov. 2023. Available at: https://www.nist.gov/system/files/documents/2023/11/03/Building-the-US-Semiconductor-Workforce.pdf
[35] Semiconductor Research Corporation "Decadal Plan for Semiconductors", Chapter 5: New Compute Trajectories for Energy-Efficient Computing.
[36] IAC R&D WG (Feb., Rec. 2-1): "Improve computing energy efficiency by 1,000X in a decade including leveraging domain specific accelerators and architectures, and innovation in materials, process and equipment technologies."
IAC R&D WG (Feb., Rec. 2-2): "Develop and implement next-generation semiconductor manufacturing that is 10X more capital and human resource efficient and achieve net zero emissions with minimum waste and demonstrated sustainable materials in the next decade."
IAC R&D WG (June, Rec. 7): "Set grand challenges of achieving 10x increase in productivity and 10x decrease in environmental/energy footprint for mainstream advanced packaging capabilities, including eco-benign semiconductor manufacturing."
[37] PCAST, at 24.
[38] IAC R&D WG (Feb., Rec. 1-3): "Establish chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging."

roadmaps. Ensuring equipment developers work across TCs will help ensure that their next generations of products are most competitive in domestic and global markets for the most leading-edge technologies.

To ensure these cross-cutting objectives are adequately prioritized and secure the resources needed to ensure progress in these areas, SIA recommends they should be given dedicated budget and an allocation of access to facilities or tool time at technical centers to conduct research within their domain. There should also be a body of experts empowered to set the direction within each of these cross-cutting priorities and deploy initiatives at technical centers. Without mechanisms such as these in place—i.e., if technical center technology advisory boards are charged with also managing cross-cutting R&D objectives—there is risk that these cross-cutting R&D priorities may be viewed as secondary objectives. For example, projects aimed at energy efficiency and sustainability may be found less meritorious than projects that pursue performance improvements. Or, access to factory tooling at a TC could be awarded to projects within the direct purview of that TC to the exclusion of projects aimed at a security objectives.

C. Prioritization of Key End Markets

Consistent with the goals of the CHIPS Act, the technology centers should also conduct research and prototyping focused on end markets that are of strategic importance for national and economic security. For example, centers should develop robust portfolios for innovations in advanced communications, high-performance computing (HPC) and artificial intelligence (AI), automotive, low-power/edge processing, and emerging technologies (e.g., life science). These activities would bring together the subset of players from across the ecosystem whose products will ultimately be packaged into an integrated solution. For instance, a working group on HPC and AI would bring together advanced logic, memory, and advanced packaging providers, among others.

Under these working groups, a diversity of businesses and NSTC TCs would pursue development in concert, facilitating co-design and full-stack innovations, which many in the

industry affirm as critical for rapid advancement as innovation broadens well beyond scaling. This organizational structure may also lend itself to more focused sets of investments being made to drive advancement in a particular market segment.

IV. Participation Structure

A. Eligible Entities

For any participation model, SIA recommends that eligibility for funding under the NSTC extend to academic institutions (i.e., universities, national laboratories, etc.), non-governmental research organizations, shared user facilities, start-ups, small businesses, and larger companies.

CRDO indicates that participation in the NSTC will include both U.S. companies and research entities as well as international companies and research entities from allied countries.[39] The CRDO also expects that most NSTC-funded work will take place at facilities within the U.S.[40] SIA supports this approach.

B. Access Models

The science and technology community employs a range of models to govern access to shared research infrastructure and collaborative research. Each of these models will be best suited to a particular user of the NSTC, and so SIA recommends a combination of participation options in order to provide appropriate support for startups, small businesses, academic researchers, large corporations, government researchers, and other stakeholders.

- *Membership:* One structure that is used by some cooperative R&D organizations involves companies buying into a membership (the dues for which create some portion of the operating and/or research budget). Membership is designed to allow participation in collaborative research projects. Members should be granted access to non-exclusive, royalty free licenses for research and commercial products for intellectual property that comes out of projects in which they participate.

- *User Facility Model:* Many government-owned research facilities grant free access to researchers who submit proposals that are subsequently selected through a competitive peer review process. This structure could be adopted by the NSTC and the APPF to grant non-profit and academic users access to their facilities for projects that generally support the mission of the NSTC or APPF.

- *Fee for Access:* To maximize use of NSTC/APPF infrastructure and proffer an additional revenue stream, companies that wish to execute proprietary research at the NSTC or APPF ought to have access to facilities, equipment, and personnel. Use of these

[39] 15 U.S.C. §4657 ("None of the funds authorized to be appropriated to carry out this chapter may be provided to a foreign entity of concern.") Therefore, entities from "countries of concern" should not be eligible to participate in the CHIPS R&D programs.
[40] CRDO Vision Document, at 19.

resources should come at a fair and reasonable cost to those companies. Further, use of these resources for proprietary research purposes should not interrupt or delay CHIPS R&D efforts.

C. Research Projects

For NSTC members, there are two primary models for initiating research—requests for proposals (RFPs) and project co-funding—each with benefits and potential drawbacks. SIA recommends the NSTC deploy a combination of both approaches to meet the needs of various stakeholders in the semiconductor industry.

Requests for Proposals (RFPs): Many Federal research programs assemble program advisory committees with a remit to define a research portfolio ahead of funding opportunities. Funding opportunities are subsequently written in accordance with these advisory committee recommendations. Once proposals are submitted, a separate committee of subject matter experts evaluates these proposals against a rubric and scoring criteria to determine a subset most meritorious of funding. Importantly, these review committees are comprised of "peers," so that they may be reviewed by those with the greatest ability to scrutinize submissions. For programs that are aimed at piloting, prototyping, and industrial scaling—such as the NSTC and the NAPMP—it is important that both program advisory committees and peer reviewers consist of both upstream academic researchers and downstream industry users with the greatest knowledge of design, processing operations, business models/economics, and emerging state-of-the-art. The combination of these elements will ensure the NSTC and NAPMP remain focused on industry priorities and commercially relevant timing.

- ***Benefits:*** Peer review is a widely accepted and reputable practice for evaluation. Assuming multi-disciplinary teams of true "peers" are identified to assess proposals, peer review is viewed as objective and a fair means of assessment.

- ***Potential Drawbacks:*** Given the expansive range of eligible entities SIA is recommending, it will be challenging to assemble truly representative peer review committees. Further, it may be difficult to avoid scenarios in which competitor companies may be in a position to review one another's proposals. In these instances, it will be essential to utilize recusal mechanisms to maintain the integrity of the process.

Project Co-funding: In a project co-funding mechanism, the NSTC and APPF (under guidance by an industry-informed advisory committee) could announce a project scope, and all companies with interest in that project space would have an option to "buy in" to the project. In doing so, their dollars would support execution of the project both within NSTC facilities, and also at other facilities, such as universities or national laboratories. Within this model, all entities that buy into a project would receive non-exclusive, royalty free access for commercial products to intellectual property that results from the project.

- ***Benefits:*** This model maintains an industry focus due to the fact that companies have the opportunity to support only the projects that are within their interests. Projects with broad industry appeal will receive greater total funding than projects with minimal industry appeal.
- ***Potential Drawbacks:*** This model has a risk of deprioritizing and underfunding R&D in support of niche segments of the semiconductor ecosystem. Additionally, this model risks prioritizing projects that promise nearer term returns. The NSTC ought to maintain a balanced portfolio of near-term prototyping projects and also more speculative, bigger bets—not all of which may be commercialized.

Ultimately, the NSTC should adopt a combination of both of these paradigms. Project co-funding is a model that creates a sustainable revenue stream beyond the 5-year CHIPS Act appropriations, and it will help keep the NSTC focused on industry priorities. Use of RFPs will still be needed for new and smaller segments of the ecosystem that do not have a broad industry presence, and it will likely be most impactful for small and start-up companies that do not always have adequate resources to contribute to co-funded projects. For some awards made to smaller companies following an RFP, NSTC could even authorize awardees to apply a portion of their award to support a co-funded project.

D. Ensuring Long-Term Funding for the NSTC

The funds allocated to the NSTC and other elements of the CHIPS R&D Program are among the most formidable investments the federal government has ever made in the nation's semiconductor R&D leadership. However, the NSTC is intended to persist for years and decades—well beyond the five-year lifetime of the initial $5 billion of CHIPS R&D funds. A long-term challenge will be the development of a sustainable source of funding to keep the NSTC successful beyond its initial five years. Therefore, the NSTC and CHIPS R&D programs must crowd in private sector R&D investment through an operating mechanism, research agenda, and scope of work that companies will find value in so that they are compelled to commit their own resources. Aligning with industry innovation priorities and roadmaps will support greater company buy-in and increasing their willingness provide resources, such as participation fees, cost shares, personnel, equipment, and other in-kind contributions.

Accordingly, Natcast and NSTC executive leadership should aim to establish operating models that will be self-sufficient even once the initial funds are exhausted.[41] This is likely to include significant supports to establish and adapt initial research infrastructure at the outset. The NSTC operating model and funding structure should be evaluated in an ongoing manner once participants have had time to assess the value of the organization's early efforts. In the meantime, it is likely that the CHIPS R&D programs would benefit from renewed Congressional

[41] IAC Org/PPP WG (Feb., Rec. 4-2): The NSTC should develop a sustainable business model, with increased funding by industry over time. Government funding should provide risk capital to facilitate broad participation of firms and research institutions of all sizes and means.

appropriations beyond this initial 5-year period, and the NSTC should seek to establish early "wins" in the next three years to create a strong case for continued federal support.

V. Policy Considerations

The CHIPS Act sets forth requirements for (1) the domestic production of the results from research programs and (2) the protection of intellectual property derived from these programs. The CHIPS Act states: "The head of any executive agency receiving funding under this section shall develop policies to require domestic production, to the extent possible, for any intellectual property resulting from microelectronics research and development conducted as a result of such funding and domestic control requirements to protect any such intellectual property from foreign adversaries."[42] SIA supports aligning such policies with existing, industry-accepted practices (including from other government research agencies such as DARPA, SBIR, Tech Hubs, etc.) that promote national security and ensure companies can retain and commercialize their intellectual property.

A. Domestic Production

Incentivizing the domestic production in the U.S. of new technologies developed with government funding is appropriate and consistent with the overall goals of the CHIPS Act, and participants engaged in the CHIPS research programs should commit to commercializing these innovations in the U.S to the extent practicable. At the same time, however, overly broad or exclusive requirements would be problematic and could dissuade corporate R&D involvement. At high-volume commercial fabs, semiconductor companies typically maintain "copy exactly" practices which allow them to achieve high yields and efficiencies in facilities around the world while avoiding quality incursions from varied processes. Requiring research participants to produce new technologies exclusively in the U.S. could require companies to outfit fabs differently country-by-country. Further, for innovations on existing technologies that are exclusively manufactured abroad, domestic production may not be feasible to any extent. Accordingly, any domestic production requirement should also allow participating companies to deploy new technologies generated from the CHIPS programs to their manufacturing sites worldwide (excluding countries of concern).

Consistent with the CHIPS Act and Executive Order 14104,[43] the NAPMP's first notice of funding opportunity (NOFO)[44] on R&D for advanced packaging materials and substrates requires applicants to provide a Commercial Viability and Domestic Production Plan (CVDP) that includes "a realistic business model for the funded innovations, […] a technology transition plan, and […] pathways to benefitting national and economic security, such as through the

[42] 15 U.S.C. § 4656(g)

[43] White House, "Executive Order on Federal Research and Development in Support of Domestic Manufacturing and United States Jobs," July 2023. Available at: https://www.federalregister.gov/documents/2023/08/02/2023-16636/federal-research-and-development-in-support-of-domestic-manufacturing-and-united-states-jobs

[44] Notice of Funding Opportunity, National Advanced Packaging Manufacturing Program, Materials & Substrates (NAPMP NOFO). Available at: https://www.nist.gov/chips/notice-funding-opportunity-chips-national-advanced-packaging-manufacturing-program-napmp

domestic availability of the technology and successful adoption by commercial or defense partners." Additionally, the NOFO states that "CHIPS R&D does not require the covered 'production' to occur exclusively within the United States," but applicants must explain why such domestic production may not be possible.

SIA supports this approach and encourages NSTC to facilitate responsible domestic production policies that enable integrating innovations into global operations.

B. Disclosure of National Security Risks and Research Security

Pursuant to the CHIPS statute requirement to impose "domestic control requirements to protect any such intellectual property from foreign adversaries," CRDO has identified the security of research conducted under the CHIPS programs as being a top priority.

To address these concerns, participants in these programs should be subject to rigorous disclosure requirements pertaining to personnel with access to information on CHIPS research projects. As set forth in applicable guidance documents governing research security (e.g., NSPM-33, NIST IR 8484), participating companies should disclose the citizenship, academic and work experience, and other relevant background information of those with access to research projects. The first NAPMP NOFO indicates intent to align with these guidance documents as sufficient for compliance with the research security requirements, and applicants must submit a research security plan "describing internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity."[45] The NAPMP appears to afford funding recipients sufficient time to implement the requisite guidance. The NSTC and other CHIPS R&D programs should likewise ensure funding recipients and project participants have sufficient time to implement necessary research security procedures.

C. IP Policies

Policies relating to IP will likely have a significant impact on the overall success of the NSTC. Fair and equitable IP policies can facilitate company involvement and help drive the NSTC as a center of innovation and its overall future success. At the same time, misplaced IP policies pose the risk of disincentivizing industry players from participating in the NSTC and diminish its ability to achieve its goals.

The NSTC should look to successful models employed by other programs. As a starting point, the NSTC should adopt IP management practices that closely resemble research entities with which semiconductor companies already have existing relationships, such as SRC and imec.[46]

[45] NAPMP NOFO, at 50

[46] PCAST Report, at 16: "Best practices from established research models, such as Semiconductor Research Corporation and Europe's Interuniversity Microelectronics Centre, should be applied in the final IP framework and security definition."

Under this model, companies participating in a given project should be granted non-exclusive, royalty free perpetual licenses for patented.[47] Similar to the approach taken for NASA's Commercial Orbital Transportation Services (COTS) program, NSTC should allow "participating companies to retain the IP they [create] to avoid potentially chilling effects on innovation and ensure that companies [can] serve markets effectively."[48] The research programs should employ nondisclosure agreements (NDAs) to protect the IP that a company may bring to the research endeavor. In addition, EO 14104, requires federal agencies and departments to consider whether "exceptional circumstances" exist under Bayh-Dole such that the federal government may retain title to IP / "subject inventions" developed with Federal funds. As described above, such requirements would be of great concern and likely disincentivize participation in NSTC programs.

D. Reducing Administrative Burdens

Different processes for the NSTC and other CHIPS R&D programs (e.g., NAPMP, etc.) will create administrative burden for industry partners. To the extent feasible, both programs should draw from practices in other collaborative research operations and adopt consistent processes and administrative requirements to facilitate increased industry participation, transparency, and trust.

[47] PCAST Report, at 17: "We recommend that all IP developed with funding by a COE (i.e., membership fees, government funding, state or university funding) be licensed to COE members in good standing as a non-exclusive, royalty-free perpetual license for research and commercial products. Ownership of IP will be retained by the inventors or inventors' respective institutions. Any pre-existing IP which is necessary to practice the IP created by the NSTC will be identified up front by the owner of the preexisting IP. If the NSTC chooses to use this pre-existing IP, it should be licensed to members on the best terms possible."

[48] MITRE (2021), at 20.

IAC Org/PPC WG (June, Rec. 6-1.1): The primary goals of the NSTC IP strategy should be to enable access to NSTC research while protecting member IP.

IAC Org/PPC WG (June, Rec. 6-1.2): Multi-tiered IP governance framework designed to foster collaborations ranging from basic research to advanced proprietary prototyping work.

IAC Org/PPC WG (June, Rec. 6-2): Mode I. Research data and underpinnings mandated to become feeder for national data sets; Mode II & III. Enhance security & privacy of sharing options for proprietary work + standardization of sharing mechanisms

Conclusion

These recommendations are intended to help move the NSTC forward and achieve its mission of advancing U.S. semiconductor leadership and technology innovation in support of national goals and domestic industry. This document should be used to guide the evolution of the CHIPS R&D programs, including the NSTC, and present CHIPS R&D leadership with important industry insights and priorities. SIA looks forward to ongoing engagement with Natcast, CRDO, and other federal research agencies to establish an impactful and successful semiconductor R&D ecosystem of the future.