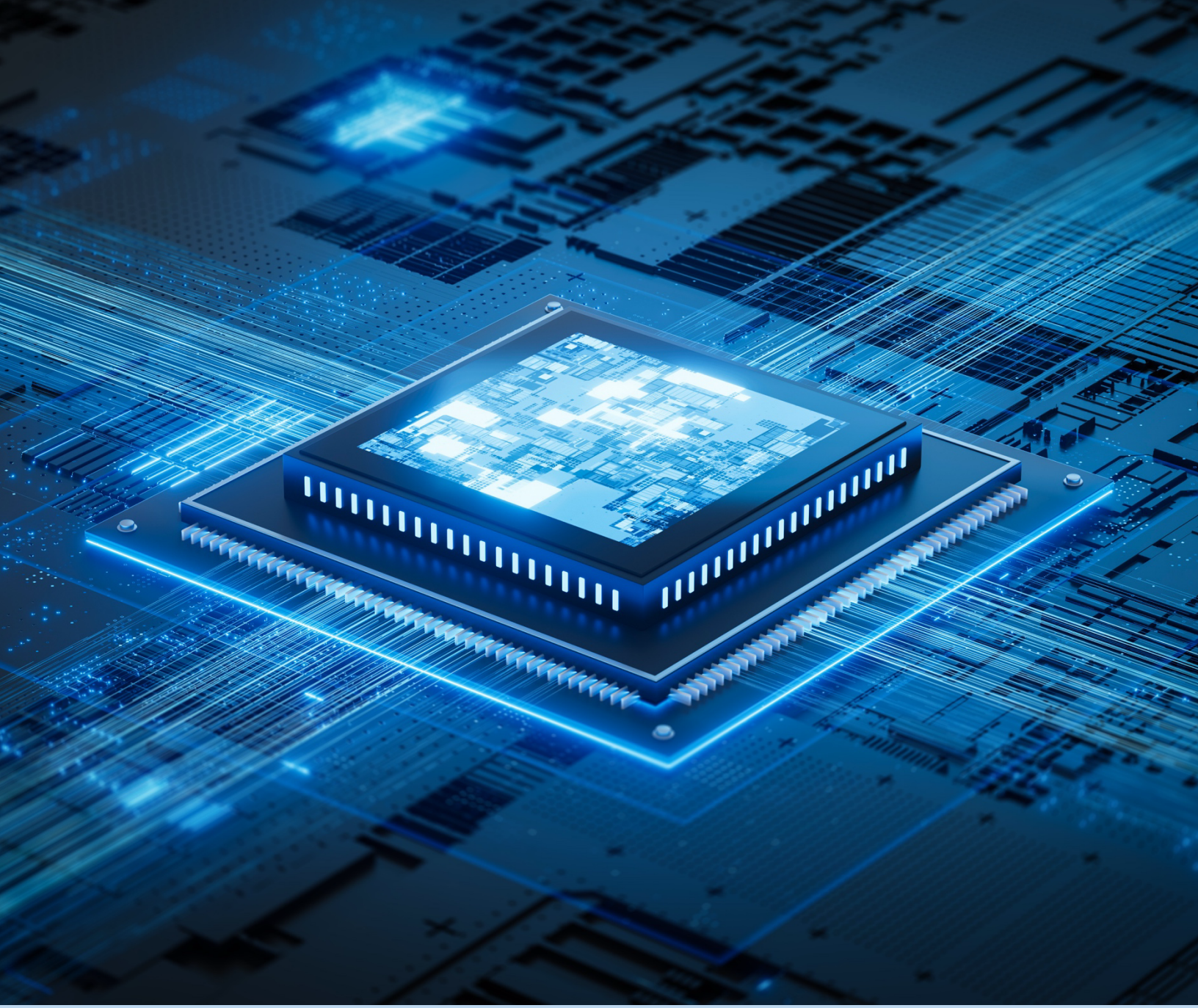


SEMICONDUCTOR R&D PROGRAMS: Essential Innovation for U.S. Technology Leadership

June 2025

SEMICONDUCTOR INDUSTRY ASSOCIATION

CONTENTS

Introduction

U.S. leadership in semiconductor technology is vital to economy and national security.

To win the competition for technology leadership—as well as for critical industries enabled by semiconductors, such as artificial intelligence, high performance computing, advanced communications, quantum, energy, defense, medical technology, and transportation—the U.S. must resecure its role as the epicenter of semiconductor innovation. Federal research programs established through the Fiscal Year 2021 National Defense Authorization Act and funded under the CHIPS and Science Act are working to meet the changing nature of the industry, its technologies, and most importantly how it operationalizes innovation. These investments are beginning to address specific gaps in American semiconductor competitiveness, resilience, and supply chain security. And, they are being made at a critical time in which dramatic industry changes are renegotiating the geography of innovation.

Key Takeaways

1. To win the global competition for technology leadership, the U.S. must maintain its role as the leader in semiconductor innovation.

2. The CHIPS R&D Programs have the potential to deliver on an aggressive, comprehensive, and industry-aligned strategy that reflects the newest innovation trajectories in the industry.

3. These programs have made progress in deploying their resources to award recipients, and several of those projects are now underway. The programs have started to develop needed infrastructure, with final contracts in place for smaller sites and larger facilities under contract negotiation. More progress is needed to define the research agenda, consistent with industry priorities and the needs of high volume manufacturing, and begin implementation of this agenda.

4. As these programs continue to be implemented they must be sustained at the appropriated levels and maintain their commitment to industry-informed programming.

R&D Investments to Meet the Rising Competition for Innovation Leadership

In recent years, governments around the world—from both allied and adversarial nations alike—have competed fiercely to secure advanced semiconductor R&D, understanding that where cutting-edge research takes place defines where the most cutting-edge businesses will grow. For instance, in 2025 alone, the People's Republic of China (PRC) is investing a staggering $55 billion on research in semiconductors, artificial intelligence, and quantum information sciences.[1] Federally funded semiconductor research programs through the CHIPS R&D Office (CRDO) hold the promise to deliver on an ambitious, comprehensive, and industry-aligned strategy to ensure the most cutting-edge semiconductor technologies are developed in America, made in America, and benefit the American economy. And the CRDO programs are democratizing access to these innovation assets that would not be available without public funds. The CRDO programs reviewed in this paper are the following:

National Advanced Packaging Manufacturing Program (NAPMP)	**National Semiconductor Technology Center (NSTC)**	**Semiconductor Manufacturing and Adv. Research with Twins USA (SMART USA) Institute**	**CHIPS Metrology Program**

R&D Investments to Sustain U.S. Manufacturing Leadership Long-term

The CHIPS R&D Programs are an essential complement to the $540 billion of investments being made in domestic semiconductor manufacturing capacity.[2] Product cycles in the industry have historically progressed on a two-year cadence. However, as the industry transitions to novel innovation strategies, product cycles are accelerating. The U.S. must win the global competition for the heart of semiconductor innovation to keep these domestic facilities at the leading-edge long term. Moreover, the industry-driven nature of the CRDO programs is intended to support continued revitalization of the U.S. semiconductor supply chain, consistent with Administration priorities to enhance America's competitiveness in innovation and manufacturing. And, unlike conventional government funding programs that seek to engage early technologies, the CRDO programs have a unique mission to activate technologies for high-volume manufacturing in the near term.

[1] Tom's Hardware, "China to spend $55 billion on R&D in 2025 — Semiconductor, AI and quantum computing fields to benefit," March 2025. https://www.tomshardware.com/tech-industry/china-to-spend-usd55-billion-on-r-and-d-in-2025-semiconductor-ai-and-quantum-computing-fields-to-benefit

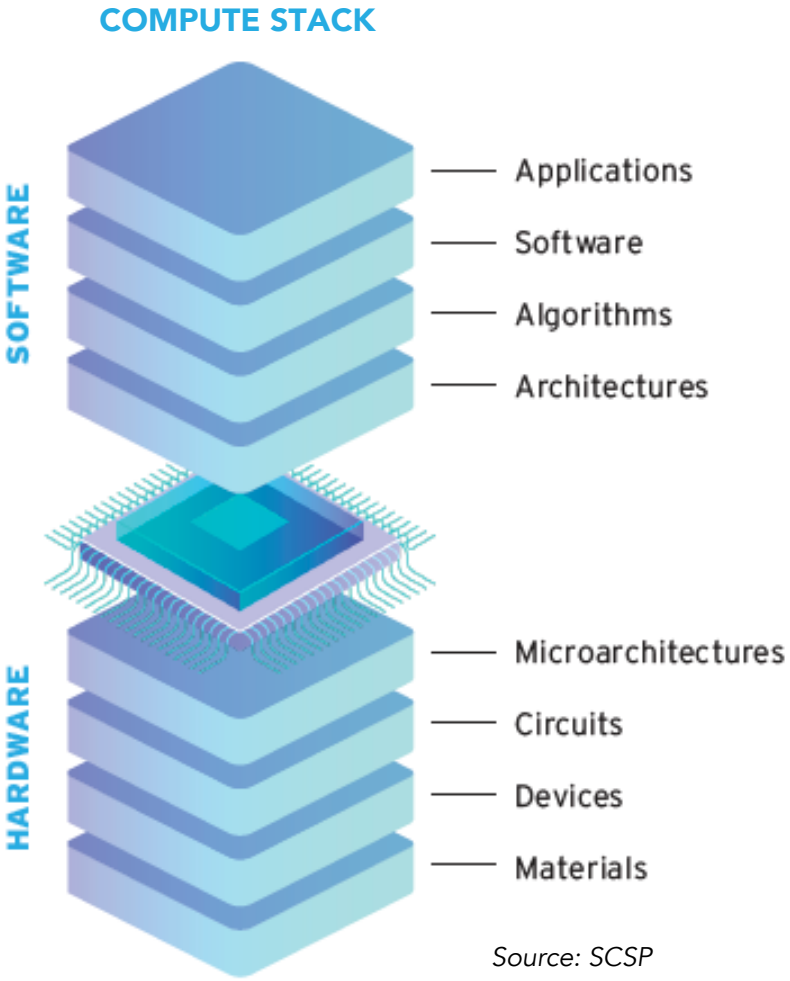
[2] Semiconductor Industry Association, "America's Chip Resurgence: Over $540 Billion in Semiconductor Supply Chain Investments," updated March 2025. https://www.semiconductors.org/chip-supply-chain-investments/

I. Importance of Semiconductor Research Programs

As these research programs continue to ramp up, they hold potential to meet the innovation challenges facing the semiconductor industry and drive advances across the compute stack.

The Evolving Dynamic of Moore's Law and Beyond

New and powerful avenues for semiconductor innovation have emerged in recent years, requiring new approaches to collaboration and technology development. In prior decades, advancing compute performance was achieved primarily through "scaling" – miniaturizing features on a chip to accommodate more transistors onto a single piece of silicon. Accordingly, "Moore's Law" predicted that the number of transistors on a chip will double every two years, accompanied by a decrease in cost. This model of innovation yielded remarkable benefits for decades, and the march of Moore's Law continues to this day. However, novel innovation frontiers hold immense promise for dramatic leaps in compute performance for advanced logic, memory, and analog. These new methods push beyond Moore's Law and appeal to "full stack" strategies – innovating across software, materials, design, architectures, and packaging – and demand collaboration throughout the value chain. Meanwhile, for an increasing number of applications (e.g., certain end uses in industrial, medical devices, automotive, etc.), performance is not measured solely by the number of transistors; instead, new solutions drive new value propositions for new end markets, such as ultra-low power consumption, high bandwidth, the ability to operate at higher voltages regimes, greater stability at higher temperatures, or lower latency.



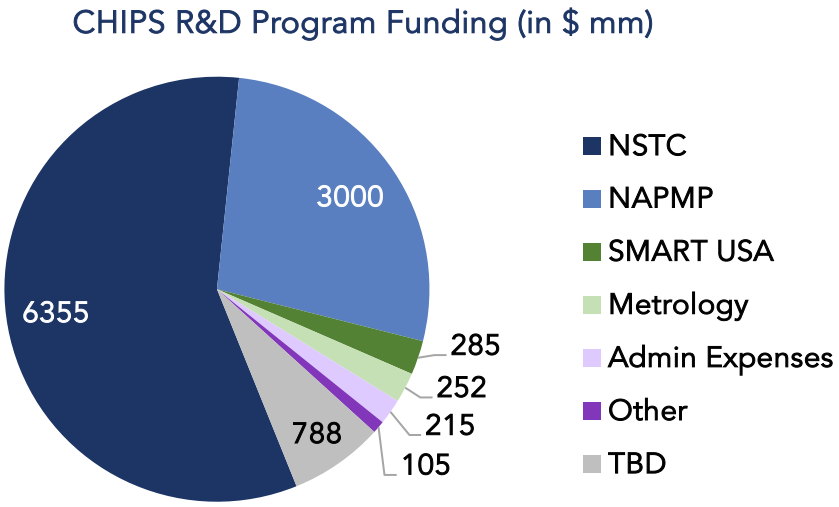
Source: SCSP

Federal Investments to Capture Novel Innovation

New demands from customers are re-orienting and expanding how the semiconductor industry innovates, and the CHIPS R&D Programs are poised to provide the infrastructure and collaborative research platform essential to ensuring the American semiconductor ecosystem remains ahead of our global competitors across these various innovation dimensions.

To supplement federally backed research programs, these new programs fill a void in the U.S. semiconductor ecosystem by allowing fierce industry competitors to work in a pre-competitive and collaborative space to tackle important innovation needs.

The framework of these programs, guided by industry leaders[3] and technology roadmaps, position the NAPMP, NSTC, SMART USA, and Metrology to deliver outsized and rapid impact for the nation while ensuring American dominance against global competitors in the technology race of the future. Approximate funding for these programs totals $11 billion over five years is allocated as follows:[4]



To effectively compete in the global semiconductor innovation race, these programs must be sustained at the appropriated levels. Maintaining funding at appropriated levels will ensure these programs have the resources to launch their work and build strong connections with industry partners.

[3] The Department of Commerce Industrial Advisory Committee for these R&D programs is comprised of some of the industry's most prominent technology leaders, and the NSTC and SMART USA will feature industry-led technology advisory boards, ensuring that commercial relevance is a key priority.

[4] U.S. Department of Commerce Office of Inspector General, "Commerce CHIPS Act Programs Status Report," June 2025. https://www.oig.doc.gov/wp-content/OIGPublications/OIG-25-021-I.pdf

CHIPS R&D Programs Overview

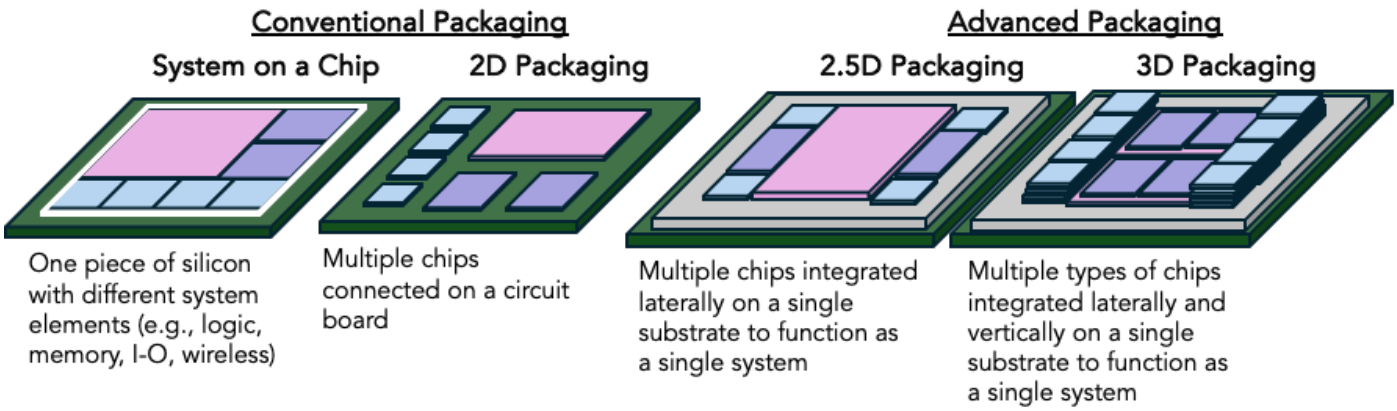
The four programs administered through the Department of Commerce are aimed at meeting the evolving technology development needs of the semiconductor industry in the U.S. The programs have been compiled with industry input, and ongoing insights from industry are essential to ensure these programs remain most relevant to industry partners. These programs are summarized below, and more detail follows in the rest of this report.

	Overview	R&D Focus and Facilities
National Advanced Packaging Manufacturing Program (NAPMP)	Support advanced compute for artificial intelligence, high-performance compute, and niche systems; the NAPMP is deploying a comprehensive strategy to secure this emerging and high-value-add sector in the U.S.	**6 research topics:** • Awards Announced: materials/substrates • Final Applications Submitted: photonics & connectors, co-design & EDA, chiplet ecosystem, equipment/tools/processes, power delivery & thermal management **Advanced Packaging and Piloting Facility:** Natcast contracted as operator of a fully-integrated advanced-packaging pilot line
National Semiconductor Technology Center (NSTC) *Operator: Natcast*	Support transition of early-stage research to commercially relevant technologies and build full-stack innovation programs for stakeholders across the value chain. Support workforce development.	**Collaborative facilities to expand access to valuable innovation assets:** • Piloting and Prototyping Facility • EUV Accelerator • Design and Collaboration Facility
Semiconductor Manufacturing and Advanced Research with Twins USA (SMART USA) Institute	Develop digital twins as an innovation tool to simulate and optimize process developments without the time and expense of physical trials. SMART USA aims to reduce chip-development and manufacturing cost by 40% and development-cycle times by 35%.	**Key objectives:** • Create the "Digital backbone" • Establish industry-wide standards • Build a network of shared facilities • Launch a digital marketplace • Expand the digital-twins-capable workforce
Metrology Program	Driving the industry's ability to make critical measurements for process verification and failure analysis.	**Program features:** • Hardware programs at NIST facilities • Digital assets including data sets, references, and software libraries

II. NAPMP: Innovating Through Advanced Packaging Technologies

Advanced packaging[5] is a novel semiconductor technology that promises to accelerate capabilities of the most powerful chips for artificial intelligence and high-performance computing (AI and HPC). It will also facilitate more rapid and cost-efficient design and manufacturing of customizable systems for high-mix, low-volume markets—such as for defense applications critical to national security. In the past, state-of-the-art chip performance was limited to what features could be fabricated on a single, two-dimensional silicon wafer (i.e., "system-on-chip," SOC).

Now, advanced packaging enables components of a chip system to be manufactured separately and then subsequently incorporated together into a single package, ultimately increasing the total silicon content (and hence, computing power) of the entire chip. Whereas conventional packaging does not directly impact performance of a chip, advanced packaging is now a critical means of driving compute performance. Moreover, by manufacturing different components of a chip separately, fabs are able to enhance their profitability by simplifying their manufacturing flows, increasing factory throughput and yields, and enabling more continuous innovations and product improvements since all components of a system no longer need to be designed and manufactured together.



While the earliest advanced packaging technologies are now on commercial markets, much of advanced packaging's potential remains on the horizon—and global leadership for this critical sector is up for grabs. The U.S. currently faces a critical shortfall in packaging supply chain,

[5] Unlike packaging of most goods to protect them during shipping, packaging in the semiconductor industry refers to the process of encasing a fully processed wafer that has been cut into individual "die." This casing must protect the die from the external environment and create reliable electrical contacts in and out of the package. In the past, conventional packaging has been a comparatively low value-add segment of the semiconductor value chain that is not directly related to the overall performance of a chip, but advanced packaging is a sophisticated, high-value source of innovation.

housing only 4% of global capacity in assembly, test, and packaging.[6] Given the imminent rise in the role of advanced packaging to drive compute performance, this is an opportune and strategic time for the country to pursue advanced packaging and intercept the growing and high value-add sector to seed capacity in the U.S.

Congress recognized the importance of innovation in semiconductor packaging and established the NAPMP "to strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem" (15 U.S.C. 4656(d)). The program is led by NIST and targets packaging applications most critical to public interest, namely AI and HPC. The NAPMP is coordinating broadly with other programs (including DARPA's Next Generation Microelectronics Manufacturing program[7]) to make investments in the semiconductor and AI ecosystems.

The mission of the NAPMP is to develop a holistic strategy[8] to solve these pressing challenges and enable a thriving domestic advanced packaging industry. The NAPMP strategy is built around six identified research areas:

1. Materials and Substrates
2. Equipment, Tools, and Processes
3. Power Delivery, Thermal Management
4. Photonics and Connectors
5. Co-design, EDA, and
6. Chiplet Ecosystem

Descriptions of the six R&D priority areas and their importance to semiconductor innovation are found in Appendix I. As of June 2025, the NAPMP has finalized $300 million in awards for its first R&D funding opportunity, focused on materials and substrates, in addition to a $1.1 billion contract to establish the program's flagship Advanced Packaging Piloting Facility (APPF), which will be co-located and operated in conjunction with the NSTC piloting facility in Arizona. Industry is also eagerly awaiting decisions on the funding opportunity for the five additional R&D initiatives, but final awards, valued at $1.6 billion in total, have not yet been announced.

The APPF will invest in an integrated manufacturing advanced packaging process flow so that new technologies may be proved out at commercially relevant packaging scales. Proving the viability of innovations in this facility will considerably derisk technologies as they are developed and enable more efficient integration into commercial advanced packaging operations. As the APPF plans develop, ongoing collaboration with industry is needed to ensure the facility succeeds in establishing a robust U.S. advanced packaging sector.

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[6] Semiconductor Industry Association / Boston Consulting Group, "Emerging Resilience in the Semiconductor Supply Chain," May 2024. https://www.semiconductors.org/emerging-resilience-in-the-semiconductor-supply-chain/

[7] DARPA's Next Generation Microelectronics Manufacturing (NGMM) program is also developing advanced packaging technologies, but whereas the NAPMP focuses on developing advanced packaging for large compute workload applications like AI and HPC, NGMM is focused on incorporation of mixed materials (i.e., silicon, wide bandgap semiconductors, diverse node sizes, etc.) into a common package for higher mix, lower volume end markets like the defense.

[8] CHIPS R&D Office, "The Vision for the NAPMP," Nov. 2023. https://www.nist.gov/system/files/documents/2023/11/19/NAPMP-Vision-Paper-20231120.pdf

III. NSTC: Innovating the Full Semiconductor Technology Stack

Innovation in the semiconductor industry is an increasingly collaborative venture, and the NSTC aims to establish a long-term R&D resource for the entire U.S. semiconductor ecosystem to enable broad success domestically for established industry players, start-ups, and academia. For decades, computer hardware innovation and computer software innovation operated in relatively independent loops. Hardware providers turned out more powerful processors by incorporating more transistors, and software providers wrote programs to execute the computing workloads of their customers.

Today, the industry is relying heavily on new "full stack" solutions to better tailor hardware and software to one another to ultimately deliver integrated systems with greater performance and efficiency. This innovation strategy is proving effective, but it requires an elevated level of collaboration between players through the full compute stack and the full value chain. Other regions have invested heavily in national semiconductor research consortia to facilitate this innovation (e.g., Europe, Japan, Taiwan, Singapore, China, etc.), but America's success and pace of progress will depend on our ability to scale collaborative innovation domestically with new environments, tools, and infrastructure.

The NSTC was established "to conduct research and prototyping of advanced semiconductor technology and grow the domestic semiconductor workforce to strengthen the economic competitiveness and security of the domestic supply chain" (15 U.S.C. 4656(c)). The NSTC was directed by Congress to operate as a "public private-sector consortium" with participation from the private sector and federal research agencies. To ensure the long-term success of the NSTC and sustained industry buy-in, it is essential that the operation be continually responsive to industry technology priorities.

The Commerce Department designated Natcast (the National Center for the Advancement of Semiconductor Technology) as the purpose-built non-profit organization tasked with operating the NSTC, with $6.3 billion made available through a long-term funding agreement. The three overarching goals of the NSTC are:

- Extend U.S. technology leadership,
- Reduce the time and cost to prototype, and
- Build and sustain a semiconductor workforce development ecosystem.[9]

[9] NSTC Strategic Plan, available at https://natcast-1e229.kxcdn.com/assets/uploads/2025/02/Natcast-NSTC-Strategic-Plan-FY25-27-Feb-2025_webf.pdf

As a public-private partnership, the NSTC's work is guided both by the U.S. Department of Commerce and an expert Technical Advisory Board comprised of the leading technologists from across the semiconductor supply chain. To provide the infrastructure necessary to execute on these goals, the NSTC is establishing three primary facilities, which are described briefly below. More detailed descriptions can be found in Appendix II.

1. Prototyping and Advanced Packaging Piloting Facility: The NSTC is seeking to scale new manufacturing and advanced packaging technologies to commercial relevance and facilitate "lab-to-fab" transitions. Novel technologies tend to be initiated in academic contexts and demonstrated at small scales and low throughput. Once a proof-of-concept is demonstrated, significant development work must be done to mature the technology for deployment in commercial market. In fact, the value of a new technology cannot be assessed without sending wafers through a fully integrated manufacturing flow and measuring overall performance. The prototyping and advanced packaging piloting facility will provide this capacity with a full, integrated manufacturing flow. This facility will be located at the Arizona State University Research Park. Preliminarily activities will begin at ASU in 2026, with new construction to be completed by the end of 2028.

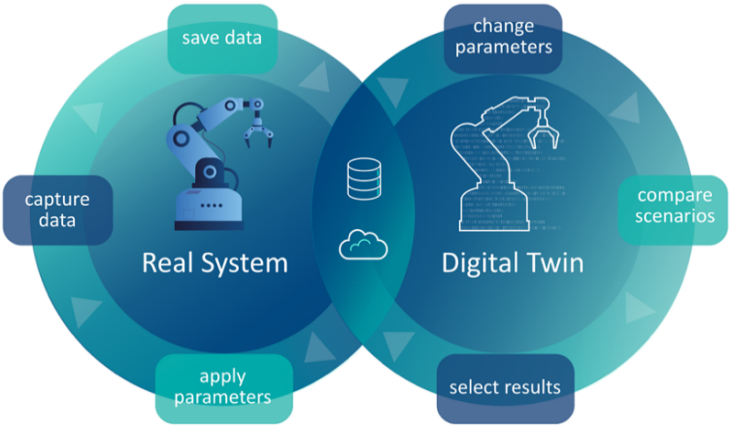
2. EUV Accelerator: Extreme ultraviolet (EUV) lithography has proven a vital and indispensable tool to manufacture advanced semiconductors, and continued advancements in EUV lithography (and even its successor, high numerical aperture (high NA) EUV lithography) are needed to enable the industry to keep pace with leading-edge manufacturing. Meanwhile, adjacent segments of the industry that enable lithography must also advance their technologies in tandem. The NSTC EUV Accelerator is tasked with democratizing access to this essential tool and supporting this entire community to develop their innovations together and bring new EUV technologies to market more rapidly. This facility is expected to open in summer of 2025.

3. Design Collaboration Facility (DCF): Determining the layout of billions of transistors across a wafer to execute a large computing workload is an extraordinarily complex task. The design segment of the semiconductor value chain comprises companies that build electronic design automation (EDA) software, IP providers that assemble libraries of design blocks to be incorporated into chip designs, and fabless firms that use EDA software and IP blocks to design full chip systems. The DCF will support R&D in design and feature a new "design enablement gateway," which will reduce barriers to chip startups by centralizing access to EDA software and data libraries. By leveraging the collective purchasing power of the NSTC and its members, the DCF will accelerate timelines and significantly reduce the growing cost associated with design and development of experimental chips and architectures. This facility is expected to open in summer of 2025.

Unlike the other CHIPS R&D Programs—whose goal is to support termed research initiatives expiring by the end of the CHIPS Act authorization—the NSTC's mission and activities is intended to outlive the CHIPS Act and be supported by private sector funds in the long term. While considerable work remains in developing its technology agenda, the NSTC is initiating long-arc programs and structures to serve as a semiconductor industry research consortium for decades.

IV. SMART USA: Innovating through Digital Twins

SMART USA (Semiconductor Manufacturing for Advanced Research with Twins) is a newly established Manufacturing USA Institute designed to advance digital twins in the U.S. semiconductor industry value chain. Digital twins are virtual representations of physical systems that remain connected in real time. This arrangement allows engineers to simulate and optimize processes virtually (using real data streams) and then apply results directly to the physical systems without the resource intensity and time constraints of physical trials. Ultimately, digital twin technology enables more innovation in the digital realm, using AI to reduce development costs and accelerate technologies to market ahead of global competitors.



Digital twins can be created at multiple levels. A single manufacturing step can be twinned to quickly optimize conditions for wafer processing. At a broader level, a critical "layer" of the manufacturing flow (some smaller number of related steps to pattern a feature) can be twinned to understand how these steps can be co-optimized to form better chips. Entire fabs can also be twinned to optimize operations across the facility. By creating digital twins at these various levels, SMART USA aims to reduce U.S. chip R&D and manufacturing costs by >40% and development cycle times by >35%.

Key initiatives of the SMART USA Institute include:

- Creating the "Digital Backbone" – a national platform for developing, testing, and deploying digital twins.
- Establishing industry-wide standards to ensure interoperability, security, and consistency in digital twin development and use.
- Building a national network of shared facilities, including fabs, packaging, assembly, and test centers, to support applied research.
- Launching a digital marketplace where organizations can share and exchange digital twin technologies, data, and best practices.
- Expanding the digital twin-capable workforce through curriculum development and trainings that use digital twins to prepare over 100,000 semiconductor workers.

Through these initiatives, SMART USA members will create the nation's first repository of secure, validated, and interoperable digital twins for the industry. They will enable the integration of AI and high-performance computing directly on the fab floor and foster real-time collaboration among manufacturers, equipment providers, and suppliers resulting in a more agile, efficient, and innovative industry.

In addition to $285 million of federal funding, SMART USA has secured non-binding commitments for over $700 million from industry and academic partners, exceeding $1 billion in total investment over a 5-year period. SMART USA will unite America's top researchers and innovative institutions, pursuing a vision for a strong, competitive, and sustainable domestic semiconductor manufacturing ecosystem.

V. Metrology: Innovating through Precision, Verification, and Digital Assets

The ability to pattern ever smaller features on a chip and the ability to stack multiple chiplets together for 3-dimensional heterogeneous integration promises to advance the capability of semiconductor products. However, given the industry's demands for absolute precision and its intolerance for error, manufacturers rely on the ability to rapidly, accurately, and precisely characterize new features and value their products.

For instance, as feature sizes become smaller, the resolution of our tools must also become smaller without compromises to the fidelity of the measurement. Also, as we stack multiple components on top of one another for advanced packaging applications, manufacturers must be able to verify things like structural integrity and adhesion at buried interfaces before committing additional components to the package.

Semiconductor metrology is the science of measuring both physical features and electrical characteristics of a chip. The CHIPS Metrology Program is making a series of high-impact investments to drive the industry's ability to make critical measurements for non-destructive factory-based processes as well as for lab-based process development and failure analysis.

These investments include hardware programs to devise new tooling capabilities at NIST, and they also include the generation of digital assets such as references, data sets, and software libraries. To deliver on the ultimate goals of the CHIPS Act, the Metrology Program is activating universities, federal lab scientists, start-ups, and corporations to drive world-leading measurement science domestically.

Winning the Chip Race through NAPMP, NSTC, SMART USA, and Metrology

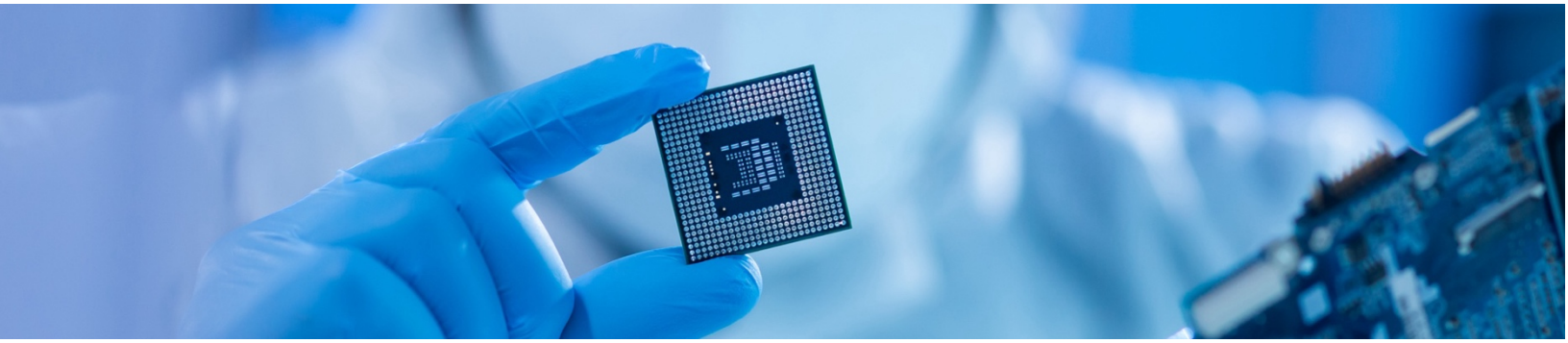
As innovation pathways evolve in the semiconductor industry, so too must American research programs to lead in the new innovation landscape and compete with global challengers. Federal research programs have traditionally provided a significant economic return on investment,[10] and the semiconductor research programs being implemented hold the promise to drive innovation, enhance competitiveness, and strengthen our economy and national security.

Collaborative research consortia are emerging around the globe to build the synergy needed to accelerate the next generations of microelectronics technologies. Taken together, the CHIPS R&D Programs are working to create the infrastructure and capabilities for the semiconductor industry in the U.S. to engage in collaboration and technology development needed to compete globally and secure American leadership in the technologies of the future. To meet the emerging innovation paradigms, federally funded semiconductor research programs remain critical to a holistic strategy of strengthening the competitiveness of the semiconductor industry in America.

As the programs build on initial progress, they must ensure that they:

- Remain responsive to industry priorities,
- Establish a range of program offerings oriented to high volume manufacturing,
- Articulate research agendas to enhance U.S. competitiveness across the industry, and
- Coordinate among each other to ensure alignment of efforts.

These programs are off to a promising start, and additional collaboration with industry will ensure they deliver on their promise of driving semiconductor innovation in the U.S.



[10] Federal government funding for semiconductor R&D offers an outsized return on investment through economy-wide benefits. Each dollar invested by the federal government into semiconductor research increases overall U.S. gross domestic product (GDP) by $16.50. Semiconductor Industry Association, "Sparking Innovation: How Federal Investment in Semiconductor R&D Spurs U.S. Economic Growth and Job Creation," June 2020. https://www.semiconductors.org/sparking-innovation/.

Appendix I: National Advanced Packaging Manufacturing Program (NAPMP) Program Descriptions

The NAPMP is structured around six R&D priorities and an integrated facility. Descriptions of the priority areas and their importance to semiconductor innovation are summarized below:

1. Materials and Substrates: Integrating a set of components from different wafers so that they may operate collectively to process a compute workload is a formidable challenge. Ideally, these components would not operate as a set of discrete elements, but as a singular system where the lines between the components are blurred and inconsequential. Data and power must be able to flow between the different components rapidly and efficiently. Interposers are substrates that have a high degree of electrical interconnects, thermal management materials, and structural mounting hardware already deposited on the substrate (glass, silicon, organic) so that "chiplets" may be more rapidly and efficiently integrated. In general, the more interconnects joining the diverse components, and the "closer" they are to one another, the more the components will function as a single system.

2. Equipment, Tools, and Processes: New factory tooling is required to prepare substrates and interposers, mount chips/chiplets, measure these processes in the fab to ensure quality, package these new systems, and build electrical connectivity.

3. Power Delivery and Thermal Management: In conventional 2D packages, heat dissipates through the top of the chip, but as chiplets are stacked on top of one another, thermal dissipation through the top of the chiplet is no longer an option. To prevent chips from overheating, the new methods are needed to shunt waste heat out of the package.

4. Photonics and Connectors: Conventional semiconductor technologies have historically transmitted data electronically throughout the system. However, moving electrons through metal wires/connectors generates significant waste heat, which can damage components. Converting digital electronic signal to an analog photonic signal allows for faster data transmission (even transmitting multiple signals through a single connector at once) without the problematic heat generation. This advancement is a significant opportunity for advanced packaging.

5. Chiplet Ecosystem: As advanced packaging technologies develop and the industry is more adept at incorporating a variety of chiplets into a package, there will be increased opportunity for the development of specialized chiplets to compete in a chiplet marketplace. These chiplets will span a wide variety of use cases and end markets.

6. Co-Design and Electronic Design Automation (EDA): The advent of advanced packaging technologies opens considerably more degrees of freedom (i.e., stacking, heterogeneous integration, larger packages) and options for new packages. EDA software must advance commensurately to optimize designs of these new packages.

Appendix II: National Semiconductor Technology Center (NSTC) Facilities Descriptions

The NSTC is establishing three primary facilities to provide infrastructure and capacity needed to advance piloting and prototyping work for commercially oriented technologies at scale. Each facility is described below:

1. EUV Accelerator

As feature sizes for advanced logic processors and memory technologies decreased, the industry began adding more steps to their already-lengthy manufacturing flows to be able to pattern ever smaller transistors (i.e., multiple patterning lithography). For semiconductor manufacturers, this meant holding more inventory as it made its way through the factory, adding tooling modules, increasing square footage of clean room space to accommodate those tools (already the most expensive square footage of real estate to construct), and more technicians and engineers to operate those fleets of tools. And, as the number of steps in the manufacturing flow increased, so too did the opportunity for error—in an industry that is famously precise and intolerant of error—which impacted yields and profitability. The development of EUV lithography dramatically reduced the need for multiple patterning, condensed manufacturing flows, and boosted yields even for the smallest feature sizes, ultimately serving to deliver more advanced chips and operate businesses sustainably.

Continued advancements in EUV lithography are needed to enable the industry to keep pace with Moore's Law and fabricate smaller and smaller transistor features. Meanwhile, adjacent segments of the industry that enable lithography must also advance their technologies in tandem. For instance, new photoresists must be developed that can provide resolution at the nanometer (or even sub-nanometer) length scale. And once the photoresist is developed, the tool makers must devise techniques for how to deposit the new photoresist very uniformly and thinly across the surface of the wafer. Finally, metrology companies will need to figure out how to measure all of this with the precision that the industry demands. The NSTC EUV Accelerator will serve a critical role supporting this entire community to develop their innovations together and bring new EUV technologies to market.

The EUV Accelerator will be housed at the Albany Nanotech Complex, which is set to be North America's only public research center with access to high numerical aperture (NA) EUV lithography. With a sticker price of ~$350 million, high NA EUV is the most critical and advanced manufacturing tool to enable patterning of leading-edge processors. And access to this first-of-a-kind tool will be democratized through the NSTC, affording valuable access for a groundswell of American start-ups that will build leadership domestically. Furthermore, housing and maintaining such a tool is enormously costly. By siting the EUV Accelerator at this complex, the NSTC has identified an important means of reducing capital expenditures and accelerating the availability of this resource. NY CREATES, which operates the complex, is set to receive $825 million from the NSTC. The facility is planned to begin operations in summer of 2025.

2. Design and Collaboration Facility

Determining the layout of billions of transistors across a wafer to execute a complex computing workload is an extraordinarily complex task. The design segment of the semiconductor value chain comprises companies that build electronic design automation (EDA) software, IP providers that assemble libraries of design blocks to be incorporated into chip designs, and fabless firms that use EDA software and IP blocks to design full chip systems. Moreover, this industry segment sits at the nexus between the hardware providers and software providers, critical to full stack innovation.

The NSTC Design and Collaboration Facility will support R&D in design and feature a new "design enablement gateway," which will reduce barriers to chip startups by centralizing access to EDA software and data libraries. By leveraging the collective purchasing power of the NSTC and its members, the DCF will accelerate timelines and significantly reduce the growing cost associated with design and development of experimental chips and architectures. The facility is also set to be the core of the NSTC Workforce Center of Excellence, which will invest $250 million in programs focused on developing semiconductor talent – including technicians, engineers, and researchers – across education levels and disciplines to address projected shortages in the chip workforce.[11] This Natcast-operated facility will also house the NSTC's core administrative functions, right in the heart of Silicon Valley and is set to be operational in 2025.

3. Prototyping and Advanced Packaging Piloting Facility

The NSTC will also scale new technologies to commercial relevance and facilitate "lab-to-fab" transitions for new materials, devices, and advanced packaging solutions in a state-of-the-art R&D environment. Novel technologies tend to be initiated in academic contexts and demonstrated at relatively small scales and low throughput. Once a proof-of-concept is demonstrated, there is significant development work that must be done to mature the technology before it can enter the market. For example, in semiconductor equipment, issues of uniformity across a wafer, run-to-run consistency, throughput rate, and many others all must be optimized before a tool can be deemed "mature." Meanwhile, the value a new technique adds to a wafer must be reconciled with the what the market is willing to pay for it. R&D teams have both science and economic problems that must be resolved in order to justify use of a new technology. Oftentimes, this value cannot be assessed properly without sending wafers through a full integrated manufacturing flow and measuring overall performance.

The prototyping and advanced packaging piloting facility will provide capacity to develop and scale technologies toward commercial relevance, and it will house a full, integrated manufacturing flow so that technologies may be fully proved out. This facility will be located at the Arizona State University Research Park. Preliminarily activities will begin at ASU in 2026, while construction of the new facility will be finished to begin operations by the end of 2028. While considerable work remains, the NSTC has already attracted nearly 150 members, including leading chip companies and universities, and is poised to be one of America's leading semiconductor research consortia in the years ahead.

[11] Semiconductor Industry Association / Oxford Economics, "Chipping Away: Assessing and Addressing the Labor Market Gap Facing the U.S. Semiconductor Industry," July 2023. https://www.semiconductors.org/chipping-away-assessing-and-addressing-the-labor-market-gap-facing-the-u-s-semiconductor-industry/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